

# quantum<mark>d</mark>ata

# 980 DP1.2 Video Generator Module Video Pattern Testing of DisplayPort 1.2 Displays

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#### 980 DP1.2 Video Generator Module



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# 980 DP1.2 Video Generator Module Overview

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## 980 DP1.2 Video Generator Module – General Features

- Supports maximum link symbol rates of up to 2160-Mbytes/second for testing DP1.2 HBR2 capable displays with 4 lanes up to 5.4Gb/s.
- Pattern testing
  - Over 300 test patterns.
  - Configure image parameters through convenient GUI dialog boxes.
  - Advanced features such as Deep Color and 3D test patterns and formats.
- Format library
  - Over 600 timings (formats).
  - Configure format parameters through convenient GUI dialog boxes.
  - Format editor enables custom creation of formats.
- Continues...

### 980 DP1.2 Video Generator Module – General Features

- Protocol Testing
  - HDCP authentication.
- EDID Decode
  - View sink's EDID in human readable text.

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## 980 DP1.2 Video Generator Module – DP Specific Features

- DPCD register decode
  - View DPCD registers and link status in human readable text.
- Monitoring Aux Channel with Auxiliary Channel Analyzer (ACA) application.
  - View EDID exchanges.
  - View DPCD exchanges.
  - View HDCP authentication transactions.
  - View link training transactions.

## • Set link training parameters:

- Force link training ("non-adaptive") set link rate, number of lanes, clock recovery, equalization, symbol lock, etc.
- Auto link training ("adaptive") application automatically configures link in the optimal way based on the capabilities of the cable and sink device.



#### 980 DP1.2 Video Generator Module in 980B

 980 DP 1.2 Video Generator module placed in slots 3 or 6 of the 980B chassis.

Contract PORT:HDMI2-T70 INTF:HDMI2-T70 INTF:HDMI INTF:HDMI INTF:HDMI IMM	f:/Standard/2160p60.xml 5:/Standard/GraysAll.img 2840p2150 Brogrossius 1	H:135.00kHz F:60.00Hz	put 🧬 Disconnect
Format	Pattern Audio	Cools	Refresh
Resolution         V           240p2x         240p4x         262           288p2x         288p4x         312	Frame Rate           • 263         • 24/1.001         • 24           • 313         • 25	Aspect 480p59 Ratio VIC 2 • 4:3 480p60	HDMI Generator Card 1 DisplayPort
● 480p ● 480p2x ● 480i2x ● 480p4x ● 480i4x	30/1.001     30     50     60/1.001     60	● 16:9 ● 64:27 ● 256:135 ● 256:135	H H H H H H Card 6
576p           576p2x         576i2x           576p4x         576i4x	● 10 ● 120/1.001 ● 12 ● 20	0 Box 0 Fill 4:3 0 VIC 3 720p59 VIC 4 720p59 VIC 4	Card 7 HDMI Playback Card 3
○ 720p           ○ 1080p         ○ 1080i           ○ 2160p	● 240/1.001 ● 24 5 ● 1250	0 ● 16:9 VIC 4 ● 1.85:1 1080i29 ● 2.39:1 VIC 5	
		1080130 VIC 5 4801222	9
Left to Right 👻 💿	Settings 📄 Edit 🜔 Clear Sel	ection @ Apply	
			X Close
			000
			796
	0		



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#### 980 DP1.2 Video Generator Module in 980R

 980 DP 1.2 Video Generator module placed in slots 1,3 or 6 of the 980R chassis.



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# 980 DP1.2 Video Generator Module Operation – Video Pattern Testing

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#### 980 DP1.2 Video Generator Module – DP1.2 Transmitter



Select Generator application:

 Generator to access GUI for controlling DP and HDMI generator modules.

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## 980 DP1.2 Video Generator Module – DP1.2 Transmitter



Select video mode:

 Select between DP1.2 or HDMI and DVI from HDMI module.

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💷 Generator					
Interface v INTF:DISPLAY_PORT	FMT:/Standard/CVR1260.xr IMG:/Standard/SmpteBar.: 1280x960 Progressio	nl img ze RGB-8bpp	H:59. F:59.	20 kHz 92Hz P:85.25MHz	🔊 Disconnect
Format	Pattern		<mark>%</mark> å Te	pols	C Refresh
🚺 CEA 💦 Folder 🔲 Lists	s EDID				
J6750 APP0875	APP1059 APP1075	APP1175	CEA0659	CVR0760	DisplayPort Generator Card 3
CVR0812 CVR0860	CVR0860H CVR0960D	CVR1012	CVR1060	CVR1060D	HDMI 2.0
CVR1060H CVR1060_	CVR1160 CVR1160D	CVR1212	CVR1212D	CVR1212E	Generator Card 5
CVR1212G CVR1260	CVR1260D CVR1260E	CVR1260G	CVR1260H	CVR1312H	HDMI Generator
CVR1360H CVR1412	CVR1412D CVR1460	CVR1460D	CVR1560D	CVR1612	Card 7
CVR1612D CVR1660	CVR1660D CVR1660_	CVR1760D	CVR1760H	CVR1860	HDMI Playback Card 6
CVR1860H CVR1960	CVR1960D CVR1960H	CVR2060	CVR2060D	CVR2060H	
CVR2160H CVR2360D	CVR2460D CVR2560E	CVR2560H	CVR2760H	CVT0675	
CVT0675D CVT0685	CVT0685D CVT0685H	CVT0760D	CVT0775D	CVT0785D	
СVT0850 СVT0850Н	СVT0860 СVT0860Н	CVT0875	СVТ0875Н	CVT0885	
CVT0885H CVT0950D	CVT0960D CVT0975D	CVT0985D	CVT1050	CVT1050D	
Select Path: /Standard				8	
	Edit 🤇 💿 Settings 🖉 🛴	Find ) ( ち Trar	nsfer		A V
					💢 Close

Select Format:

- Select timing format from Format Library from the Folder activation button.
- Scroll through list of format timings.
- Over 600 formats to select from.

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Select Format:

- Use Find tool to locate formats quickly.
- Find tool allows partial strings.

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I Generator				
Interface v No VIC Code	PORT IMG:/Standard/CV PORT IMG:/Standard/Sm 1280x960 Pro	R1260.xml pteBar.img ogressive RGB-8bpp	H:59.20kHz F:59.92Hz F:85.2	put 🦻 Disconnect
Format		Pattern	Ca Tools	C Refresh
CEA       Folder         1080i25       1080i29         480i2x29       480i2x30         480p59SH       480p60         576p50LH       576p50SH         DMT0660       DMT0675         DMT1260G       DMT1275G         SVD02H1       SVD02H2         SVD03H1       SVD03H2         SVD05H1       SVD05H2         SVD06L1       SVD06L2	Lists         EDID           1080i30         1060p.           480i2xL1         480i2xL2           480p60LH         480p60SH           720p50         720p59           DMT0860         DMT0875           DetDEL1         DetDEL2           SVD02H3         SVD02H4           SVD03L1         SVD03L2           SVD06L3         SVD06L4	1080p24       1080p50         48012xS1       48012xS2         57612x25       57612xLH         720p60       CVT1660D         DMT1060       DMT1075         IBM0770H       SVD01H1         SVD02L1       SVD02L2         SVD04H1       SVD04H2         SVD06H1       SVD07H2	1080p59       1080p60         480p59       480p59LH         576i2xSH       576p50         CVT1960H       DMT0659         DMT1175       DMT1260D         SVD01L1       SVD01L2         SVD02L3       SVD02L4         SVD06H3       SVD06H4         SVD07L1       SVD07L2	<ul> <li>DisplayPort Generator Card 3</li> <li>HDMI 2.0 Generator Card 5</li> <li>HDMI Generator Card 7</li> <li>HDMI Playback Card 6</li> </ul>
Bood EDID and Concrete Ed				•
Read EDID and Generate For	Edit O Settings	🔵 🚺 Find 🔰 Trans	fer	
				🔀 Close

Select Format:

• Configure list of formats based on the EDID of the connected display.

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Select Format:

- For CEA formats, use CEA smart filtering tool to locate formats.
- Select parameters either left to right or "Arbitrary."

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Create custom lists of formats:

- Configure a specific test of formats for viewing and selecting.
- Save for later reuse.

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🔳 Generator									
Interface	PORT:DP-T3	0/31 FM AY_PORT IM	T:/Standard G:/Standard 1280x960	/CVR1260.xml /SmpteBar.img Progressive	RGB-8bpp		H:59.20kHz F:59.92Hz	P:85.25MHz	🔊 Disconnect
	Format			Pattern			😪 Tools		😂 Refresh
CEA	🐚 Folder	Lists	EDID EDID						
2160p60	1080p60	CVR2060	CVR1260	CVR1960				•	DisplayPort Generator Card 3
									HDMI 2.0 Generator Card 5
									HDMI Generator Card 7
									HDMI Playback Card 6
								•	
C Select	ists: MyFormatL	ist						*	
		🛛 📝 Edit	) 💿 Setti	ngs 🛛 属 Find	d) ( <b>5</b> Ti	ransfer			A V
									X Close

Select Format (Timing):

 Create your own custom format lists using the editor utilities.

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Configure Format Settings:

- Select timing format from Format Library.
- Configure format parameters such as Color Space, Sampling, Range and Bits per Component (two examples shown).

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#### 980 DP1.2 Video Generator Module – Format Editor

Format Editor: /Sta	ndard/CVT2550H.xml	😤 Navigator 🛛 🕀 Home 🖙 E
finning Genera	TY Digital Video Y Digital Audio Y AFD	
	Pixel Rate 256.250007 MHz 3.902439 hs	Entry Units
	Horizontal Ver <u>tical</u>	O Machine
R	T4.146414 KHz III 49.963891 Hz	• Time
	Tune 1.000000 Base 74.146414 KHz	Scan Type
Ac	2560 Pixels 💋 9.990244 us 1440 Lines 📝 19.421034 ms	Interlace
Bir	896 Pixels III 3.496585 us 44 Lines III 0.593420 us	Back Porch
Tot	3456 Pixels 2 13.486829 us 1484 Lines 20.014454 ms	Clock Pulse
PL	176         Pixels         0.686829         us         3         Lines         0.040460         ms           272         Pixels         1.061462         ns         5         Lines         0.067434         ms	PreEmphasis
		DC Balance
	Serration width Adjustment 0 Pixels Eq. Before 0 Lines	Flat Front Porch
	H to V Pulse Delay 0 Pixels Eq. After 0 Lines	Repeat Field
	🕨 Use 🛛 🕞 New 🕞 Open 🛛 🕞 Save	

Create custom formats:

- Use Format Editor to create additional custom formats.
- Tweak individual format parameters.
- Apply immediately for testing or save custom formats for later reuse.

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Select Test Patterns:

- Select test pattern from Pattern Library.
- Over 300 test patterns to select from.
- Scroll through patterns using scroll bar.

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Configure pattern parameters:

Set test pattern
 parameters such as
 color and gamma.

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Configure pattern parameters:

 Some test patterns have variations. The Rendition tab enables you to test with any of these other "Renditions".

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Configure pattern parameters:

 The Level tab enables you to set the luminance in IRE of the test pattern.

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Configure pattern parameters:

 Put a marker on the Tx1 output so that you can distinguish which module Tx port is connected to.

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## 980 DP1.2 Video Generator Module – Image Scrolling



Scroll any test pattern with Image Scroll feature:

- Select scroll speed in horizontal and vertical axes.
- Select extent of travel.
- Select reverse or repeat scrolling.

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# 980 DP1.2 Video Generator Module Configuring Link Training Parameters

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## 980 DP1.2 Video Generator – Configure Link Training

I Generator		- • •
PORT:DP-T30/31         FMT:CVT1660D.xml         H           Interface v         INTF:DISPLAY_PORT         IMG:/Standard/SmpteBar.img         F           No VIC Code         1680x1050         Progressive RGB-8bpp	:65.29kHz :59.95Hz P:146.25MHz	Disconnect
📮 Format	🗶 Tools	Refresh
Link Train DPCD Viewer HDCP Test EDID Decode Image Shift 3D Editors Adaptive Training Mon-Adaptive Training Train at Lane Count 0 1 0 2 0 4 Train Based on Capabilities Train Based on Capabilities	Symbol locked Symbol locked Symbol locked Symbol locked	DisplayPort Generator Card 3 HDMI 2.0 Generator Card 5 HDMI Generator Card 7 HDMI Playback Card 6
		A V X Close

Select Link Train tool:

 Provides current status of link training on top panel.

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## 980 DP1.2 Video Generator – Configure Link Training

💷 Generator		
Interface v POR	T:DP-T30/31         FMT:CVT1660D.xml         H:65.29kHz           F:DISPLAY_PORT         IMG:/Standard/SmpteBar.img         F:59.95Hz	🛛 🍠 Disconnect
No VIC Code	1680x1050 Progressive RGB-8bpp P:146.25MH	
<u> </u>	Pormat Pattern 7 Tools	Refresh
Link Train	Current Status	DisplayBart
DPCD Viewer	Main Stream: Enabled	Generator
	Lane Count: 4 Lanes	Card 3
HUCP Test	Link Rate: 5.40 Gbps per Lane	HDMI 2.0
EDID Decode	Lane 2: CR done, ChannelEQ done, Symbol locked	Generator
Image Shift	Lane 3: CR done, ChannelEQ done, Symbol locked	Card 5
	Lane 4: CR done, ChannelEQ done, Symbol locked Inter-lane Alignment: Yes	НДМІ
)	Defreeh	Generator
Editors	Reliesn /	Card 7
	Adaptive Training Non-Adaptive Training	НДМІ
	Train at Lane Count	Playback
	Train at Tink Pate (Chng)	
	Irain Based on Capabilities	
		💢 Close

Select Link Train tool:

- Select between Adaptive (automatic) link training and Non-Adaptive (shown in example).
- Set limits on source lane count and link rate capabilities.

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## 980 DP1.2 Video Generator – Configure Link Training



Select Link Train tool:

- Select between
   Adaptive (automatic shown in example) link
   training and Non Adaptive (user control).
- Enables precise control over lane count and link rate.

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# 980 DP1.2 Video Generator Module Viewing EDIDs

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View EDIDs – Select Interface:

 Select which Tx port to view EDID of connected display.

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View EDIDs – Select Interface:

 Select which Tx port to view EDID of connected display.

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Decode and view EDIDs:

- View EDIDs of connected display in human readable text.
- Navigate through block
   0 per page.
- Navigate through block
  1 per page.

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💷 Generator			
Interface v IN	RT:DP-T30/31 FMT:CVT1660D.xml FF:DISPLAY_PORT IMG:/Standard/SmpteBar.img 1680x1050 Progressive RGR-8ppp	H:65.29kHz F:59.95Hz	connect
	Format	😤 Tools 🗧 Ref	resh
Link Train	DP.T30 ᢦ ) ( ™ Read ) ( 📓 Save ) (	🖻 Load	
DPCD Viewer	Block #01 CFA Data Block: Tag 2 bytes 16: Video Data	Disp	olayPort nerator
HDCP Test	Number of Descriptors: 16 SVD #001: (16) 1920x1080p & 60 Hz 16:9 Native	C.	ard 3
EDID Decode	SVD #002: (5) 1920x1080j @ 60 Hz 16:9 SVD #003: (4) 1280x720p @ 60 Hz 16:9	( HD Ger	MI 2.0 nerator
Image Shift	SVD #004: (3) 720x480p @ 60 Hz 16:9 SVD #005: (2) 720x480p @ 60 Hz 4:3	c	ard 5
3D	SVD #006: (7) 720(1440)x480i 0 60 Hz 16:9 SVD #007: (22) 720(1440)x576i 0 50 Hz 16:9 SVD #008: (1) 640x480p 0 60 Hz 4:3	( H Ger	IDMI nerator
Editors	SVD #008: (1) 640x480p @ 60 H2 4:3 SVD #009: (6) 720(1440)x480i @ 60 Hz 4:3 SVD #010: (17) 720x576p @ 50 Hz 4:3 SVD #011: (18) 720x576p @ 50 Hz 16:9 SVD #012: (21) 720(1440)x576i @ 50 Hz 4:3 SVD #013: (19) 1280x720p @ 50 Hz 16:9 SVD #014: (20) 1920x1080i @ 50 Hz 16:9 SVD #015: (31) 1920x1080p @ 50 Hz 16:9 SVD #016: (32) 1920x1080p @ 24 Hz 16:9	Ci H Pla Ci	ard 7 HDMI hyback ard 6
	Block < 2/2 >	Page < 2/8 ≽ 🔥 🗶	lose

Decode and view EDIDs:

- View EDIDs of connected display in human readable text.
- Navigate through block
  0 (1) per page.
- Navigate through block
  1 (2) per page.

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Decode and view EDIDs:

- View EDIDs of connected display in human readable text.
- Save EDIDs for emulation testing of sources.

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# 980 DP1.2 Video Generator Module Viewing DPCD Registers

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	Generator				
		RT:DP-T30/31 F:DISPLAY_PORT	FMT:CVT1660D.xml IMG:/Standard/SmpteBar.img	H:65.29kHz F:59.95Hz	🔊 Disconnect
No	VIC Code	Format	1680x1050 Progressive RGB-8bpp	P:146.25MHz	🕄 Refresh
C	Link Train	Receive	DP-T30 v C Read All	Read Page 🤇 🔤 Report )	Diseles Dect
	DPCD Viewer	Capability 00000-0008F	DPCD Revision ?	2: 00000-0008F	Generator
	HDCP Test	Link			Card 3
C	EDID Decode	00100-001C2			HDMI 2.0 Generator
C	Image Shift	Link/Sink Status			Card 5
Ć	3D	00200-00217 00280-002FF			HDMI Generator
Ć	Editors	) Test			Card 7
		Automation 00218-00270			HDMI Playback
		Source			Card 6
		00300-003FF			
		Sink Specific			
		00400-004FF			
		Branch Specific			
		00500-005FF			
		Sink Control			
	A V	00600			A V
					X Close

View DPCD Registers:

- Select DPCD Viewer.
- Select DP Tx port to view DPCD of connected display.

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💷 Generator						
Interface v PORT	P:DP-T30/31 DISPLAY_PORT	FMT:CVT1660D.xml IMG:/Standard/SmpteBar.img	PGB-9hpp	H:65.29kHz F:59.95Hz		S Disconnect
	Format	Pattern	KGB-GDPP	😤 Tools	P.146.25Mi2	S Refresh
Link Train	Receiver Capability		Receiver Capability	Page ) Report	)	DisplayPort
DPCD Viewer	00000-0008F	DPC Register data has not been r	D Revision ??: 00000 ead.	-0008F		Generator Card 3
	Configuration					HDMI 2.0
Image Shift	Link/Sink					Generator Card 5
3D	Status 00200-00217 00280-002FF					HDMI Generator
Editors	Test					Card 7
	00218-00270					(HDMI Playback
	Source Specific					Card 6
	Sink Specific 00400-004FF					
	Branch Specific 00500-005FF					
	Sink Control					
A V	00600	I				A V
						💢 Close

View DPCD Registers:

 Read either the entire DPCD or read each page.

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I Generator						- • •
Interface V INTE No VIC Code	DP-T30/31 DISPLAY_PORT	FMT:CVT16 IMG:/Star 1680x	560D.xml ndard/SmpteBar.img 1050 Progressive	RGB-8bpp	H:65.29kHz F:59.95Hz F:146.25MHz	Disconnect
🧧 🖳 🖳 F	ormat		Pattern		👫 Tools	😂 Refresh
Link Train	Receiver		DP-T30 👻 🤇 🎅 Re	ad All ) ( 🤹 Read Pag	ge 🔵 📼 Report 🔵	
DPCD Viewer	Capability 00000-0008F		DPC	Receiver Capability D Revision 1.2: 00000-000	08F	DisplayPort Generator
HDCP Test	Link Configuration	00000: DI Bit	PCD_REV Name	Value	Description	HDMI 2.0
EDID Decode	00100-001C2	7-4	MAJOR REV	1		Generator
Image Shift	Link/Sink Status	3-0	MINOR_REV	2		Card 5
3D	00200-00217 00280-002FF	00001: M2 Bit	AX_LINK_RATE Name	Value	Description	HDMI Generator
Editors	Test	7-0	MAX_LINK_RATE	14h	5.4 Gbps per lane	Card 7
	Automation 00218-00270	00002: M2 Bit	AX_LANE_COUNT Name	Value	Description	HDMI Playback Cord 6
	Specific 00300-003FF	4-0 5 6	MAX_LANE_COUNT TPS3 SUPPORTED	4 1 Y(1)	4 lanes Reserved	
	Sink Specific	7	ENHANCED_FRAME_CAI	P Y(1)		
	00400-004FF Branch	00003: M2 Bit	AX_DOWNSPREAD Name	Value	Description	
	Specific 00500-005FF	0 1	MAX_DOWNSPREAD	1 0	Up to 0.5% Reserved	
	Sink	2		0	Reserved	
	Control	4		ŏ	Reserved	
	00600	5	NO AUX HANDSHAFF	0	Reserved	
A V	ESI	7	NO_AOA_NANDONAKE_I	0	Reserved	A V
						X Close

View DPCD Registers:

Reading Receiver
 Capability.

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💷 Generator							
Interface v PORT	F:DP-T30/31 F:DISPLAY_PORT	FMT:CVT1 IMG:/Star 1680x	660D.xml ndard/SmpteBar.img (1050 Progressive RGB-8bpp		H:65.29kHz F:59.95Hz P:146.25MH		Disconnect
E F	ormat		Pattern		😤 Tools	12	Refresh
Link Train	Receiver		DP-T30 👻 🞅 Read All	🗯 Read Pa	ge 🛛 🕅 🔤 Report		
	Capability		Link Confi DPCD Revision 1	iguration	102		DisplayPort
DPCD Viewer	0000-000			.2. 00100-00		~	Generator
( HDCP Test )	Link	00100: L	INK_BW_SET	Velue	Description		
	Configuration		Name	vaiue			HDMI 2.0
EDID Decode	Link/Sink	7-0	LINK_BW_SET	14h	5.4 Gbps per lane		Generator
( Image Shift )	Status	00101: L	ANE_COUNT_SET				
30	00200-00217	Bit	Name	Value	Description		номі
	00280-002FF	4-0	LANE_COUNT_SET	4	4 lanes		Generator
(Editors	Test	5		0	Reserved		
	Automation	7	ENHANCED_FRAME_CAP	Y(1)	REBEIVED		ндмі
	Source	00102· T	DAINING DATTEDN SET.				Playback
	Specific	Bit	Name	Value	Description		
	00300-003FF	1-0	TRAINING RATTERN SELECT		None		
	Sink	2	TRAINING_FATTERN_DEBECT	0	Reserved		
	Specific	3		0	Reserved		
	00400-004FF	4	RECOVERED_CLOCK_OUT_EN	N(0)			
		5	SCRAMBLING_DISABLE	N(0)			
	Branch	7-6	SYMBOL_ERROR_COUNT_SEL	0	Disparity and Symbol er		
	Specific						
	00500-005FF	00103: 1 Bit	Name	Value	Description		
	Sink			varue			
	Control	1-0	VOLTAGE SWING SET	0	Level #		
	00600	2	MAX_SWING_REACHED	N(O)			
		4-3	PRE-EMPHASIS_SET	1	Level #		
	ESI	5	MAX_PRE-EMPHASIS_REACHED	N(0)		Ŧ	A V
							X Close

View DPCD Registers:

# Read Link Configuration page.

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I Generator							
Interface v PORT	DP-T30/31 DISPLAY PORT	FMT:CVT16 IMG:/Stan	60D.xml dard/SmpteBar.img		H:65.29kHz F:59.95Hz	]	🖻 Disconnect
No VIC Code	_	1680x	1050 Progressive RGB-8bpp		P:146.25MH	z	
🔋 F	ormat		🛃 Pattern		😤 Tools		🖹 Refresh
	Receiver		DP-T30 👻 🎅 Read All 🔪	💈 Read Pag	ge ) 🗖 🔤 Report )		
	Capability		Link/Sin	k Status		1	DisplayPort
( DPCD Viewer )	00000-0008F		DPCD Revision 1.2: 002	200-00217 002	280-002FF		Generator
	Link	00200: SI	INK COUNT		ſ	Î\	Card 3
	Configuration	Bit	Name	Value	Description		
EDID Decode	00100-001C2					-7	HDMI 2.0
$\succ$	Link/Sink	6	CP PEADY	1 N(0)	Bits 7 + 5:0		Card 5
( Image Shift )	Status		CF_READI	N(0)			
$\succ$	00200-00217	00201: DE	VICE_SERVICE_IRQ_VECTOR			1	НОМІ
3D	00280-002FF	Bit	Name	Value	Description	ľ	Generator
	Test	0	REMOTE CONTROL COMMAND PENI	DING N(0)			Card 7
	Automation	1	AUTOMATED_TEST_REQUEST	N(0)			
	00218-00270	2	CP_IRQ	N(0)			HDMI
		3	MCCS_IRQ	N(0)			Playback
	Source	4	DOWN_REP_MSG_RDY	N(0)			Card 6
	Specific	5	SINK SPECIFIC IPO	N(0)			
	00300-003FF	7	SINK_SPECIFIC_INg	0	Reserved		
	Sink	-		2			
	Specific	00202: LA	NE0_1_STATUS:				
	00400-004FF	Bit	Name	Value	Description		
	Branch	0	LANE0 CR DONE	Y(1)			
	Specific	1	LANEO CHANNEL EQ DONE	Y(1)			
	00500-005FF	2	LANE0_SYMBOL_LOCKED	Y(1)			
		3		0	Reserved		
	Sink	4	LANE1_CR_DONE	Y(1)			
	Control	5	LANE1_CHANNEL_EQ_DONE	Y(1)			
	00600	6	LANEI_SIMBOL_LOCKED	Y(1)	Pagarwad		
A V	ESI	,		0	REBELVEU	-	A V
							X Close

View DPCD Registers:

• Read Link/Sink Status page.

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💷 Generator						- • •
Interface v PORT INTF No VIC Code	DP-T30/31 DISPLAY_PORT	FMT:CVT10 IMG:/Star 1680x	560D.xml ndard/SmpteBar.img 1050 Progressive RGB-8bpp		H:65.29kHz F:59.95Hz F:146.25MHz	🔊 Disconnect
E Fe	ormat	$\mathbf{M}$	🕂 Pattern		👫 Tools	🕄 Refresh
Link Train	Receiver		DP-T30 👻 🎅 Read All 🤇	Read Page	ge 🔵 🚾 Report 🔵	
DPCD Viewer	Capability 00000-0008F		Test Auto DPCD Revision 1.	mation .2: 00218-002	270	DisplayPort Generator
HDCP Test	Link Configuration	00218: TI Bit	EST_REQUEST Name	Value	Description	HDMI 2.0
EDID Decode	00100-001C2 Link/Sink	0	TEST_LINK_TRAINING TEST_PATTERN	N(0) N(0)		Generator Card 5
Image Shift	Status 00200-00217	2 3	TEST_EDID_READ PHY_TEST_PATTERN	N(0) N(0)		НДМІ
Editors	00280-002FF Test	5	FAUX_IESI_FAITERN	0	Reserved Reserved	Generator Card 7
	Automation 00218-00270	7 00219: TI	EST LINK RATE	0	Reserved	HDMI Playback
	Source	Bit	Name	Value	Description	Card 6
	Specific 00300-003FF	7-0	TEST_LINK_RATE	00h	Reserved	
	Sink Specific	00220: TH Bit	EST_LANE_COUNT Name	Value	Description	
	Branch Specific 00500-005FF	4-0 5 6 7	TEST_LANE_COUNT	0 0 0	Reserved Reserved Reserved Reserved	
	Sink Control 00600	00221: TI Bit	EST_PATTERN Name	Value	Description	
A V	ESI	7-0	Requested Pattern	0	None	A V
						X Close

View DPCD Registers:

Read Test Automation page.

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💷 Generator			
Interface v No VIC Code	C:DP-T30/31 C:DISPLAY_PORT	FMT:CVT1660D.xml     H:65.29kHz       IMG:/Standard/SmpteBar.img     F:59.95Hz       1680x1050     Progressive       RGB-8bpp     P:146.25Mi	Disconnect
🤅 F	ormat	Pattern 🎇 Tools	🔁 🍣 Refresh
Link Train	Receiver	DP-T30 👻 🤶 Read All 🤇 🗯 Read Page 🖉 🔤 Report	
	Capability	Source Specific DPCD Revision 1.2: 00300-003FF	DisplayPort
	00000-0008F		Card 3
( HDCP Test )	Link	00300: SRC_IEEE_OUI	
	00100-001C2	001. 00000m (0)	HDMI 2.0
	Link/Sink	00303: SRC_DEVICE_ID_STRING	Generator
(Image Shift )	Status	ASCII: ""	
3D	00200-00217	00309: SEC HARDWARE REVISION	
$\succ$	00280-002FF	Bit Name Value Description	Generator
( Editors )	Test		
	Automation	7-4 Major Revision 0	НДМІ
	00218-00270		Playback
	Source	0030A: SRC_FW_SW_MAJOR_REV	Card 6
	5pec111C	varae = oon (o)	
	Cinh	0030B: SRC_FW_SW_MINOR_REV	
	Specific	Value = 00n (0)	
	00400-004FF	0030C: SRC_VENDOR_SPECIFIC(0)	
	Branch		
	Specific	[031C][00 00 00 00 00 00 00 00][]	
	00500-005FF	[0324][00 00 00 00 00 00 00][]	
	Sink		
	Control	[033C][00 00 00 00 00 00 00 00][]	
	00600	[0344][00 00 00 00 00 00 00][]	
A V	ESI	[034C][00 00 00 00 00 00 00 00][] [03541[00 00 00 00 00 00 00][]	- A V
			¥ Close

View DPCD Registers:

Read Source Specific page.

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I Generator			_ • •
Interface v PORT INTF No VIC Code	DP-T30/31 DISPLAY_PORT	FMT:CVT1660D.xml         H:65.29kHz           IMG:/Standard/SmpteBar.img         F:59.95Hz           1680x1050         Progressive           RGB-8bpp         P:146.	utput 🔊 Disconnect
E Fe	ormat	Pattern 👫 Tools	S Refresh
Link Train	Receiver Capability	DP-T30 v Read All Read Page Report Sink Specific DPCD Revision 1.2: 00400-004FF	DisplayPort
Drcb viewei	00000-0008F		Card 3
(HDCP Test	Link Configuration	00400: SINK_IEEE_OUI OUI: 0080E1h (32993)	
EDID Decode	00100-001C2	00403. SINU DEVICE ID STRING	HDMI 2.0 Generator
Image Shift	Link/Sink Status	Bytes: 44 70 31 2E 32 00 ASCII: "Dp1.2"	Card 5
3D	00200-00217 00280-002FF	00409: SINK_HARDWARE_REVISION Bit_Name Value Description	HDMI Generator
Editors	Test		E Card 7
	Automation 00218-00270	3-0Minor Revision07-4Major Revision0	HDMI Playback
	Source Specific	0040A: SINK_FW_SW_MAJOR_REV Value = 00h (0)	Card 6
<b></b>	Sink	0040B: SINK_FW_SW_MINOR_REV Value = 00h (0)	
	00400-004FF	0040C: SINK_VENDOR_SPECIFIC(0) [040C][00 00 02 01 00 80 E1 44][D]	
	Branch Specific	[0414][70 31 2E 32 00 00 00 00][p1.2] [041C][00 00 02 01 00 80 E1 44][D]	
	00500-005FF	[0424][70 31 2E 32 00 00 00 00][p1.2] [042C][00 00 02 01 00 80 E1 44][D]	
	Sink	[0434][70 31 2E 32 00 00 00][p1.2]	
	00600	[0444][70 31 2E 32 00 00 00 00][p1.2]	
AV	ESI	[044C][00 00 02 01 00 80 E1 44][D] [0454][70 31 2E 32 00 00 00 00][p1.2]	
			X Close

View DPCD Registers:

Read Sink Specific page.

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View DPCD Registers:

Read Sink Control page.

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# 980 DP1.2 Video Generator Module Monitoring Aux Channel Transactions

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#### 980 DP1.2 Video Generator - Auxiliary Channel Analyzer

- Monitor Aux Channel transactions (Link Training, DPCD exchanges, HDCP and EDID) through Auxiliary Channel Analyzer (ACA).
- 980 Video Generator module emulates DP1.2 source and monitors DPCD exchanges, Link Training transactions, HDCP authentication transactions and EDID exchanges.



#### 980 DP1.2 Video Generator Module – Monitor Link Training

,	DT2C	30	$> B \cdot A = E D T = 16$		St	art Time: 00:00:35.9268			
	DIZC	20		•		Type: Native			😑 Bac
5	DIZC	30	< ACK 00 38 4C IE 5I II 00 0A.		D	Direction: Reply			
9	DPLT	30	> W:100 LINK_BW_SET L=1 14		Poply to	Command: ACK			 to Nav
3	DPLT	30	< ACK		Kepty to	Reau Request.			
L	DPLT	30	> W:101 LANE_COUNT_SET L=1 84		00202: L	ANE0_1_STATUS:			
2	DPLT	30	< ACK		Bit	Name	Value	Description	🕞 Sta
3	DPLT	30	> W:107 DOWNSPREAD_CTRL L=1 00		0	LANEG CR DONE	N(0)		
1	DPLT	30	< ACK		1	LANEG_CHANNEL_EQ_DONE	N(0)		Pau
5	DPLT	30	> W:102 TRAINING PATTERN SET: I		2	LANEO_SYMBOL_LOCKED	N(0) 0	Reserved	
6	DPLT	30	 < ACK		4	LANE1_CR_DONE	N(0)		
,		20	> W-103 TRAINING LANED SET 1-4		5	LANE1_CHANNEL_EQ_DONE	N(0)		
,		20			7	LANEI_STHBUL_LUCKED	0	Reserved	
5	DPLI	30							
	DPLI	30	> W:103 TRAINING_LANE0_SET L=4		00203: L Bit	ANE2_3_STATUS Name	Value	Description	
3	DPLT	30	< ACK						
L	DPLT	30	> R:202 LANE0_1_STATUS: L=6		0	LANE2_CR_DONE	N(0) N(0)		
2	DPLT	30	< ACK 00 00 80 00 44 44		2	LANE2_CHANNEL_EQ_DONE	N(0)		
3	DPLT	30	> W:103 TRAINING_LANE0_SET L=4		3		0	Reserved	🔧 Eve
1	DPLT	30	< DEFER		4	LANE3_CR_DONE LANE3_CHANNEL_E0_DONE	N(0) N(0)		
5	DPLT	30	> W:103 TRAINING_LANE0_SET L=4		6	LANE3_SYMBOL_LOCKED	N(0)		🗢 Dat
5	DPLT	30	< ACK		7		0	Reserved	1
,	DPI T	30	> R:202 LANEO 1 STATUS: L=6		00204: L	ANE_ALIGN_STATUS_UPDATED			
,		20	< ACK 11 11 90 00 44 44		Bit	Name	Value	Description	
		30	S NEW II II OU OU 44 44		0	INTERLANE ALIGN DONE	N(0)		
		30	> W:102 IKAINING_PAILEKN_SEI: I		í		0	Reserved	
1	DPLT	30	< ALK		2		0	Reserved	
	DPLT	30	> W:103 TRAINING_LANE0_SET L=4	6	4		0	Reserved	
2	DPLT	30	< ACK		5		0	Reserved	
3	DPLT	30	> R:202 LANE0_1_STATUS: L=6		6	DOWNSTREAM_PORT_STATUS_CHANGED	N(0) Y(1)		
Ļ	DPLT	30	< ACK 77 77 81 00 44 44				,		🛛 🛃 Clea
	DPLT	30	> W:102 TRAINING_PATTERN_SET: I		00205: S	SINK_STATUS	Value	Description	
;					DIL	name	vacue	Description	Done of
i i	DP <u>LT</u>	30	< ACK						C Ope

View Aux Chan Link Training transactions:

• Select Specific record to view details.

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#### 980 DP1.2 Video Generator Module – Monitor Link Training

	► [-] I	Events:	384	97, Pending: 0					P		🕞 Home
	38467	DPLT	10	> W:102 TRAINING_PATTERN_SET: L=1 22		St	art Time: 05:28:22.9635			-	~
	38468	DPPRE	10	Precharge/Sync Count: 26		n	Type: Native				🗢 Back
	38469	DPLT	10	< ACK			Command: ACK				-
	38470	DPPRE	10	Precharge/Sync Count: 32		Reply to	Read Request.				🔁 Nav.
	38471	DPLT	10	> W:103 TRAINING LANEO SET L=4 00 00 00 00		00100 1	TNK RW SET				
	38472	DPPRE	10	Precharge/Sync Count: 26		Bit	Name	Value	Description		🥚 Stop
	38473	DPLT	10	< ACK		7-0	LINK BW SET	0Ah	2.7 Gbps per l		-
	38474	DPPRE	10	Precharge/Sync Count: 32					zir aspo per e		Resur
	38475	DPLT	10	> R:202 LANEO 1 STATUS: L=6		00101: L Bit	ANE_COUNT_SET Name	Value	Description		
	38476	DPPRE	10	Precharge/Sync Count: 26							
	38477	DPLT	10	< ACK 77 77 01 01 00 00		4-0	LANE_COUNT_SET	4	4 Lanes Reserved		
	38478	DPPRE	10	Precharge/Sync Count: 32		6		0	Reserved		
	38479	DPLT	10	> W:102 TRAINING PATTERN SET: L=1 00			ENHANCED_FRAME_CAP	¥(1)			
	38480	DPPRE	10	Precharge/Sync Count: 26		00102: T	RAINING_PATTERN_SET:	¥-1	Deservitetien		
	38481	DPLT	10	< ACK		B10	Name	vatue	Description		
	38482	DPPRE	10	Precharge/Sync Count: 32		1-0	TRAINING_PATTERN_SELECT	0	None		
	38483	DPLT	10	> R:202 LANEO 1 STATUS: L=3		2		0	Reserved -		💐 Event
	38484	DPPRE	10	Precharge/Sync Count: 26		4	RECOVERED_CLOCK_OUT_EN	N(0)			
	38485	DPLT	10	< ACK 77 77 01		7-6	SYMBOL_ERROR_COUNT_SEL	0	Disparity and		🗢 Data
	38486	DPPRE	10	Precharge/Sync Count: 32		00102. T	DATNING LANED SET				
	38487	DNAT	10	> R:200 SINK COUNT L=8		Bit	Name	Value	Description		
	38488	DPPRE	10	- Precharge/Sync Count: 26		1-0	VOLTAGE SWING SET		Level #		
	38489	DNAT	10	< ACK 41 00 77 77 01 03 00 00		2	MAX_SWING_REACHED	N(Ö)			
	38490	DPPRE	10	Precharge/Sync Count: 32		4-3	PRE-EMPHASIS_SET MAX_PRE-EMPHASIS_REACHED	0 N(0)	Level #		
	38491	DPLT	10	> R:100 LINK BW SET L=8		6		0	Reserved		
	38492	DPPRE	10	Precharge/Sync Count: 26				0	Reserved		
	38493	DPLT	10	< ACK 0A 84 00 00 00 00 00 00		00104: T	RAINING_LANE1_SET	¥-1	Description		
/	38494	DPPRE	10	Precharge/Sync Count: 32			name	vatue	Description		🔒 Clear
	38495	DNAT	10	> R:200 SINK_COUNT L=8		1-0	VOLTAGE_SWING_SET	0 N(0)	Level #		
	38496	DPPRE	10	Precharge/Sync Count: 26		4-3	PRE-EMPHASIS_SET	0	Level #	•	🙋 Open
	38497	DNAT	10	< ACK 41 00 77 77 01 03 00 00	6	4					
					$\odot$	<	>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>	84 00	00 00 00 00	0	📙 Save

View Aux Chan Link Training transactions:

• Select Specific record to view details.

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#### 980 DP1.2 Video Generator Module – Monitor Link Training

► [-] E	events:	384	97, Pending: 0					$\mathcal{P}$		🖰 Home
38467	DPLT	10	> W:102 TRAINING_PATTERN_SET: L=1 22	•	St	art Time: 05:28:22.9676			*	
38468	DPPRE	10	Precharge/Sync Count: 26		D	irection: Reply				🗢 Back
38469	DPLT	10	< ACK			Command: ACK				
38470	DPPRE	10	Precharge/Sync Count: 32		Reply to	Read Request.				🔽 Nav.
38471	DPLT	10	> W:103 TRAINING_LANE0_SET L=4 00 00 00 00		00200: S	INK COUNT				
38472	DPPRE	10	Precharge/Sync Count: 26		Bit	Name	Value	Description		🥚 Stop
38473	DPLT	10	< ACK			SINK_COUNT	1	Bits 7 + 5:0		
38474	DPPRE	10	Precharge/Sync Count: 32		6	CP_READY	Y(1)			Resum
38475	DPLT	10	> R:202 LANE0_1_STATUS: L=6		00201: D	EVICE_SERVICE_IRQ_VECTOR				
38476	DPPRE	10	Precharge/Sync Count: 26		Bit	Name	Value	Description		
38477	DPLT	10	< ACK 77 77 01 01 00 00		0	REMOTE_CONTROL_COMMAND_PENDING	5 N(0)			
38478	DPPRE	10	Precharge/Sync Count: 32		1	AUTOMATED_TEST_REQUEST	N(0) N(0)			
38479	DPLT	10	> W:102 TRAINING_PATTERN_SET: L=1 00		3	HCCS_IRQ	N(0)			
38480	DPPRE	10	Precharge/Sync Count: 26		4	DOWN_REP_MSG_RDY	N(0) N(0)			
38481	DPLT	10	< ACK		6	SINK_SPECIFIC_IRQ	N(0)			
38482	DPPRE	10	Precharge/Sync Count: 32		7		0	Reserved		_
38483	DPLT	10	> R:202 LANE0_1_STATUS: L=3		00202: L	ANE0_1_STATUS:				💐 Events
38484	DPPRE	10	Precharge/Sync Count: 26		B1t	Name	Value	Description		
38485	DPLT	10	< ACK 77 77 01		0	LANEO_CR_DONE	Y(1)			🗢 Data
38486	DPPRE	10	Precharge/Sync Count: 32		1	LANEG_CHANNEL_EQ_DONE LANEG SYMBOL LOCKED	Y(1) Y(1)			
38487	DNAT	10	> R:200 SINK_COUNT L=8		3		0	Reserved		
38488	DPPRE	10	Precharge/Sync Count: 26		4	LANEI_CR_DONE LANEI CHANNEL EQ DONE	Y(1) Y(1)			
38489	DNAT	10	< ACK 41 00 77 77 01 03 00 00		6	LANE1_SYMBOL_LOCKED	Y(1)	Deserved		
38490	DPPRE	10	Precharge/Sync Count: 32				0	Keserved		
38491	DPLT	10	> R:100 LINK_BW_SET L=8		00203: L	ANE2_3_STATUS	v-1	Deservintion		
38492	DPPRE	10	Precharge/Sync Count: 26		B1t	name	vatue	Description		
38493	DPLT	10	< ACK 0A 84 00 00 00 00 00 00		0	LANE2_CR_DONE	Y(1)			
38494	DPPRE	10	Precharge/Sync Count: 32		2	LANE2_CHANNEL_EQ_DONE LANE2_SYMBOL_LOCKED	Y(1)			🔒 Clear
38495	DNAT	10	> R:200 SINK_COUNT L=8		3		0	Reserved		
38496	DPPRE	10	Precharge/Sync Count: 26		4 5	LANE3_CK_DUNE LANE3_CHANNEL_EQ_DONE	Y(1)			🗁 Open
38497	DNAT	10	< ACK 41 00 77 77 01 03 00 00	69	6	LANE3_SYMBOL_LOCKED	Y(1)		•	
				•	<	> 38497: < ACK 41	00 77	77 01 03 00	0	📙 Save

View Aux Chan Link Training transactions:

• Select Specific record to view details.

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Select test images for DP protocols:

• Select HDCPProd test image.

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#### 980 DP Video Generator - Auxiliary Channel Analyzer



Monitoring DDC Transactions with HDMI sink device:

 Show details of selected item in human text.

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#### **Quantum Data 980 Video Test Generation Module**



... 980 now supports video pattern testing of DP1.2-capable displays.



