



quantumdata

# **980 DP1.2 Video Generator Module**

## **Video Pattern Testing of DisplayPort 1.2 Displays**

# 980 DP1.2 Video Generator Module



# 980 DP1.2 Video Generator Module Overview

# 980 DP1.2 Video Generator Module – General Features

- Supports maximum link symbol rates of up to 2160-Mbytes/second for testing DP1.2 HBR2 capable displays with 4 lanes up to 5.4Gb/s.
- Pattern testing
  - Over 300 test patterns.
  - Configure image parameters through convenient GUI dialog boxes.
  - Advanced features such as Deep Color and 3D test patterns and formats.
- Format library
  - Over 600 timings (formats).
  - Configure format parameters through convenient GUI dialog boxes.
  - Format editor enables custom creation of formats.
- Continues...

# 980 DP1.2 Video Generator Module – General Features

- Protocol Testing
  - HDCP authentication.
- EDID Decode
  - View sink's EDID in human readable text.

# 980 DP1.2 Video Generator Module – DP Specific Features

- DPCD register decode
  - View DPCD registers and link status in human readable text.
- Monitoring Aux Channel with Auxiliary Channel Analyzer (ACA) application.
  - View EDID exchanges.
  - View DPCD exchanges.
  - View HDCP authentication transactions.
  - View link training transactions.
- Set link training parameters:
  - Force link training (“non-adaptive”) – set link rate, number of lanes, clock recovery, equalization, symbol lock, etc.
  - Auto link training (“adaptive”) – application automatically configures link in the optimal way based on the capabilities of the cable and sink device.

# 980 DP1.2 Video Generator Module in 980B

- 980 DP 1.2 Video Generator module placed in slots 3 or 6 of the 980B chassis.



# 980 DP1.2 Video Generator Module in 980R

- 980 DP 1.2 Video Generator module placed in slots 1,3 or 6 of the 980R chassis.





# **980 DP1.2 Video Generator Module Operation – Video Pattern Testing**

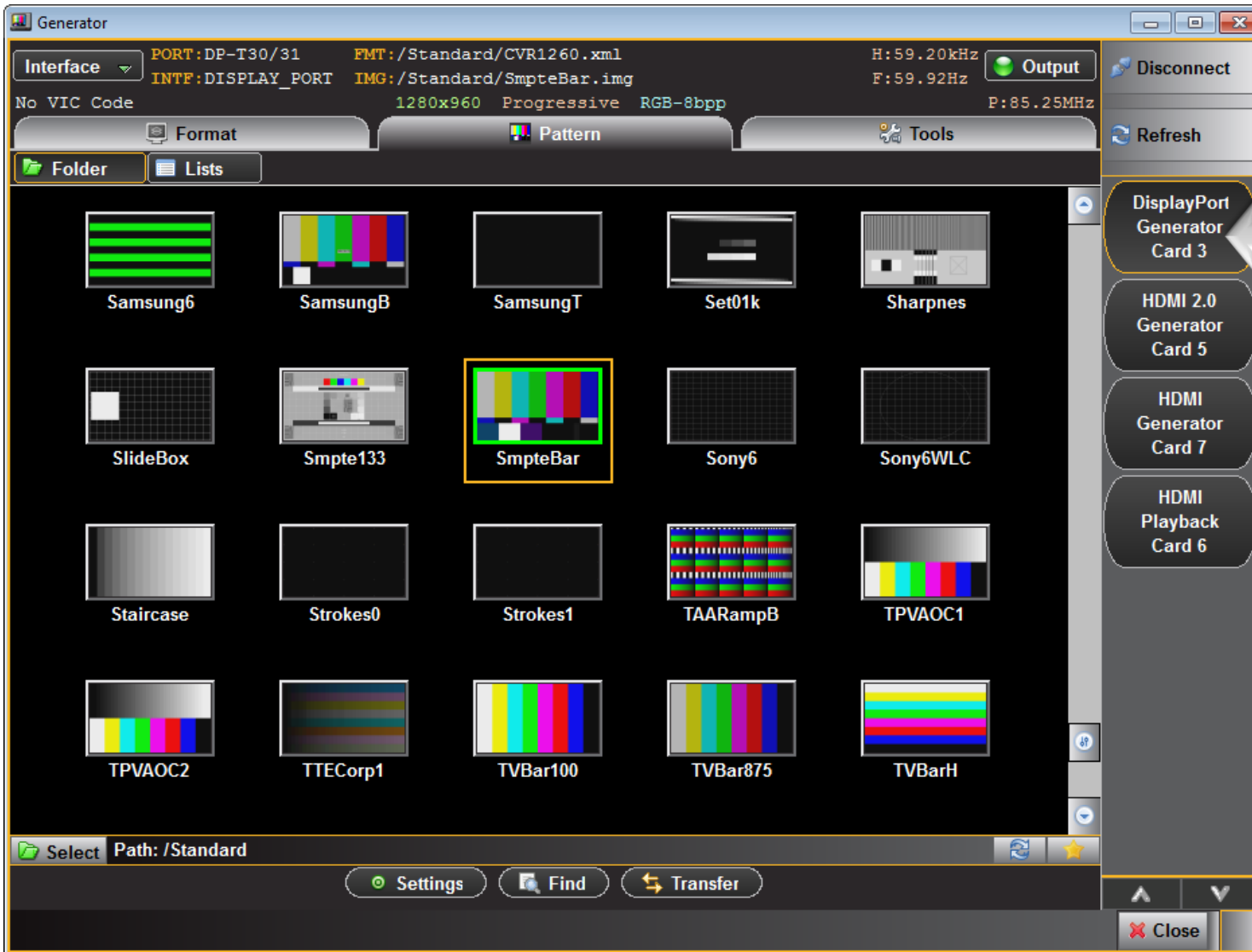
# 980 DP1.2 Video Generator Module – DP1.2 Transmitter



Select Generator application:

- Generator to access GUI for controlling DP and HDMI generator modules.

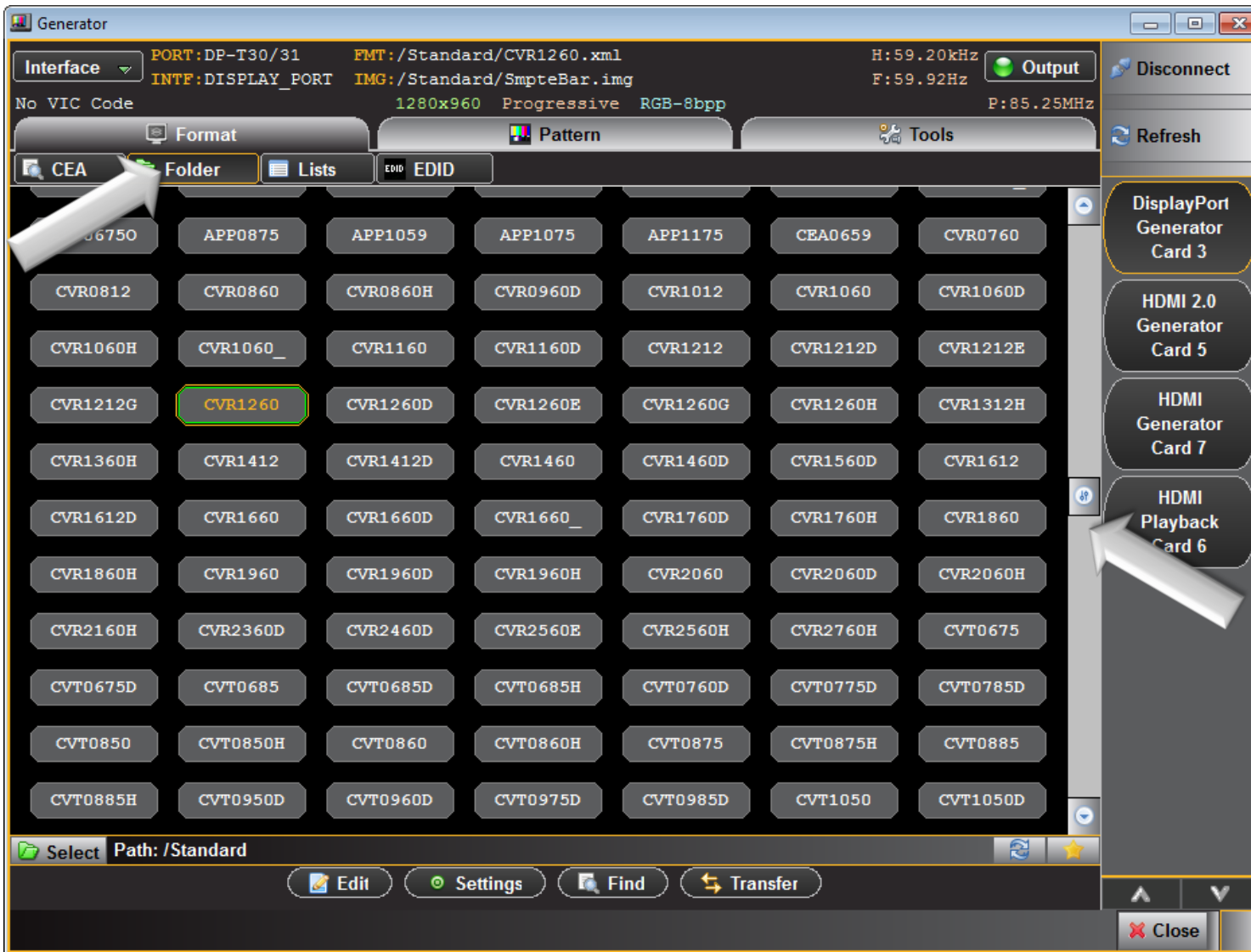
# 980 DP1.2 Video Generator Module – DP1.2 Transmitter



Select video mode:

- Select between DP1.2 or HDMI and DVI from HDMI module.

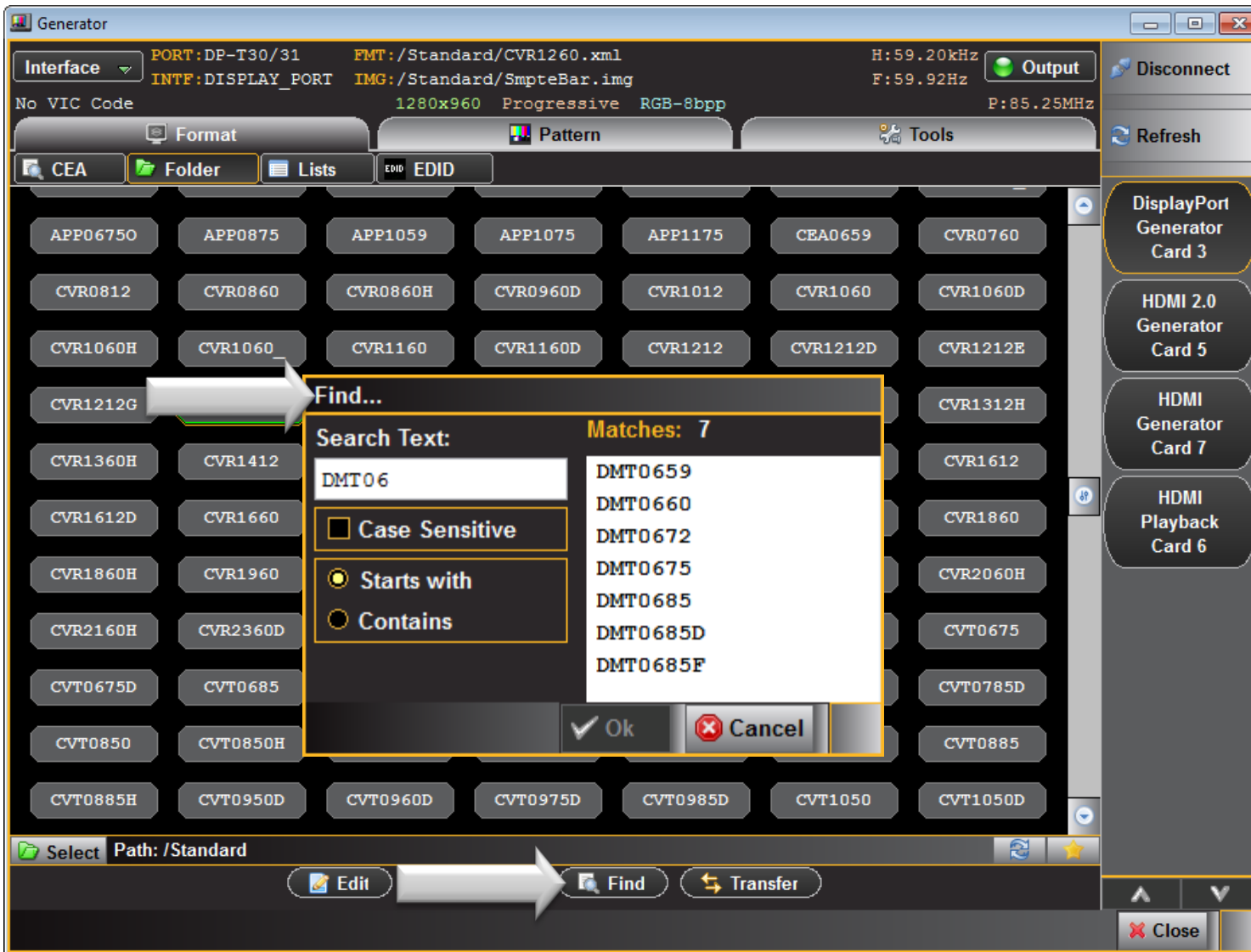
# 980 DP1.2 Video Generator Module – Format Selection



## Select Format:

- Select timing format from Format Library from the Folder activation button.
- Scroll through list of format timings.
- Over 600 formats to select from.

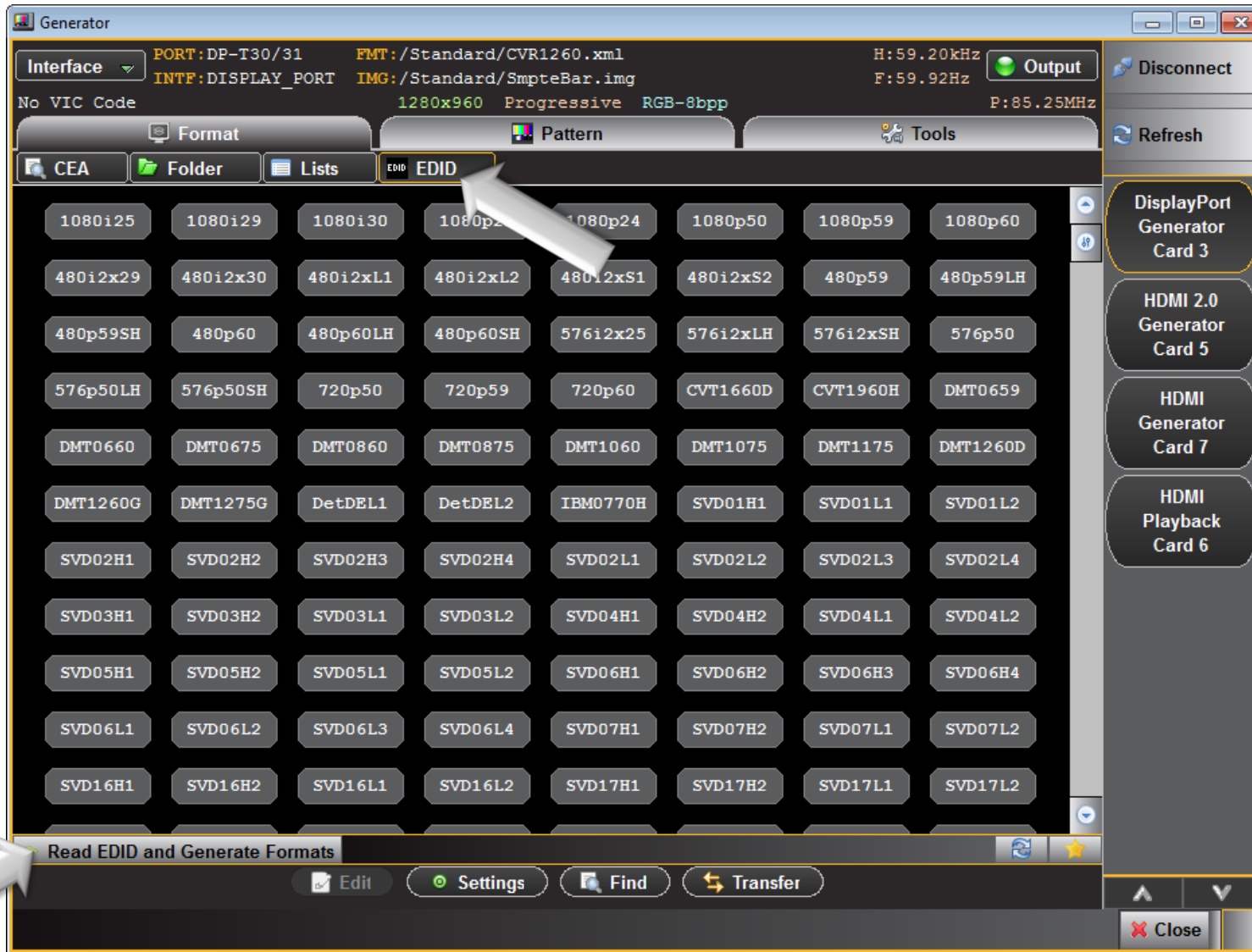
# 980 DP1.2 Video Generator Module – Format Selection



## Select Format:

- Use Find tool to locate formats quickly.
- Find tool allows partial strings.

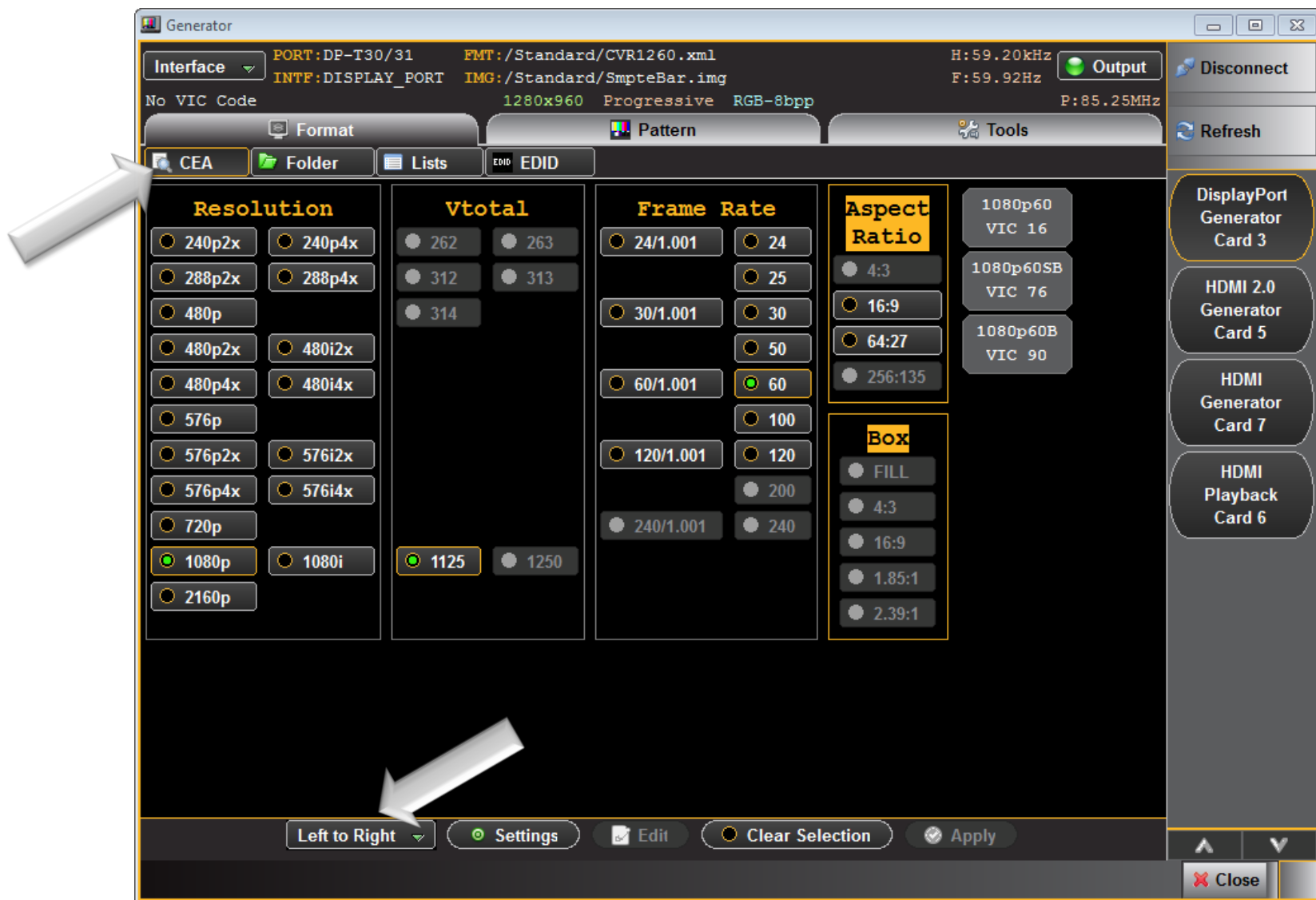
# 980 DP1.2 Video Generator Module – Format Selection



Select Format:

- Configure list of formats based on the EDID of the connected display.

# 980 DP1.2 Video Generator Module – Format Selection



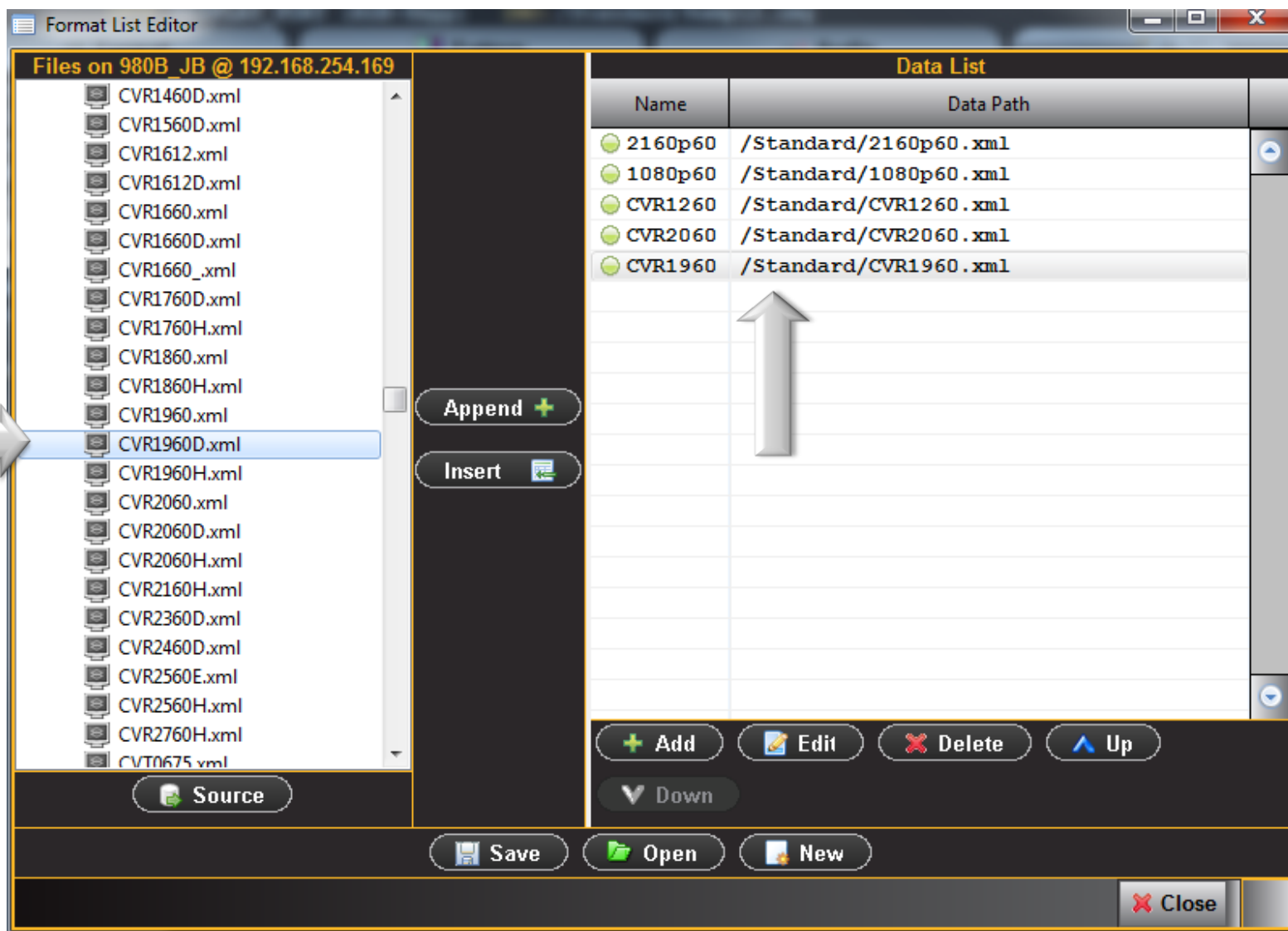
## Select Format:

- For CEA formats, use CEA smart filtering tool to locate formats.
- Select parameters either left to right or “Arbitrary.”

# 980 DP1.2 Video Generator Module – Format Selection

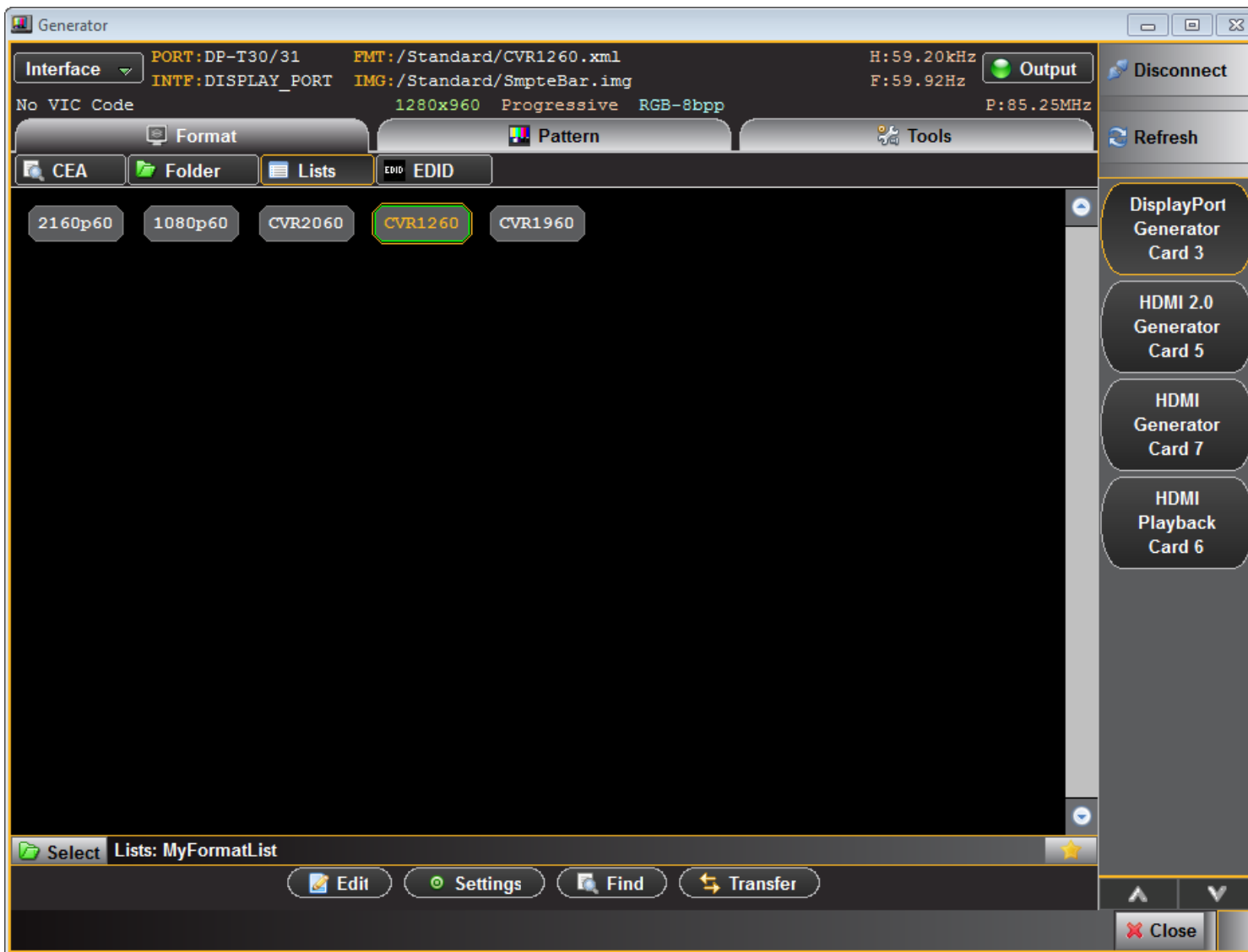
Create custom lists of formats:

- Configure a specific test of formats for viewing and selecting.
- Save for later reuse.





# 980 DP1.2 Video Generator Module – Format Selection



## Select Format (Timing):

- Create your own custom format lists using the editor utilities.

# 980 DP1.2 Video Generator Module – Format Selection



## Configure Format Settings:

- Select timing format from Format Library.
- Configure format parameters such as Color Space, Sampling, Range and Bits per Component (two examples shown).

# 980 DP1.2 Video Generator Module – Format Editor

Format Editor: /Standard/CVT2550H.xml

Timing | General | Digital Video | Digital Audio | AFD

Pixel Rate: 256.250007 MHz

Horizontal: 74.146414 KHz

Vertical: 49.963891 Hz

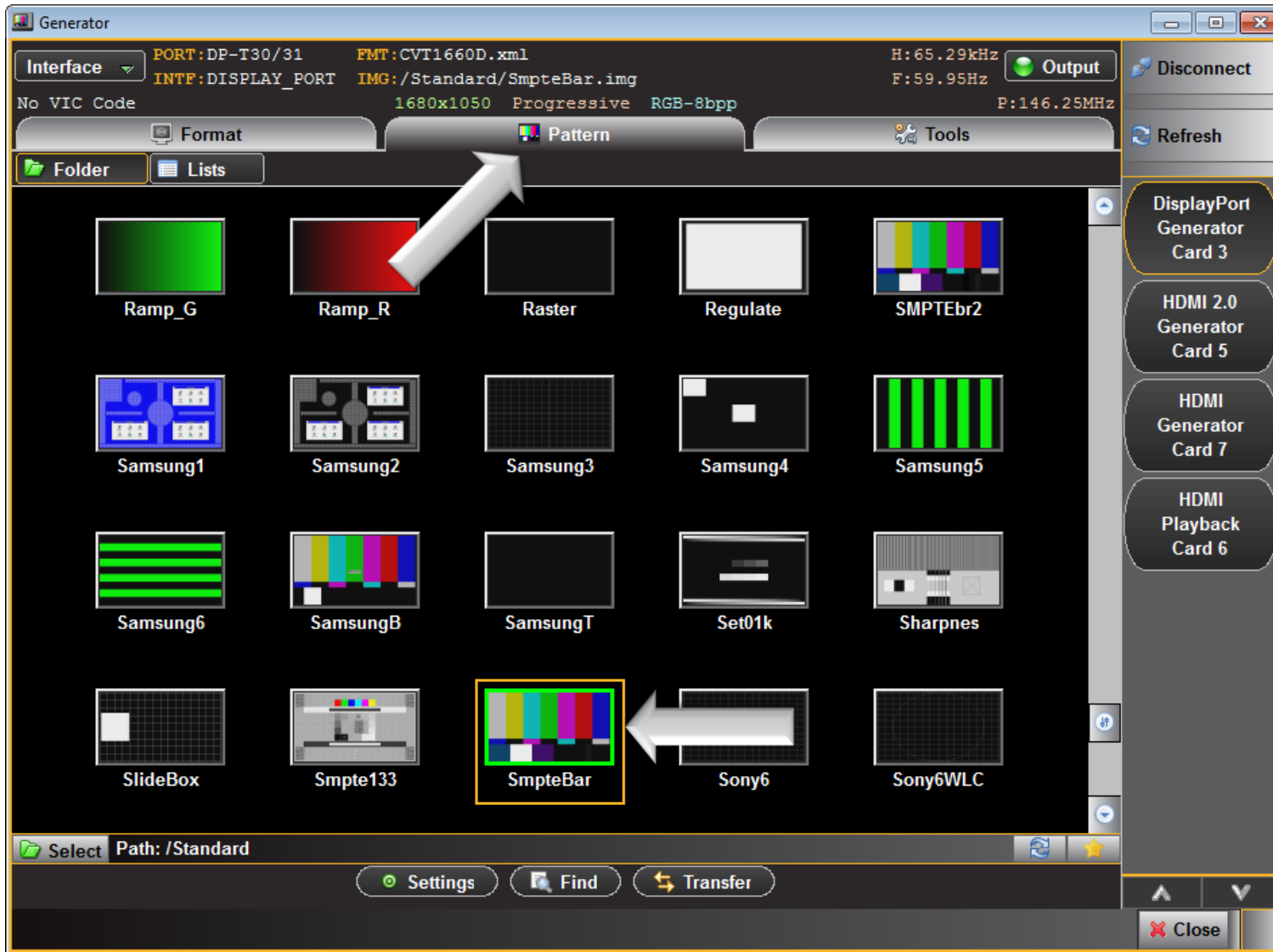
Parameter	Horizontal	Vertical
Rt	74.146414 KHz	49.963891 Hz
Act	2560 Pixels	1440 Lines
Bln	896 Pixels	44 Lines
Tot	3456 Pixels	1484 Lines
PD	176 Pixels	3 Lines
PW	272 Pixels	5 Lines

Buttons: Use, New, Open, Save

Create custom formats:

- Use Format Editor to create additional custom formats.
- Tweak individual format parameters.
- Apply immediately for testing or save custom formats for later reuse.

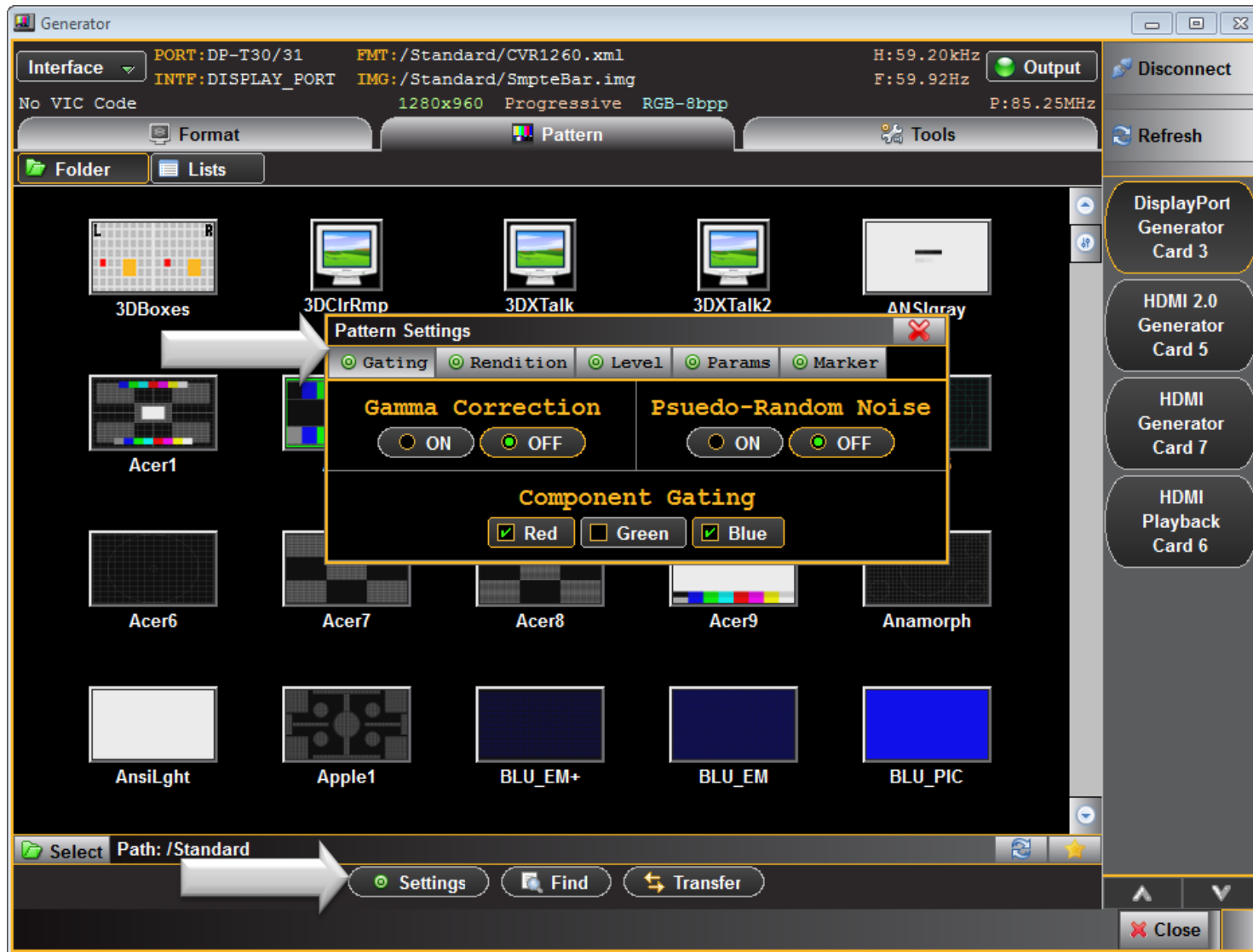
# 980 DP1.2 Video Generator Module – Pattern Testing



## Select Test Patterns:

- Select test pattern from Pattern Library.
- Over 300 test patterns to select from.
- Scroll through patterns using scroll bar.

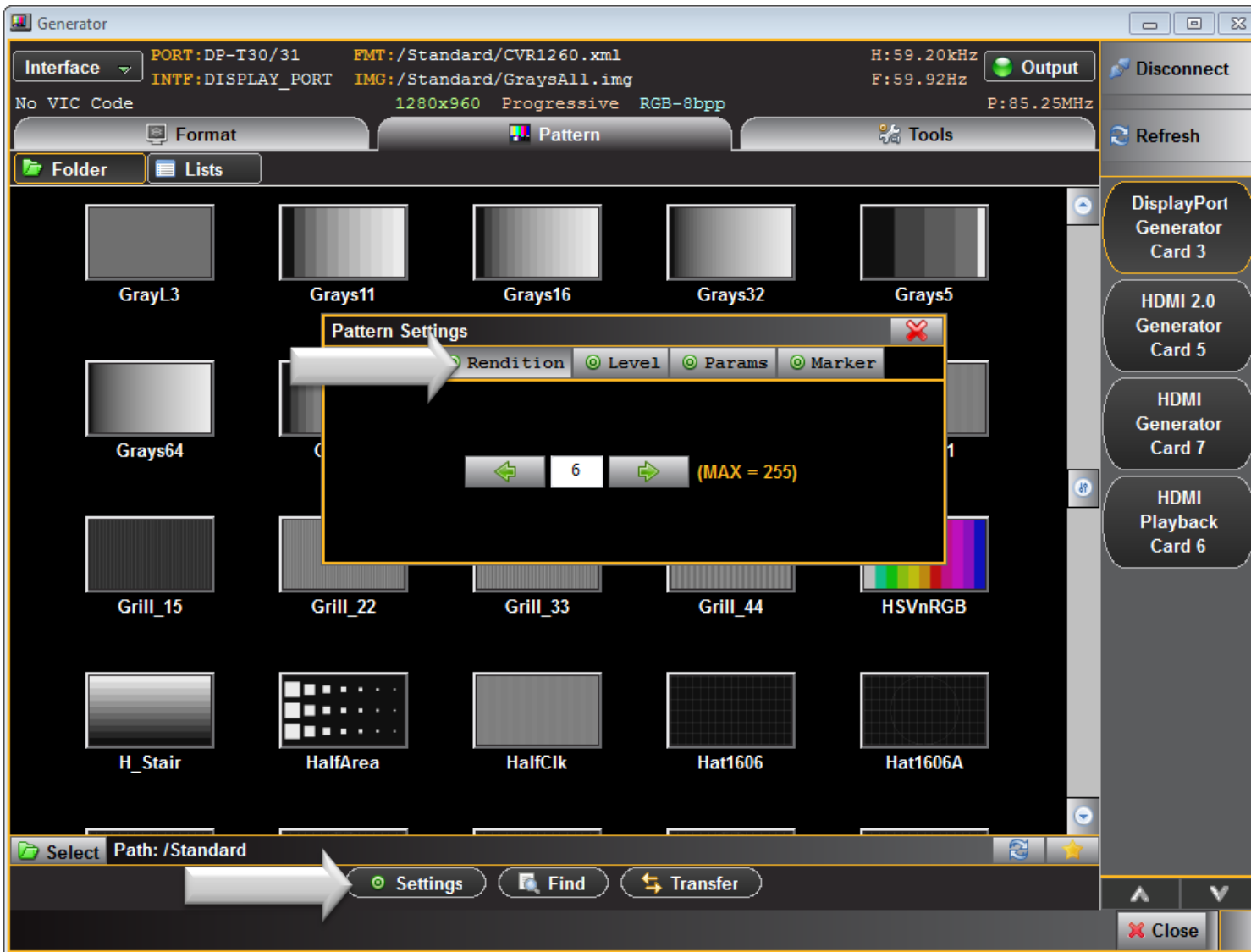
# 980 DP1.2 Video Generator Module – Pattern Testing



Configure pattern parameters:

- Set test pattern parameters such as color and gamma.

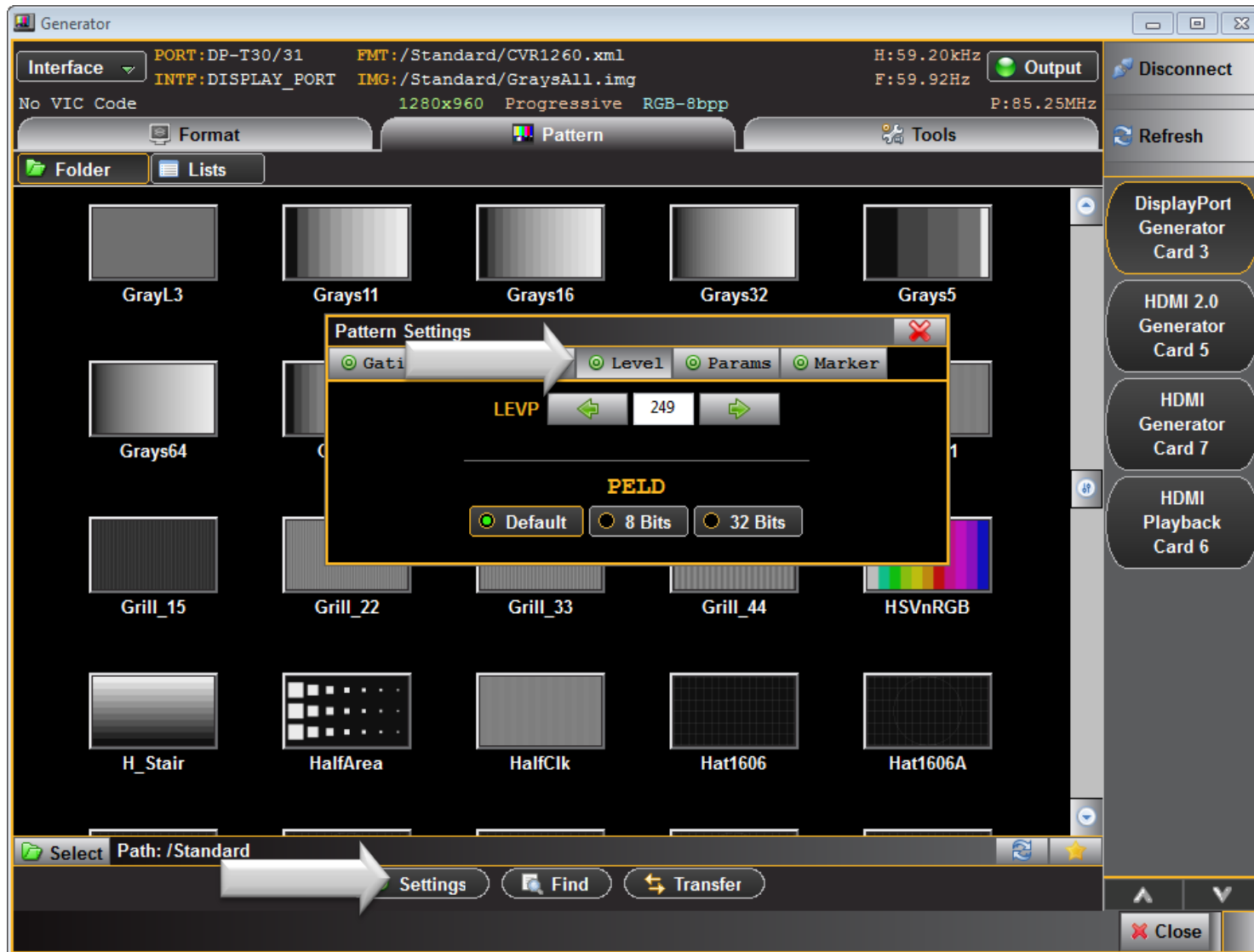
# 980 DP1.2 Video Generator Module – Pattern Testing



Configure pattern parameters:

- Some test patterns have variations. The Rendition tab enables you to test with any of these other “Renditions”.

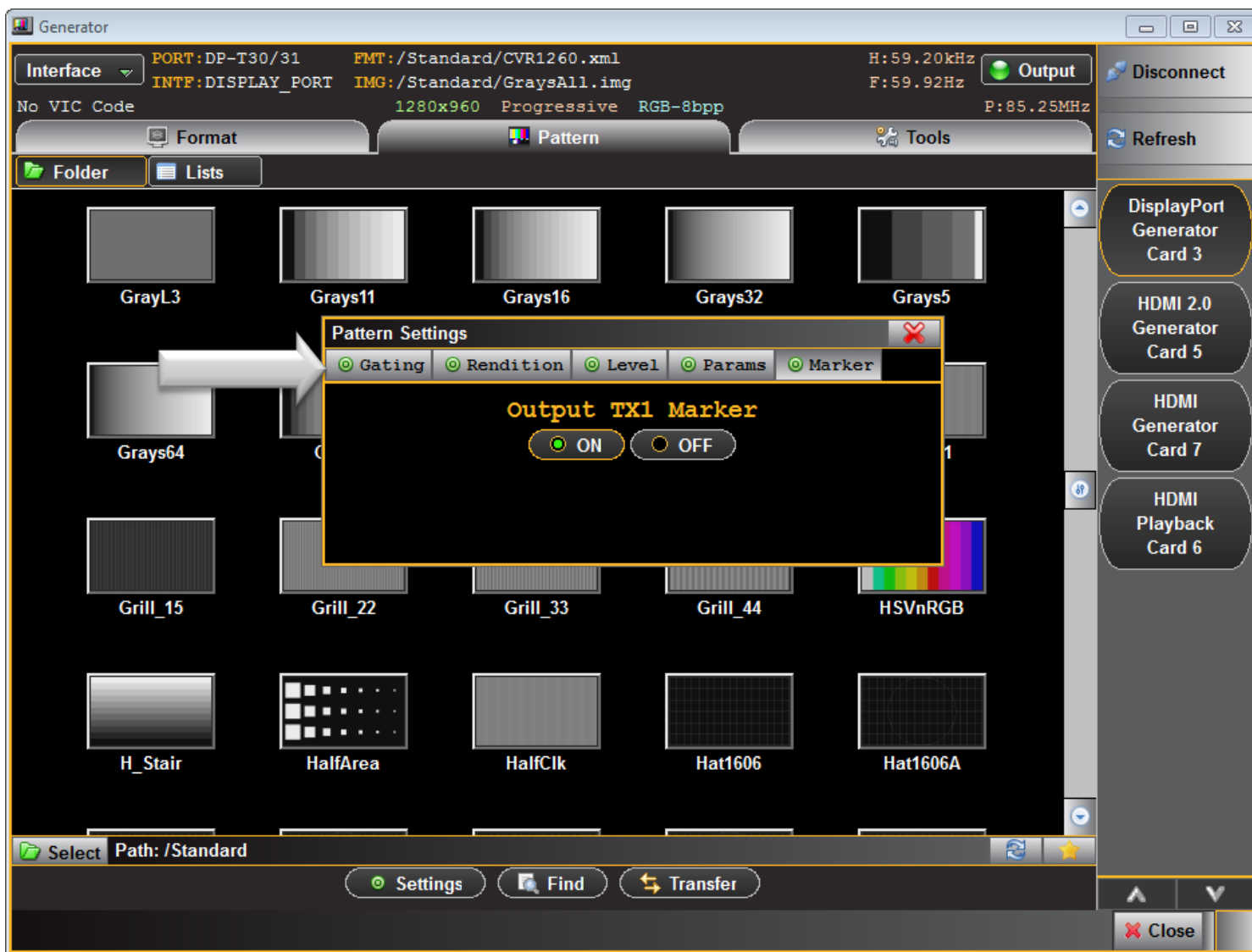
# 980 DP1.2 Video Generator Module – Pattern Testing



Configure pattern parameters:

- The Level tab enables you to set the luminance in IRE of the test pattern.

# 980 DP1.2 Video Generator Module – Pattern Testing

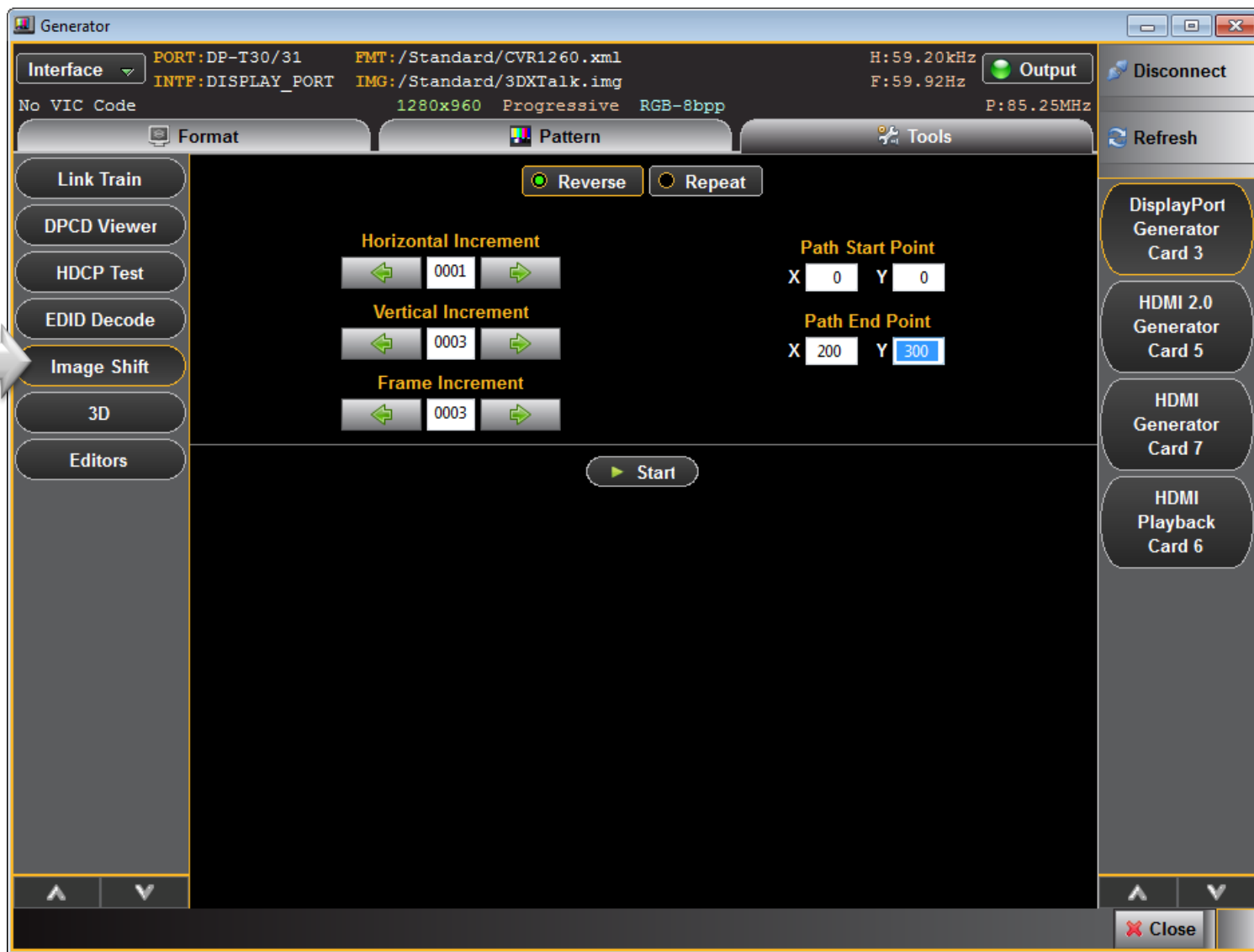


Configure pattern parameters:

- Put a marker on the Tx1 output so that you can distinguish which module Tx port is connected to.



# 980 DP1.2 Video Generator Module – Image Scrolling

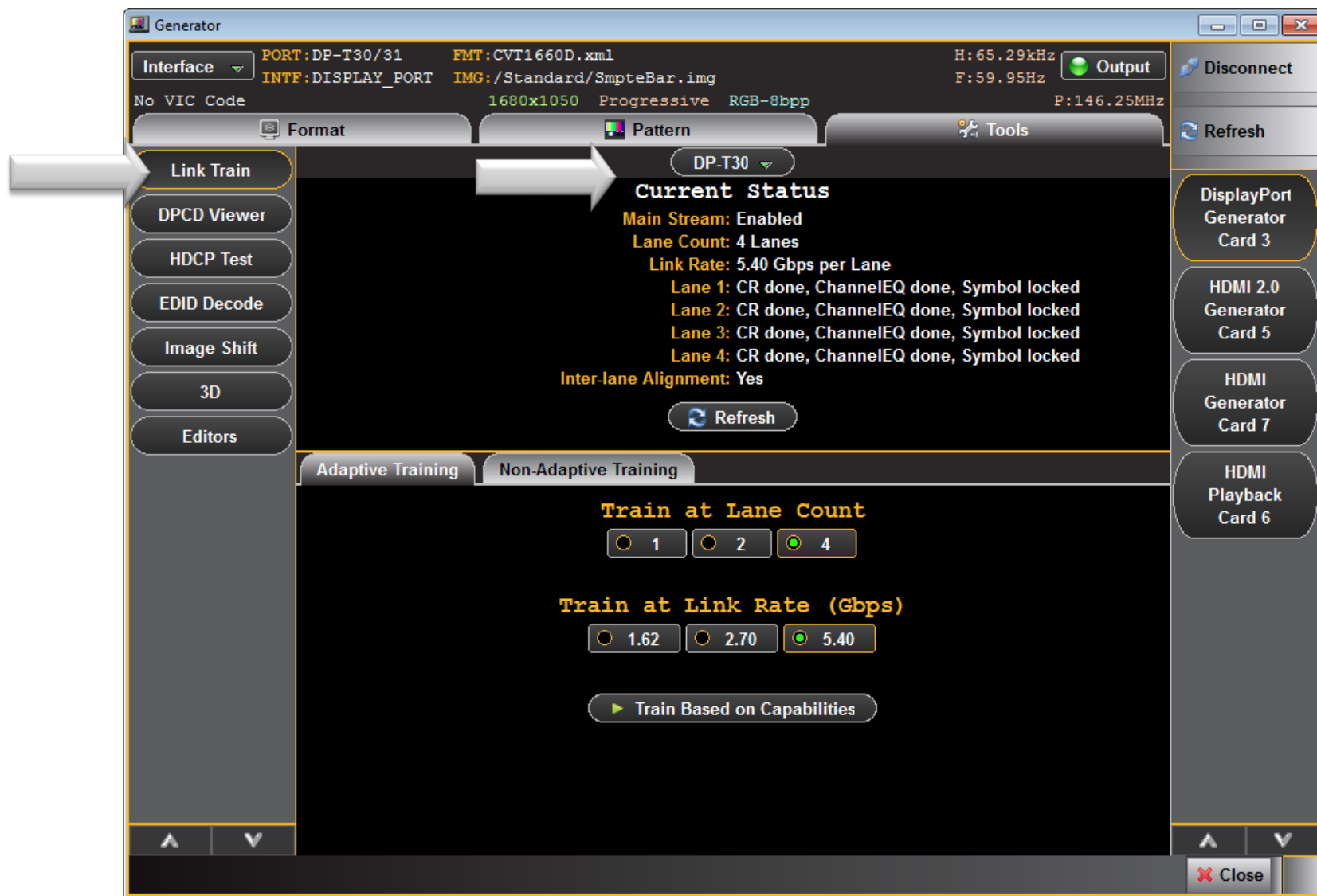


Scroll any test pattern with Image Scroll feature:

- Select scroll speed in horizontal and vertical axes.
- Select extent of travel.
- Select reverse or repeat scrolling.

# **980 DP1.2 Video Generator Module Configuring Link Training Parameters**

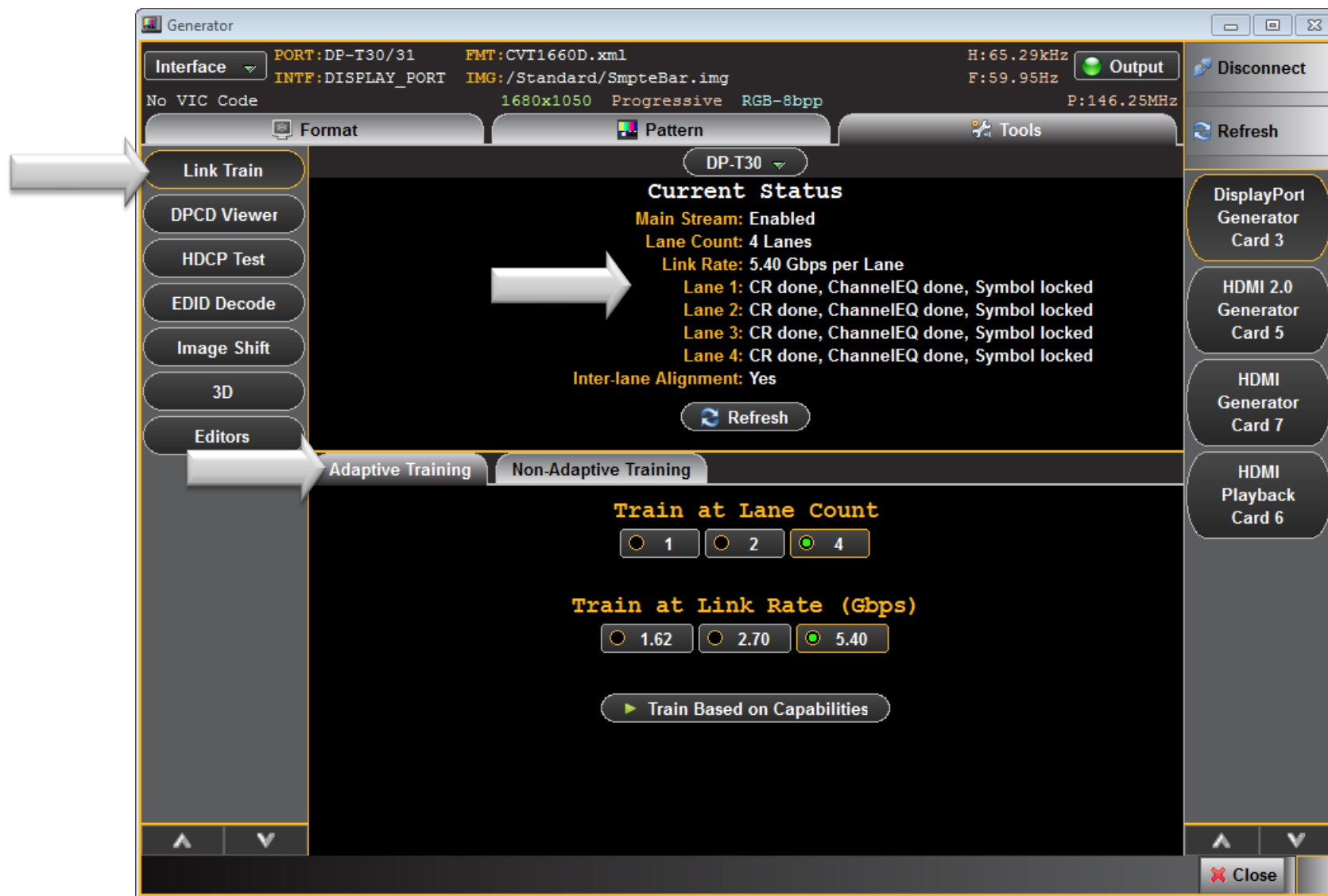
# 980 DP1.2 Video Generator – Configure Link Training



Select Link Train tool:

- Provides current status of link training on top panel.

# 980 DP1.2 Video Generator – Configure Link Training



Select Link Train tool:

- Select between Adaptive (automatic) link training and Non-Adaptive (shown in example).
- Set limits on source lane count and link rate capabilities.

# 980 DP1.2 Video Generator – Configure Link Training

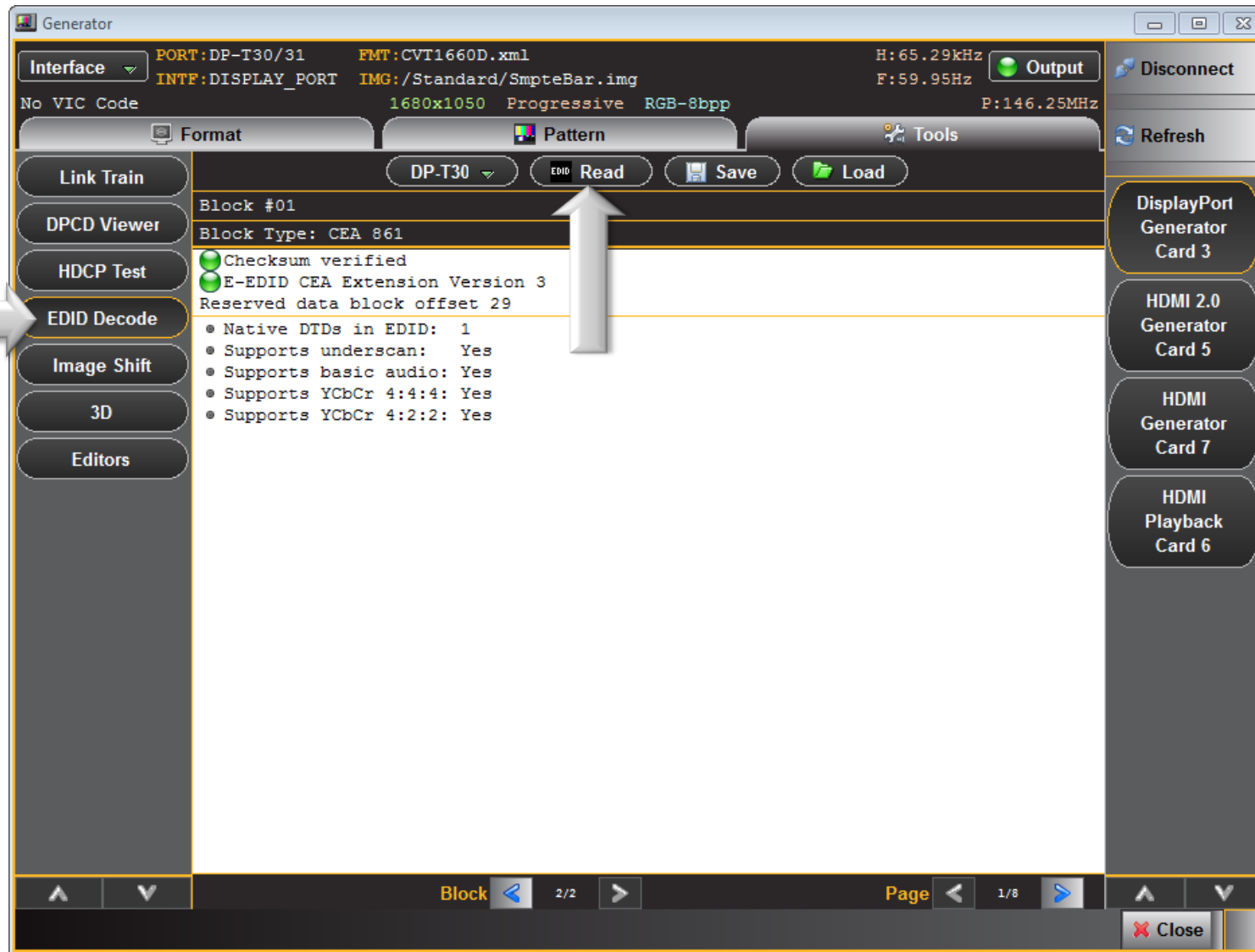
The screenshot displays the 'Generator' software interface. At the top, it shows interface settings: PORT: DP-T30/31, FMT: CVT1660D.xml, H: 65.29kHz, F: 59.95Hz, and a green 'Output' indicator. Below this, it lists 'No VIC Code', '1680x1050 Progressive RGB-8bpp', and 'P: 146.25MHz'. The main area is divided into 'Current Status' and 'Non-Adaptive Training' sections. The 'Current Status' section shows 'Main Stream: Enabled', 'Lane Count: 4 Lanes', 'Link Rate: 5.40 Gbps per Lane', and 'Inter-lane Alignment: Yes'. The 'Non-Adaptive Training' section allows configuration of 'Lane Count' (1, 2, 4), 'Link Rate (Gbps)' (1.62, 2.70, 5.40), 'Voltage Swing Level' (0, 1, 2, 3), and 'Pre-emphasis Level' (0, 1, 2, 3). A 'Force Train' button is located at the bottom of the configuration area. A sidebar on the left contains buttons for 'Link Train', 'DPCD Viewer', 'HDCP Test', 'EDID Decode', 'Image Shift', '3D', and 'Editors'. A sidebar on the right lists various video cards: 'DisplayPort Generator Card 3', 'HDMI 2.0 Generator Card 5', 'HDMI Generator Card 7', and 'HDMI Playback Card 6'. A 'Close' button is at the bottom right.

Select Link Train tool:

- Select between Adaptive (automatic – shown in example) link training and Non-Adaptive (user control).
- Enables precise control over lane count and link rate.

# 980 DP1.2 Video Generator Module Viewing EDIDs

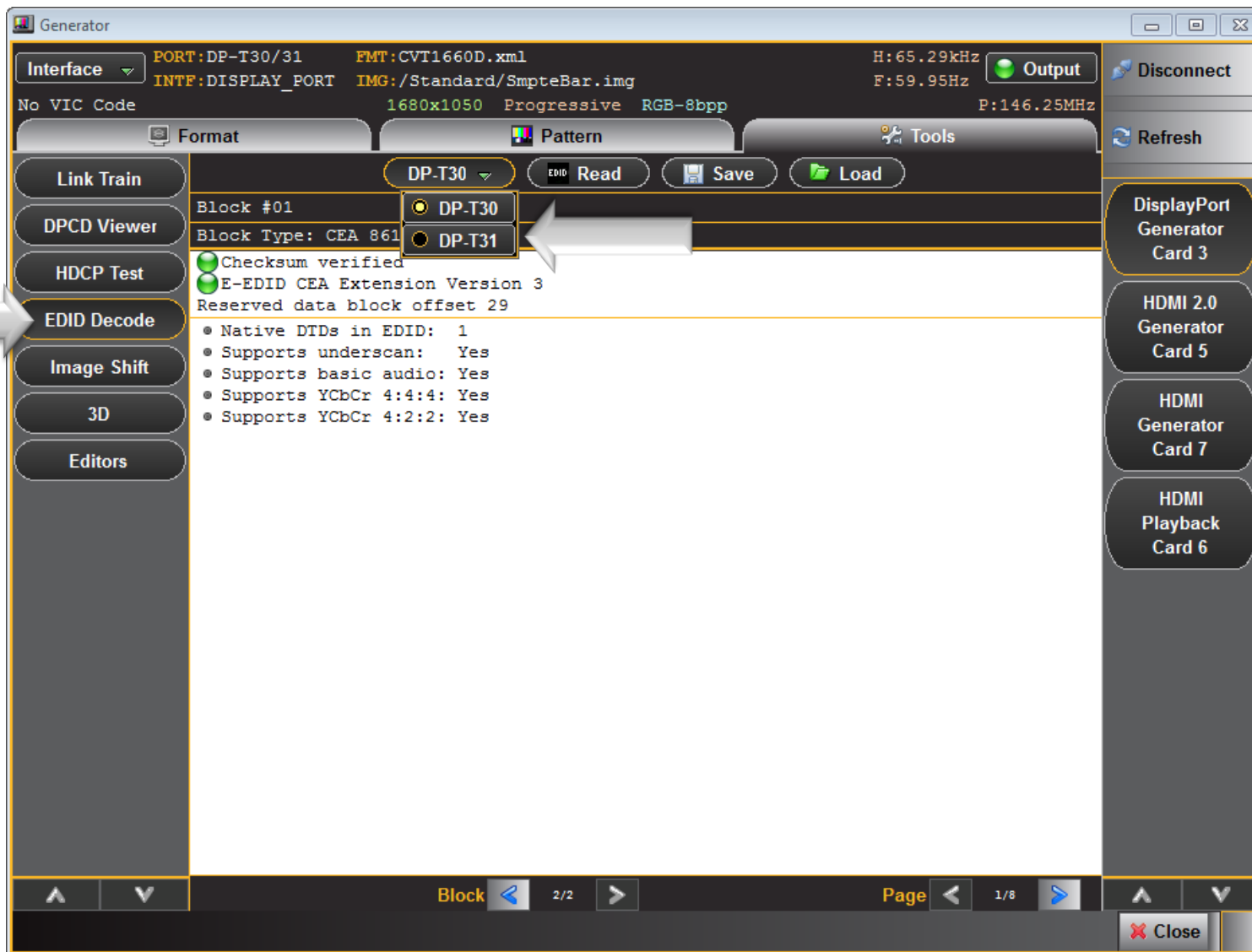
# 980 DP1.2 Video Generator Module – EDID Testing



View EDIDs – Select Interface:

- Select which Tx port to view EDID of connected display.

# 980 DP1.2 Video Generator Module – EDID Testing

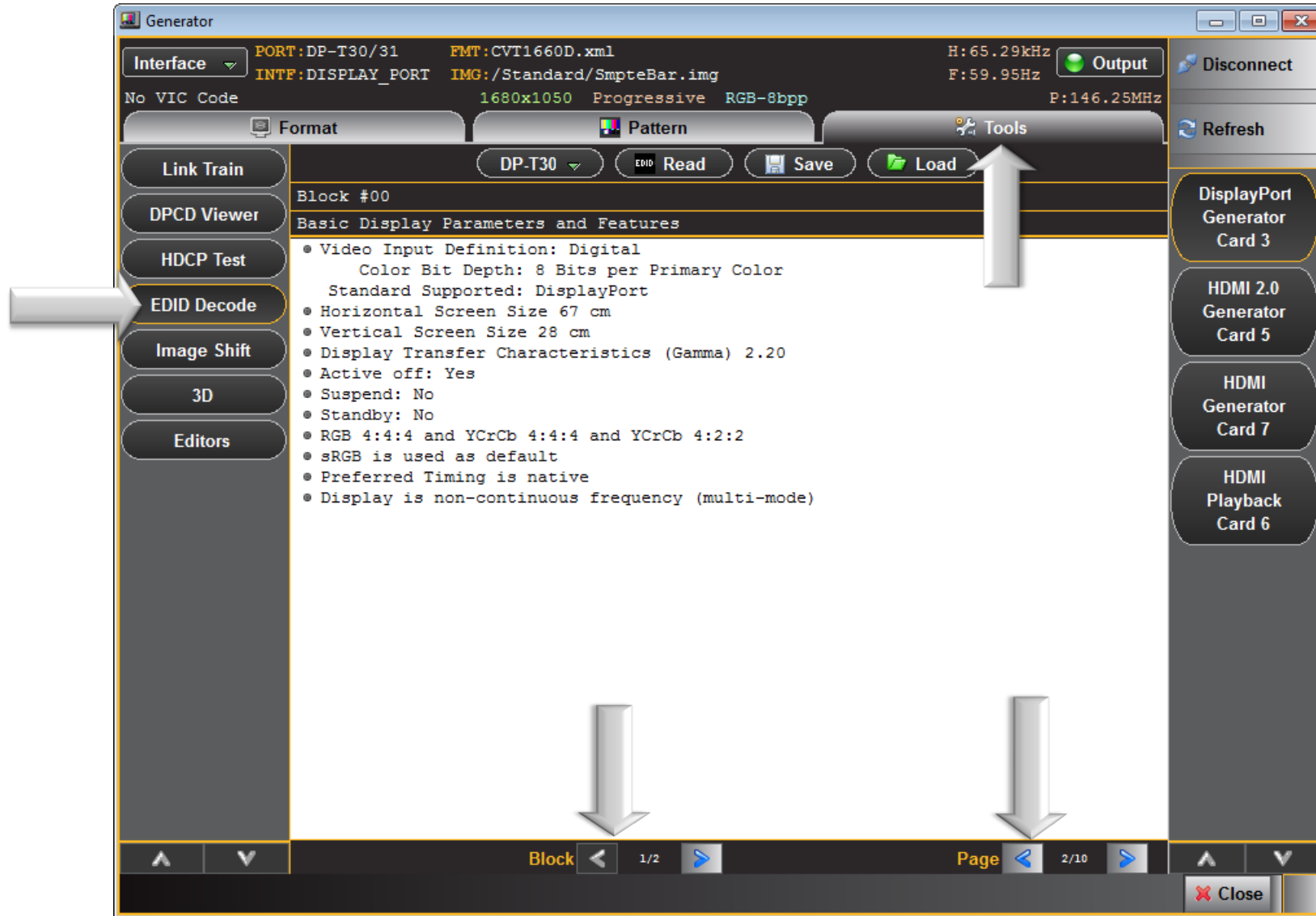


View EDIDs – Select Interface:

- Select which Tx port to view EDID of connected display.



# 980 DP1.2 Video Generator Module – EDID Testing



Decode and view EDIDs:

- View EDIDs of connected display in human readable text.
- Navigate through block 0 per page.
- Navigate through block 1 per page.

# 980 DP1.2 Video Generator Module – EDID Testing

The screenshot shows the 'Generator' software interface. The top status bar displays: PORT: DP-T30/31, FMT: CVT1660D.xml, H: 65.29kHz, Output (green dot), F: 59.95Hz, Refresh, Disconnect, and Format buttons. The main interface has tabs for Format, Pattern, and Tools. A left sidebar contains buttons for Link Train, DPCD Viewer, HDCP Test, EDID Decode (highlighted with a white arrow), Image Shift, 3D, and Editors. The central area shows 'Block #01' with 'CEA Data Block: Tag 2, bytes 16: Video Data' and 'Number of Descriptors: 16'. A list of 16 SVD descriptors is displayed, including resolution and refresh rate information. A right sidebar contains buttons for DisplayPort Generator Card 3, HDMI 2.0 Generator Card 5, HDMI Generator Card 7, and HDMI Playback Card 6. At the bottom, there are navigation controls for Block (2/2) and Page (2/8), and a Close button.

Decode and view EDIDs:

- View EDIDs of connected display in human readable text.
- Navigate through block 0 (1) per page.
- Navigate through block 1 (2) per page.

# 980 DP1.2 Video Generator Module – EDID Testing

The screenshot shows the 'Generator' software interface. The top status bar displays: PORT: DP-T30/31, FMT: CVT1660D.xml, H: 65.29kHz, Output, INTF: DISPLAY\_PORT, IMG: /Standard/SmpteBar.img, F: 59.95Hz, Disconnect, No VIC Code, 1680x1050 Progressive RGB-8bpp, P: 146.25MHz, Refresh. The main interface has three tabs: Format, Pattern, and Tools. The Tools tab is active, showing 'DP-T30' selected, 'EDID Read', 'Save', and 'Load' buttons. A grey arrow points to the 'Save' button. The left sidebar has buttons for Link Train, DPCD Viewer, HDCP Test, EDID Decode (highlighted with a grey arrow), Image Shift, 3D, and Editors. The main display area shows: Block #01, Block Type: CEA 861, Checksum verified, E-EDID CEA Extension Version 3, Reserved data block offset 29, and a list of capabilities: Native DTDs in EDID: 1, Supports underscan: Yes, Supports basic audio: Yes, Supports YCbCr 4:4:4: Yes, Supports YCbCr 4:2:2: Yes. The bottom status bar shows 'Block' 2/2 and 'Page' 1/8, with a 'Close' button.

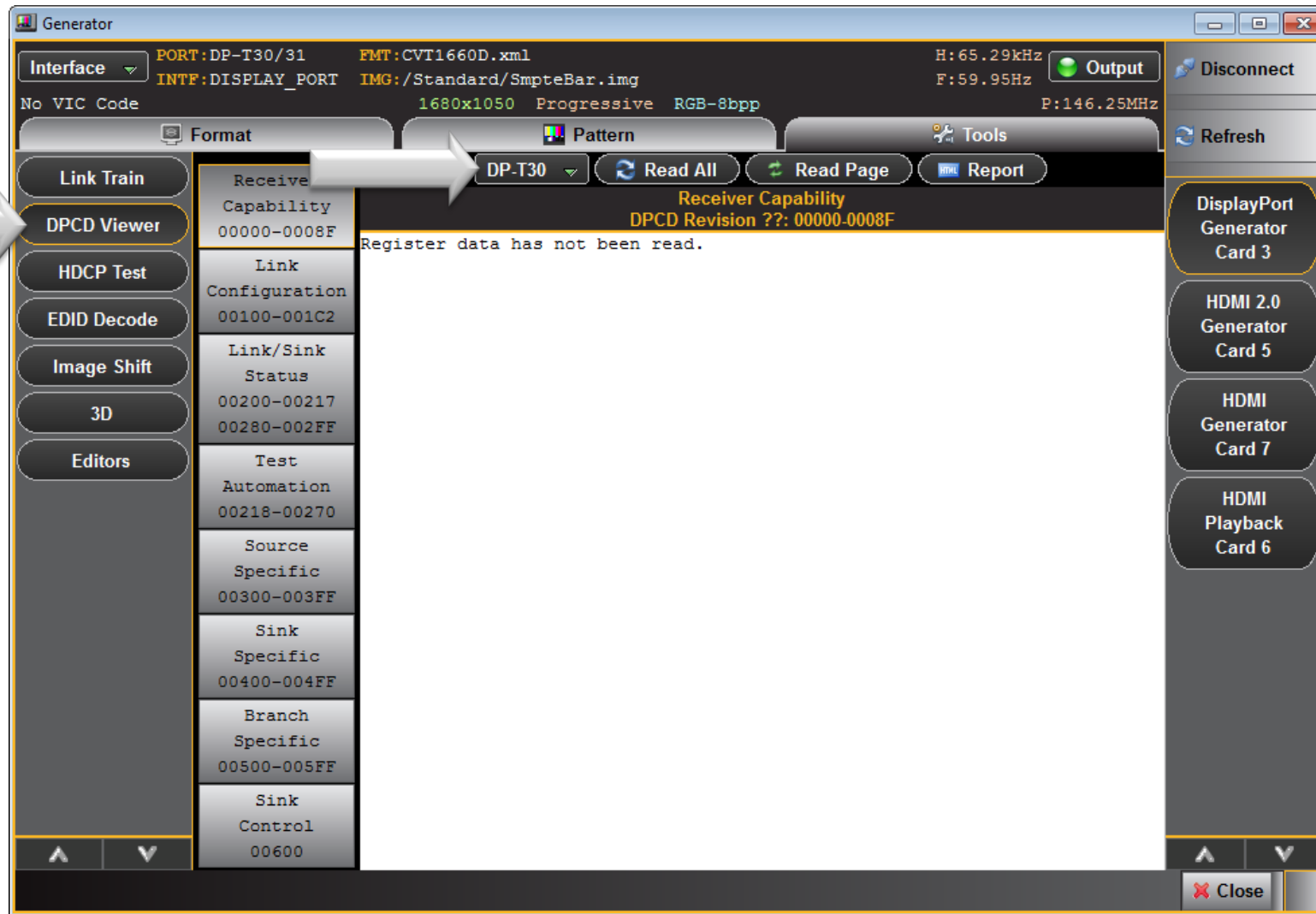
Decode and view EDIDs:

- View EDIDs of connected display in human readable text.
- Save EDIDs for emulation testing of sources.

# **980 DP1.2 Video Generator Module**

## **Viewing DPCD Registers**

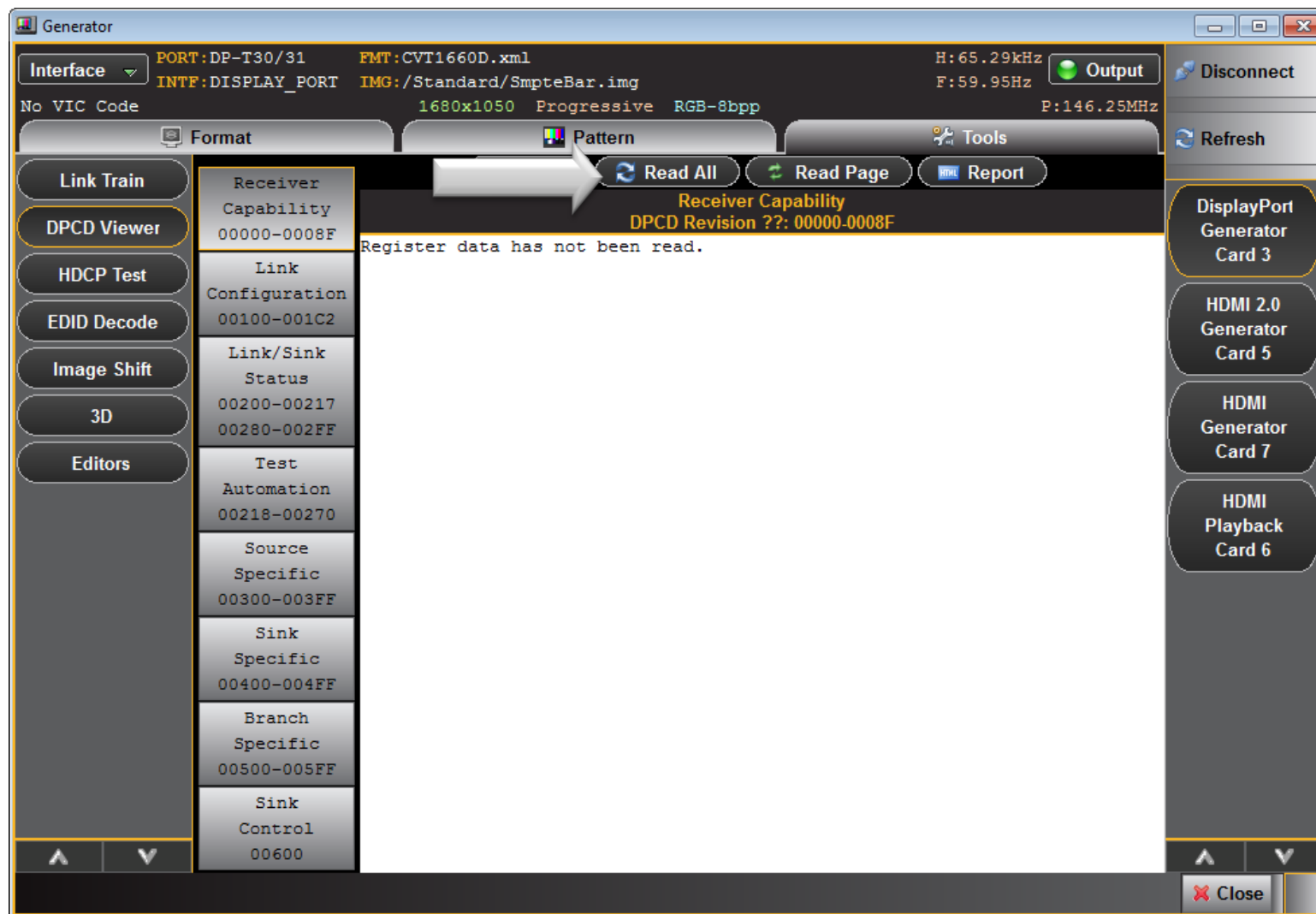
# 980 DP1.2 Video Generator Module – DPCD Testing



View DPCD Registers:

- Select DPCD Viewer.
- Select DP Tx port to view DPCD of connected display.

# 980 DP1.2 Video Generator Module – DPCD Testing



View DPCD Registers:

- Read either the entire DPCD or read each page.

# 980 DP1.2 Video Generator Module – DPCD Testing

Generator

Interface: PORT: DP-T30/31 FMT: CVT1660D.xml H: 65.29kHz Output  
INTF: DISPLAY\_PORT IMG: /Standard/SmpteBar.img F: 59.95Hz  
No VIC Code 1680x1050 Progressive RGB-8bpp P: 146.25MHz

Format Pattern Tools

DP-T30 Read All Read Page Report

Receiver Capability  
DPCD Revision 1.2: 00000-0008F

00000: DPCD\_REV

Bit	Name	Value	Description
7-4	MAJOR_REV	1	
3-0	MINOR_REV	2	

00001: MAX\_LINK\_RATE

Bit	Name	Value	Description
7-0	MAX_LINK_RATE	14h	5.4 Gbps per lane

00002: MAX\_LANE\_COUNT

Bit	Name	Value	Description
4-0	MAX_LANE_COUNT	4	4 lanes
5		1	Reserved
6	TPS3_SUPPORTED	Y(1)	
7	ENHANCED_FRAME_CAP	Y(1)	

00003: MAX\_DOWNSPREAD

Bit	Name	Value	Description
0	MAX_DOWNSPREAD	1	Up to 0.5%
1		0	Reserved
2		0	Reserved
3		0	Reserved
4		0	Reserved
5		0	Reserved
6	NO_AUX_HANDSHAKE_LINK_TRAINING	N(0)	
7		0	Reserved

View DPCD Registers:

- Reading Receiver Capability.

# 980 DP1.2 Video Generator Module – DPCD Testing

The screenshot shows the 'Generator' software interface. The top status bar displays: PORT: DP-T30/31, FMT: CVT1660D.xml, H: 65.29kHz, Output (green indicator), INTF: DISPLAY\_PORT, IMG: /Standard/SmpteBar.img, F: 59.95Hz, Disconnect, Refresh, and Format buttons. Below this, it shows 'No VIC Code', '1680x1050 Progressive RGB-8bpp', and 'P: 146.25MHz'. The main area is titled 'Link Configuration' and 'DPCD Revision 1.2: 00100-001C2'. A left sidebar contains buttons for Link Train, DPCD Viewer (highlighted), HDCP Test, EDID Decode, Image Shift, 3D, and Editors. The central display shows a table of DPCD registers with columns for Bit, Name, Value, and Description. A white arrow points to the 'Link Configuration' section of the table.

Bit	Name	Value	Description
00100: LINK_BW_SET			
7-0	LINK_BW_SET	14h	5.4 Gbps per lane
00101: LANE_COUNT_SET			
4-0	LANE_COUNT_SET	4	4 lanes
5		0	Reserved
6		0	Reserved
7	ENHANCED_FRAME_CAP	Y(1)	
00102: TRAINING_PATTERN_SET:			
1-0	TRAINING_PATTERN_SELECT	0	None
2		0	Reserved
3		0	Reserved
4	RECOVERED_CLOCK_OUT_EN	N(0)	
5	SCRAMBLING_DISABLE	N(0)	
7-6	SYMBOL_ERROR_COUNT_SEL	0	Disparity and Symbol e
00103: TRAINING_LANE0_SET			
1-0	VOLTAGE_SWING_SET	0	Level #
2	MAX_SWING_REACHED	N(0)	
4-3	PRE-EMPHASIS_SET	1	Level #
5	MAX_PRE-EMPHASIS_REACHED	N(0)	

View DPCD Registers:

- Read Link Configuration page.



# 980 DP1.2 Video Generator Module – DPCD Testing

The screenshot shows the 'Generator' software interface. The top status bar displays: Interface: DP-T30/31, FMT: CVT1660D.xml, H: 65.29kHz, Output: ON, INTF: DISPLAY\_PORT, IMG: /Standard/SmpteBar.img, F: 59.95Hz, Disconnected. The main area shows 'Link/Sink Status' for 'DPCD Revision 1.2: 00200-00217 00280-002FF'. The left sidebar contains buttons for Link Train, DPCD Viewer (selected), HDCP Test, EDID Decode, Image Shift, 3D, and ES. The right sidebar contains buttons for DisplayPort Generator Card 3, HDMI 2.0 Generator Card 5, HDMI Generator Card 7, and HDMI Playback Card 6. The main display shows the following register data:

```
00200: SINK_COUNT
  Bit Name Value Description
-----
  1 SINK_COUNT 1 Bits 7 + 5:0
  6 CP_READY N(0)

00201: DEVICE_SERVICE_IRQ_VECTOR
  Bit Name Value Description
-----
  0 REMOTE_CONTROL_COMMAND_PENDING N(0)
  1 AUTOMATED_TEST_REQUEST N(0)
  2 CP_IRQ N(0)
  3 MCCS_IRQ N(0)
  4 DOWN_REQ_MSG_RDY N(0)
  5 UP_REQ_MSG_RDY N(0)
  6 SINK_SPECIFIC_IRQ N(0)
  7 0 Reserved

00202: LANE0_1_STATUS:
  Bit Name Value Description
-----
  0 LANE0_CR_DONE Y(1)
  1 LANE0_CHANNEL_EQ_DONE Y(1)
  2 LANE0_SYMBOL_LOCKED Y(1)
  3 0 Reserved
  4 LANE1_CR_DONE Y(1)
  5 LANE1_CHANNEL_EQ_DONE Y(1)
  6 LANE1_SYMBOL_LOCKED Y(1)
  7 0 Reserved
```

View DPCD Registers:

- Read Link/Sink Status page.

# 980 DP1.2 Video Generator Module – DPCD Testing

The screenshot shows the 'Generator' software interface. The top status bar displays: Interface: DP-T30/31, FMT: CVT1660D.xml, H: 65.29kHz, Output (green dot), Disconnect; INTF: DISPLAY\_PORT, IMG: /Standard/SmpteBar.img, F: 59.95Hz, Refresh; No VIC Code, 1680x1050 Progressive RGB-8bpp, P: 146.25MHz. The main area is titled 'Test Automation DPCD Revision 1.2: 00218-00270'. It shows three registers:

- 00218: TEST\_REQUEST
- 00219: TEST\_LINK\_RATE
- 00220: TEST\_LANE\_COUNT
- 00221: TEST\_PATTERN

Bit	Name	Value	Description
0	TEST_LINK_TRAINING	N(0)	
1	TEST_PATTERN	N(0)	
2	TEST_EDID_READ	N(0)	
3	PHY_TEST_PATTERN	N(0)	
4	FAUX_TEST_PATTERN	N(0)	
5		0	Reserved
6		0	Reserved
7		0	Reserved

Bit	Name	Value	Description
7-0	TEST_LINK_RATE	00h	Reserved

Bit	Name	Value	Description
4-0	TEST_LANE_COUNT	0	Reserved
5		0	Reserved
6		0	Reserved
7		0	Reserved

Bit	Name	Value	Description
7-0	Requested Pattern	0	None

View DPCD Registers:

- Read Test Automation page.

# 980 DP1.2 Video Generator Module – DPCD Testing

The screenshot shows the 'Generator' software interface. At the top, it displays configuration details: Interface (DP-T30/31), FMT (CVT1660D.xml), H (65.29kHz), F (59.95Hz), and Output status. Below this are tabs for Format, Pattern, and Tools. The 'DPCD Viewer' tab is selected, showing a list of registers on the left and their details in the main window. A white arrow points to the 'Source Specific' register category.

**Source Specific DPCD Registers:**

Register	Value	Description												
00300: SRC_IEEE_OUI	OUI: 000000h (0)													
00303: SRC_DEVICE_ID_STRING	Bytes: 00 00 00 00 00 00 ASCII: ""													
00309: SRC_HARDWARE_REVISION														
<table border="1"><thead><tr><th>Bit</th><th>Name</th><th>Value</th><th>Description</th></tr></thead><tbody><tr><td>3-0</td><td>Minor Revision</td><td>0</td><td></td></tr><tr><td>7-4</td><td>Major Revision</td><td>0</td><td></td></tr></tbody></table>			Bit	Name	Value	Description	3-0	Minor Revision	0		7-4	Major Revision	0	
Bit	Name	Value	Description											
3-0	Minor Revision	0												
7-4	Major Revision	0												
0030A: SRC_FW_SW_MAJOR_REV	Value = 00h (0)													
0030B: SRC_FW_SW_MINOR_REV	Value = 00h (0)													
0030C: SRC_VENDOR_SPECIFIC(0)	[030C][00 00 00 00 00 00 00 00][.....]													
	[0314][00 00 00 00 00 00 00 00][.....]													
	[031C][00 00 00 00 00 00 00 00][.....]													
	[0324][00 00 00 00 00 00 00 00][.....]													
	[032C][00 00 00 00 00 00 00 00][.....]													
	[0334][00 00 00 00 00 00 00 00][.....]													
	[033C][00 00 00 00 00 00 00 00][.....]													
	[0344][00 00 00 00 00 00 00 00][.....]													
	[034C][00 00 00 00 00 00 00 00][.....]													
	[0354][00 00 00 00 00 00 00 00][.....]													

View DPCD Registers:

- Read Source Specific page.

# 980 DP1.2 Video Generator Module – DPCD Testing

The screenshot shows the 'Generator' software interface. The top status bar displays: Interface: DP-T30/31, FMT: CVT1660D.xml, H: 65.29kHz, Output (green dot), Disconnect; INTF: DISPLAY\_PORT, IMG: /Standard/SmpteBar.img, F: 59.95Hz, Refresh; No VIC Code, 1680x1050 Progressive RGB-8bpp, P: 146.25MHz. The main window is titled 'Sink Specific DPCD Revision 1.2: 00400-004FF'. The left sidebar has a 'DPCD Viewer' button highlighted, and a white arrow points to the 'Sink Specific 00400-004FF' register selection. The main display shows the following DPCD registers:

```
00400: SINK_IEEE_OUI
OUI: 0080E1h (32993)
00403: SINK_DEVICE_ID_STRING
Bytes: 44 70 31 2E 32 00
ASCII: "Dp1.2"
00409: SINK_HARDWARE_REVISION
Bit Name Value Description
-----
3-0 Minor Revision 0
7-4 Major Revision 0
0040A: SINK_FW_SW_MAJOR_REV
Value = 00h (0)
0040B: SINK_FW_SW_MINOR_REV
Value = 00h (0)
0040C: SINK_VENDOR_SPECIFIC(0)
[040C] [00 00 02 01 00 80 E1 44] [.....D]
[0414] [70 31 2E 32 00 00 00 00] [p1.2....]
[041C] [00 00 02 01 00 80 E1 44] [.....D]
[0424] [70 31 2E 32 00 00 00 00] [p1.2....]
[042C] [00 00 02 01 00 80 E1 44] [.....D]
[0434] [70 31 2E 32 00 00 00 00] [p1.2....]
[043C] [00 00 02 01 00 80 E1 44] [.....D]
[0444] [70 31 2E 32 00 00 00 00] [p1.2....]
[044C] [00 00 02 01 00 80 E1 44] [.....D]
[0454] [70 31 2E 32 00 00 00 00] [p1.2....]
```

View DPCD Registers:

- Read Sink Specific page.

# 980 DP1.2 Video Generator Module – DPCD Testing

The screenshot shows the 'Generator' software interface. The top status bar displays: PORT: DP-T30/31, FMT: CVT1660D.xml, H: 65.29kHz, INTF: DISPLAY\_PORT, IMG: /Standard/SmpteBar.img, F: 59.95Hz, and an 'Output' button. Below this, it shows 'No VIC Code', '1680x1050 Progressive RGB-8bpp', and 'P: 146.25MHz'. The main interface has a left sidebar with buttons for 'Link Train', 'DPCD Viewer', 'HDCP Test', 'EDID Decode', 'Image Shift', '3D', and 'Editors'. The 'DPCD Viewer' is active, showing a tree view of DPCD registers. The 'Sink Control' register (00600) is selected, and its details are shown in the main window. The details include a table for 'Sink Control DPCD Revision 1.2' and a 'Read All' button. A white arrow points to the 'Sink Control' register in the tree view.

Interface: DP-T30/31, FMT: CVT1660D.xml, H: 65.29kHz, INTF: DISPLAY\_PORT, IMG: /Standard/SmpteBar.img, F: 59.95Hz, Output

No VIC Code, 1680x1050 Progressive RGB-8bpp, P: 146.25MHz

Format, Pattern, Tools

DP-T30, Read All, Read Page, Report

Sink Control DPCD Revision 1.2

Bit	Name	Value	Description
2-0	SET_POWER_STATE	1	D0, FAUX Power State 1 or
3		0	Reserved
4		0	Reserved
5		0	Reserved
6		0	Reserved
7		0	Reserved

00600: SINK\_SET\_POWER

Receiver Capability 00000-0008F

Link Configuration 00100-001C2

Link/Sink Status 00200-00217, 00280-002FF

Test Automation 00218-00270

Source Specific 00300-003FF

Sink Specific 00400-004FF

Branch Specific 00500-005FF

Sink Control 00600

ESI

DisplayPort Generator Card 3, HDMI 2.0 Generator Card 5, HDMI Generator Card 7, HDMI Playback Card 6

Close

View DPCD Registers:

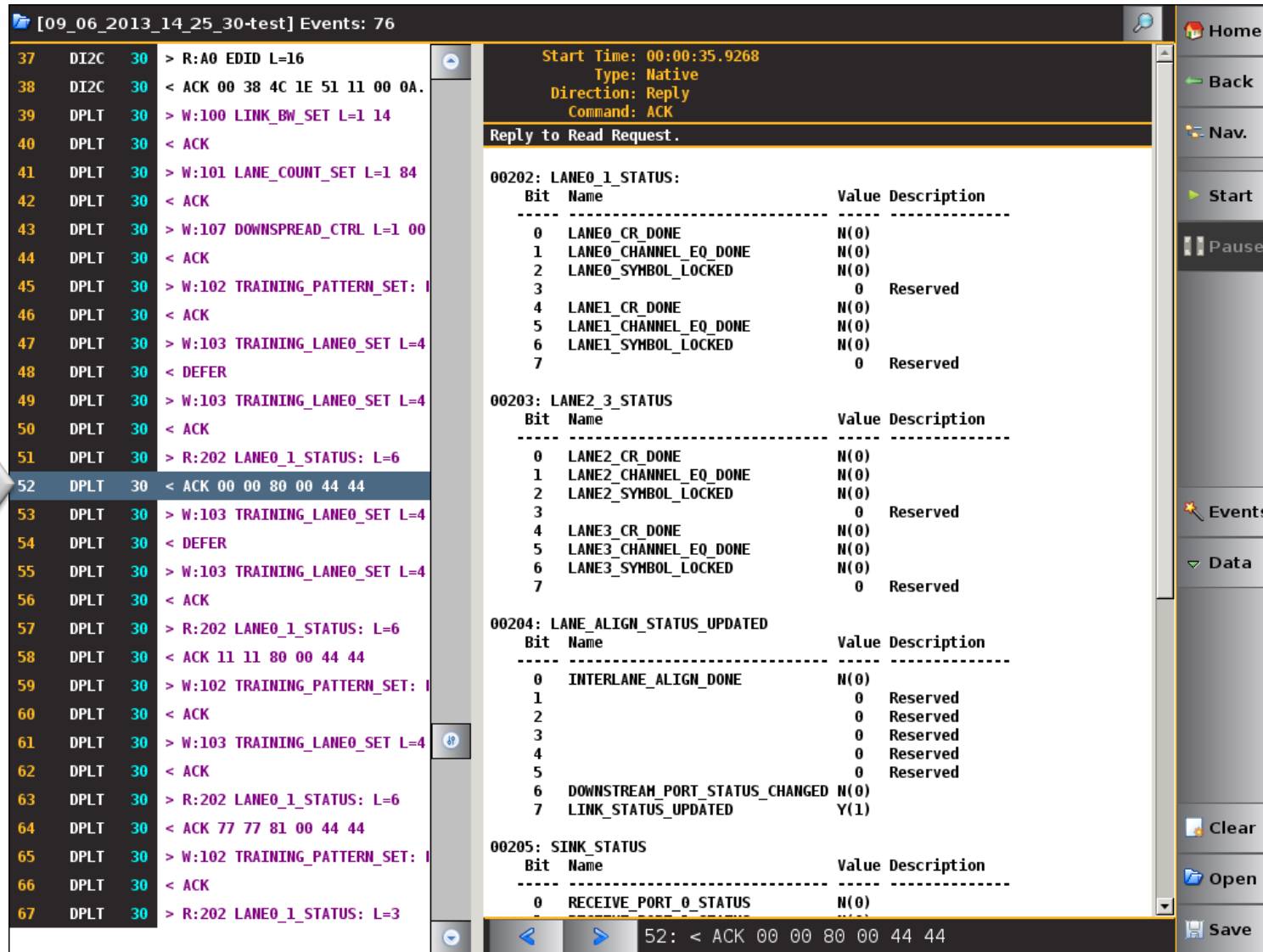
- Read Sink Control page.

# **980 DP1.2 Video Generator Module Monitoring Aux Channel Transactions**

# 980 DP1.2 Video Generator - Auxiliary Channel Analyzer

- Monitor Aux Channel transactions (Link Training, DPCD exchanges, HDCP and EDID) through Auxiliary Channel Analyzer (ACA).
- 980 Video Generator module emulates DP1.2 source and monitors DPCD exchanges, Link Training transactions, HDCP authentication transactions and EDID exchanges.

# 980 DP1.2 Video Generator Module – Monitor Link Training



[09\_06\_2013\_14\_25\_30-test] Events: 76

37 DI2C 30 > R:A0 EDID L=16  
38 DI2C 30 < ACK 00 38 4C 1E 51 11 00 0A.  
39 DPLT 30 > W:100 LINK\_BW\_SET L=1 14  
40 DPLT 30 < ACK  
41 DPLT 30 > W:101 LANE\_COUNT\_SET L=1 84  
42 DPLT 30 < ACK  
43 DPLT 30 > W:107 DOWNSPREAD\_CTRL L=1 00  
44 DPLT 30 < ACK  
45 DPLT 30 > W:102 TRAINING\_PATTERN\_SET: I  
46 DPLT 30 < ACK  
47 DPLT 30 > W:103 TRAINING\_LANE0\_SET L=4  
48 DPLT 30 < DEFER  
49 DPLT 30 > W:103 TRAINING\_LANE0\_SET L=4  
50 DPLT 30 < ACK  
51 DPLT 30 > R:202 LANE0\_1\_STATUS: L=6  
52 DPLT 30 < ACK 00 00 80 00 44 44  
53 DPLT 30 > W:103 TRAINING\_LANE0\_SET L=4  
54 DPLT 30 < DEFER  
55 DPLT 30 > W:103 TRAINING\_LANE0\_SET L=4  
56 DPLT 30 < ACK  
57 DPLT 30 > R:202 LANE0\_1\_STATUS: L=6  
58 DPLT 30 < ACK 11 11 80 00 44 44  
59 DPLT 30 > W:102 TRAINING\_PATTERN\_SET: I  
60 DPLT 30 < ACK  
61 DPLT 30 > W:103 TRAINING\_LANE0\_SET L=4  
62 DPLT 30 < ACK  
63 DPLT 30 > R:202 LANE0\_1\_STATUS: L=6  
64 DPLT 30 < ACK 77 77 81 00 44 44  
65 DPLT 30 > W:102 TRAINING\_PATTERN\_SET: I  
66 DPLT 30 < ACK  
67 DPLT 30 > R:202 LANE0\_1\_STATUS: L=3

Start Time: 00:00:35.9268  
Type: Native  
Direction: Reply  
Command: ACK  
Reply to Read Request.

00202: LANE0\_1\_STATUS:

Bit	Name	Value	Description
0	LANE0_CR_DONE	N(0)	
1	LANE0_CHANNEL_EQ_DONE	N(0)	
2	LANE0_SYMBOL_LOCKED	N(0)	
3		0	Reserved
4	LANE1_CR_DONE	N(0)	
5	LANE1_CHANNEL_EQ_DONE	N(0)	
6	LANE1_SYMBOL_LOCKED	N(0)	
7		0	Reserved

00203: LANE2\_3\_STATUS

Bit	Name	Value	Description
0	LANE2_CR_DONE	N(0)	
1	LANE2_CHANNEL_EQ_DONE	N(0)	
2	LANE2_SYMBOL_LOCKED	N(0)	
3		0	Reserved
4	LANE3_CR_DONE	N(0)	
5	LANE3_CHANNEL_EQ_DONE	N(0)	
6	LANE3_SYMBOL_LOCKED	N(0)	
7		0	Reserved

00204: LANE\_ALIGN\_STATUS\_UPDATED

Bit	Name	Value	Description
0	INTERLANE_ALIGN_DONE	N(0)	
1		0	Reserved
2		0	Reserved
3		0	Reserved
4		0	Reserved
5		0	Reserved
6	DOWNSTREAM_PORT_STATUS_CHANGED	N(0)	
7	LINK_STATUS_UPDATED	Y(1)	

00205: SINK\_STATUS

Bit	Name	Value	Description
0	RECEIVE_PORT_0_STATUS	N(0)	

52: < ACK 00 00 80 00 44 44

View Aux Chan Link Training transactions:

- Select Specific record to view details.



# 980 DP1.2 Video Generator Module – Monitor Link Training

[-] Events: 38497, Pending: 0

38467 DPLT 10 > W:102 TRAINING\_PATTERN\_SET: L=1 22  
38468 DPPRE 10 Precharge/Sync Count: 26  
38469 DPLT 10 < ACK  
38470 DPPRE 10 Precharge/Sync Count: 32  
38471 DPLT 10 > W:103 TRAINING\_LANE0\_SET L=4 00 00 00 00  
38472 DPPRE 10 Precharge/Sync Count: 26  
38473 DPLT 10 < ACK  
38474 DPPRE 10 Precharge/Sync Count: 32  
38475 DPLT 10 > R:202 LANE0\_1\_STATUS: L=6  
38476 DPPRE 10 Precharge/Sync Count: 26  
38477 DPLT 10 < ACK 77 77 01 01 00 00  
38478 DPPRE 10 Precharge/Sync Count: 32  
38479 DPLT 10 > W:102 TRAINING\_PATTERN\_SET: L=1 00  
38480 DPPRE 10 Precharge/Sync Count: 26  
38481 DPLT 10 < ACK  
38482 DPPRE 10 Precharge/Sync Count: 32  
38483 DPLT 10 > R:202 LANE0\_1\_STATUS: L=3  
38484 DPPRE 10 Precharge/Sync Count: 26  
38485 DPLT 10 < ACK 77 77 01  
38486 DPPRE 10 Precharge/Sync Count: 32  
38487 DNAT 10 > R:200 SINK\_COUNT L=8  
38488 DPPRE 10 Precharge/Sync Count: 26  
38489 DNAT 10 < ACK 41 00 77 77 01 03 00 00  
38490 DPPRE 10 Precharge/Sync Count: 32  
38491 DPLT 10 > R:100 LINK\_BW\_SET L=8  
38492 DPPRE 10 Precharge/Sync Count: 26  
**38493 DPLT 10 < ACK 0A 84 00 00 00 00 00 00**  
38494 DPPRE 10 Precharge/Sync Count: 32  
38495 DNAT 10 > R:200 SINK\_COUNT L=8  
38496 DPPRE 10 Precharge/Sync Count: 26  
38497 DNAT 10 < ACK 41 00 77 77 01 03 00 00

Start Time: 05:28:22.9635  
Type: Native  
Direction: Reply  
Command: ACK  
Reply to Read Request.

00100: LINK\_BW\_SET

Bit	Name	Value	Description
7-0	LINK_BW_SET	0Ah	2.7 Gbps per L

00101: LANE\_COUNT\_SET

Bit	Name	Value	Description
4-0	LANE_COUNT_SET	4	4 lanes
5		0	Reserved
6		0	Reserved
7	ENHANCED_FRAME_CAP	Y(1)	

00102: TRAINING\_PATTERN\_SET:

Bit	Name	Value	Description
1-0	TRAINING_PATTERN_SELECT	0	None
2		0	Reserved
3		0	Reserved
4	RECOVERED_CLOCK_OUT_EN	N(0)	
5	SCRAMBLING_DISABLE	N(0)	
7-6	SYMBOL_ERROR_COUNT_SEL	0	Disparity and

00103: TRAINING\_LANE0\_SET

Bit	Name	Value	Description
1-0	VOLTAGE_SWING_SET	0	Level #
2	MAX_SWING_REACHED	N(0)	
4-3	PRE-EMPHASIS_SET	0	Level #
5	MAX_PRE-EMPHASIS_REACHED	N(0)	
6		0	Reserved
7		0	Reserved

00104: TRAINING\_LANE1\_SET

Bit	Name	Value	Description
1-0	VOLTAGE_SWING_SET	0	Level #
2	MAX_SWING_REACHED	N(0)	
4-3	PRE-EMPHASIS_SET	0	Level #

38493: < ACK 0A 84 00 00 00 00 00 00

View Aux Chan Link Training transactions:

- Select Specific record to view details.

# 980 DP1.2 Video Generator Module – Monitor Link Training

Start Time: 05:28:22.9676  
Type: Native  
Direction: Reply  
Command: ACK  
Reply to Read Request.

Bit	Name	Value	Description
6	SINK_COUNT	1	Bits 7 + 5:0
6	CP_READY	Y(1)	

Bit	Name	Value	Description
0	REMOTE_CONTROL_COMMAND_PENDING	N(0)	
1	AUTOMATED_TEST_REQUEST	N(0)	
2	CP_IRQ	N(0)	
3	HCCS_IRQ	N(0)	
4	DOWN_REP_MSG_RDY	N(0)	
5	UP_REQ_MSG_RDY	N(0)	
6	SINK_SPECIFIC_IRQ	N(0)	
7		0	Reserved

Bit	Name	Value	Description
0	LANE0_CR_DONE	Y(1)	
1	LANE0_CHANNEL_EQ_DONE	Y(1)	
2	LANE0_SYMBOL_LOCKED	Y(1)	
3		0	Reserved
4	LANE1_CR_DONE	Y(1)	
5	LANE1_CHANNEL_EQ_DONE	Y(1)	
6	LANE1_SYMBOL_LOCKED	Y(1)	
7		0	Reserved

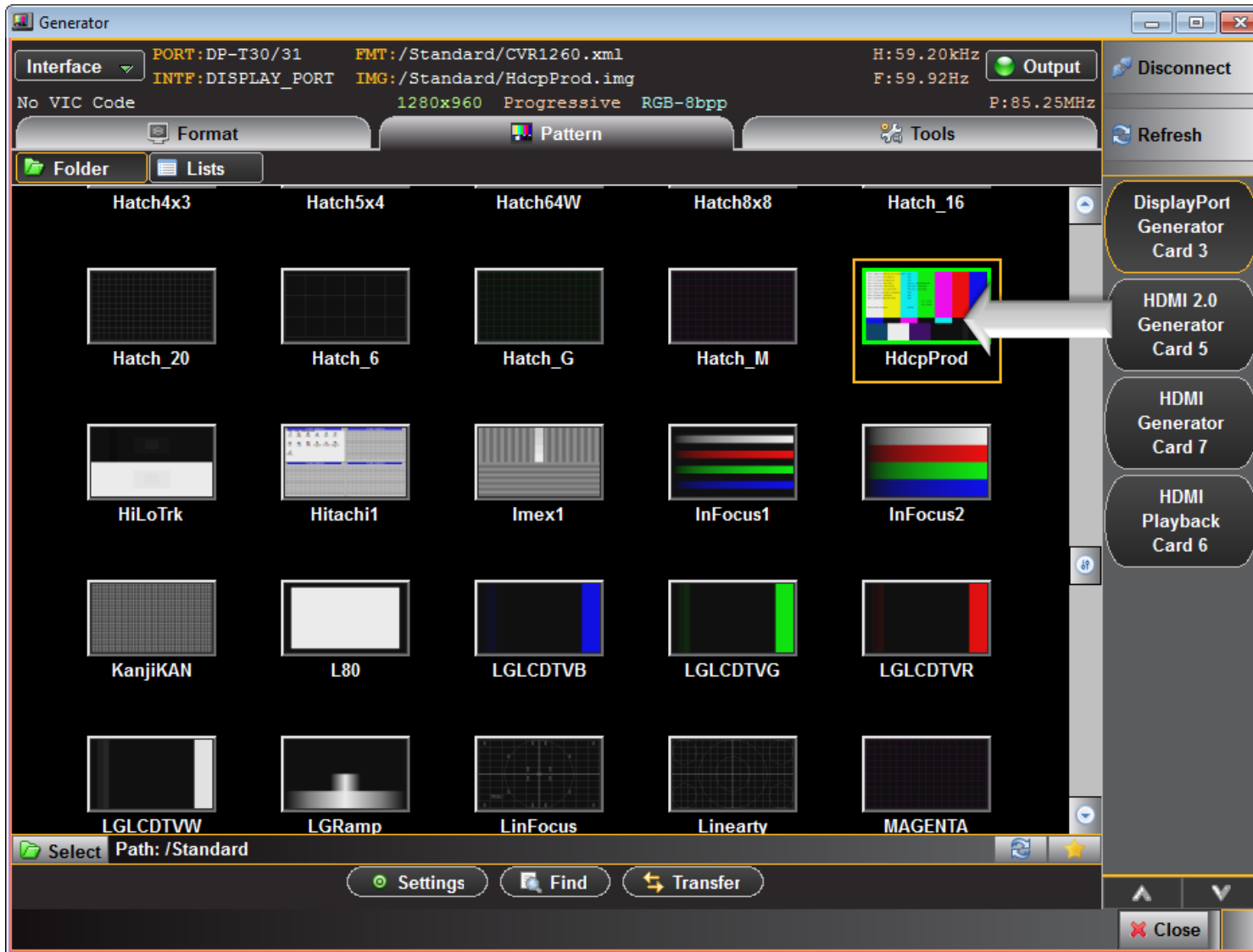
  

Bit	Name	Value	Description
0	LANE2_CR_DONE	Y(1)	
1	LANE2_CHANNEL_EQ_DONE	Y(1)	
2	LANE2_SYMBOL_LOCKED	Y(1)	
3		0	Reserved
4	LANE3_CR_DONE	Y(1)	
5	LANE3_CHANNEL_EQ_DONE	Y(1)	
6	LANE3_SYMBOL_LOCKED	Y(1)	

View Aux Chan Link Training transactions:

- Select Specific record to view details.

# 980 DP Video Generator Module – HDCP Testing



Select test images for DP protocols:

- Select HDCPProd test image.

# 980 DP Video Generator - Auxiliary Channel Analyzer

The screenshot displays the ACA Remote Control software interface. On the left, a list of events is shown, with event 68 selected and highlighted by a white arrow. The event details for event 68 are shown in the main window:

```
Start Time: 00:53:21.1498
Type: Native
Direction: Reply
Command: ACK
Reply to Read Request.
```

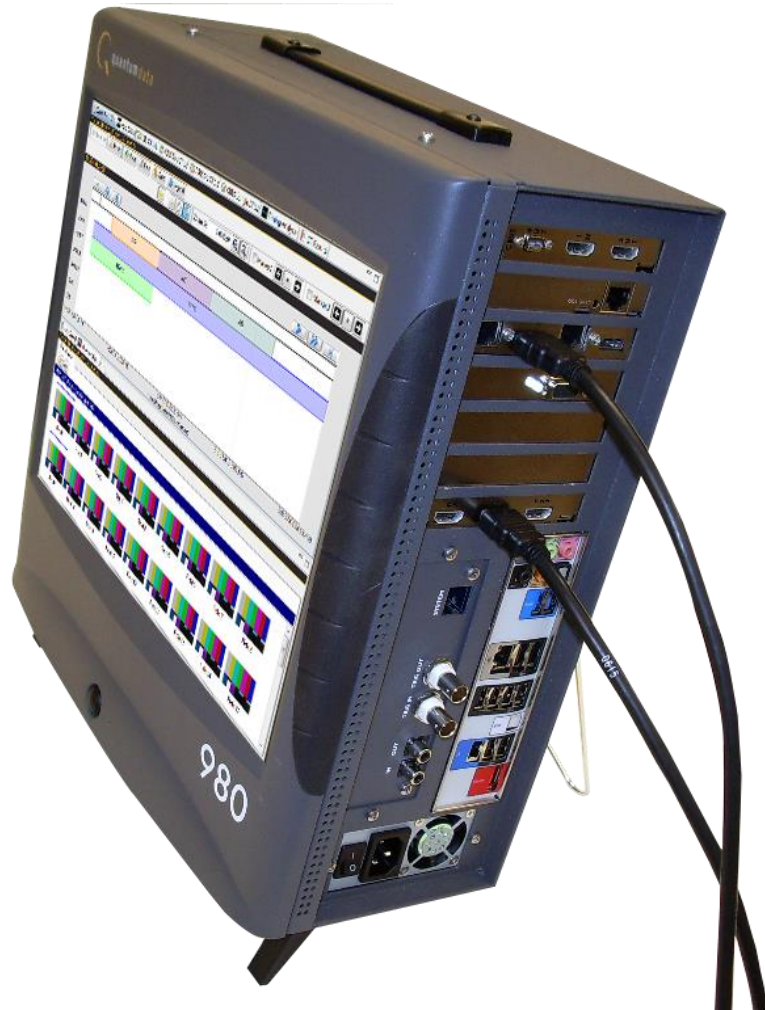
Bit	Name	Value	Description
0	HDCP_CAPABLE	Y(1)	
1	REPEATER_HDCP	Y(1)	
2		0	Reserved
3		0	Reserved
4		0	Reserved
5		0	Reserved
6		0	Reserved
7		0	Reserved

Raw Data:  
[0000][00 03 -- -- -- -- --][.. ]

Monitoring DDC Transactions with HDMI sink device:

- Show details of selected item in human text.

# Quantum Data 980 Video Test Generation Module



**... 980 now supports video pattern testing of DP1.2-capable displays.**