

High-Definition Multimedia Interface

Version 2.0

Quantum Data MOI v1.0

Test ID: HF2-31

April 11, 2014

Preface

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1.0 April 11, 2014 - Initial Release.

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Contact Information

The URL for the HDMI Forum web site is: <http://www.hdmiforum.org/>

The URL for the Quantum Data website is: <http://www.quantumdata.com>.

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Introduction

This document provides a set of Method of Implementation for test method described in HDMI Compliance Test Specification Version 2.0 (HDMI CTS 2.0). HDMI Forum created HDMI CTS 2.0 to specify a set of tests that should be performed to verify features described in HDMI Specification Version 2.0.

Scope

This document provides testing procedures for HDMI CTS 2.0 Test ID HF2-31: “Sink EDID – YCBCR 4:2:0 – Data Blocks.” The procedure below deals with single resolution and only one Test ID is considered at a time.

References Document

Normative References

High-Definition Multimedia Interface Specification Version 1.4b, October 11, 2011.
HDMI Compliance Test Specification Version 1.4b, October 11, 2011.
High-Definition Multimedia Interface Specification Version 2.0, August, 2013.
HDMI Compliance Test Specification Version 2.0,

Informative Reference

No additional informative references.

Test ID HF2-31: Sink EDID – YC_BC_R 4:2:0 – Data Blocks

Objective

Confirm that a YC_BC_R 4:2:0 capable Sink DUT EDID contains a valid Video Data Block and/or YC_BC_R 4:2:0 Capability Map Data Block.

Table 8-63 Sink EDID – YC_BC_R 4:2:0 – Related Data Block Requirements

Reference	Requirement
[HDMI 2.0: 7.1]	“When transmitting a Video Format listed in Table 7-1, Source Devices may utilize the YC _B C _R 4:2:0 Pixel Encoding method defined in this section with the VIC set to the corresponding value.”
[HDMI 2.0: 7.1.2]	“To indicate support for YC _B C _R 4:2:0 Pixel Encoding, an HDMI Sink shall use a Y420CMDB (YC _B C _R 4:2:0 Capability Map Data Block) and/or Y420VDB (YC _B C _R 4:2:0 Video Data Block), as defined in CEA-861-F Section 7.5.10 and 7.5.11, in its EDID, for all Video Formats for which it supports YC _B C _R 4:2:0 Pixel Encoding.”
CEA-861-F, Section 7.5.10	<See reference for details on YC _B C _R 4:2:0 Video Data Block>
CEA-861-F, Section 7.5.11	<See reference for details on YC _B C _R 4:2:0 Capability Map Data Block>

Capability(s)

The Source DUT supports at least one Video Format in YC_BC_R 4:2:0 color sampling mode.

Test Equipment

Item	Generic Equipment	Vendor Specific Equipment	Quantity
1	DDC Master	980 Advanced Test Platform series:	1
2	EDID Analyzer	980 HDMI Protocol Analyzer module HDMI CTS 2.0 Compliance Test Package #1	1

Generic Procedure

- 1 If the CDF field Sink_HDMI_YC_BC_R_420 is “N”, then SKIP this test.
- 2 Connect the Sink DUT to the DDC Master and EDID Analyzer.
- 3 Turn on the Sink DUT, have the DDC Master output +5V Power and read the Sink DUT’s EDID in response to a hot-plug. If the Hot Plug Detect signal is not received or the EDID is unreadable, then FAIL.

- 4 Using the EDID Analyzer, examine the YCbCr 4:2:0 Video Data Block or YCbCr 4:2:0 Capability Map Data Block (Y420VDB) of the EDID, parse and extract the declared SVDs. Also, examine the EDID's Video Data Block(s) for later steps.
- 5 For each VIC included in the CDF field Sink_HDMI_YCbCr_420_Video_Formats:
 - 5.1 If the VIC included in the CDF field Sink_HDMI_YCbCr_420_Video_Formats is not included in the extracted SVDs from the EDID, then FAIL.
- 6 If neither Y420VDB nor Y420CMDB is present in DUT's EDID, then FAIL.
- 7 If Y420VDB is present, and the length of Y420VDB is equal to 1, then FAIL.
- 8 If Y420CMDB is present and (Y420VDB[length] > 1) and no bits in Capability Bit Map set (=1), then FAIL.
- 9 For each SVD included in the body of the Y420VDB:
 - 9.1 If the same SVD (VIC) is included in the EDID's Video Data Block(s), then FAIL.
 - 9.2 If this SVD (VIC) is that of an interlaced Video Format or a Video Format that requires pixel repetition, then FAIL.
 - 9.3 If support for this SVD (VIC) is indicated in CDF field Sink_HDMI_YCbCr_420_Video_Formats as "N", then FAIL.
- 10 For each bit set to 1 in the Capability Bit Map of the Y420CMDB:
 - 10.1 If there is no SVD (VIC) corresponding to this bit in the EDID's Video Data Block(s), then FAIL.
 - 10.2 If this SVD (VIC) corresponding to this bit in the EDID's Video Data Block(s) is that of an interlaced Video Format or a Video Format that requires pixel repetition, then FAIL.
 - 10.3 If support for this SVD (VIC) is indicated in the CDF field Sink_HDMI_YCbCr_420_Video_Formats as "N", then FAIL.

Vendor Specific Test Procedure

Test Equipment

A variety of equipment is needed for testing HDMI products. Each piece is authorized and included by name in this Compliance Test Specification. This section describes the Quantum Data test equipment.

HDMI Protocol Analyzer module

The Quantum Data 980 HDMI Protocol Analyzer module can be installed in any of the 980 series Advanced Test Platforms. This 980 HDMI Protocol Analyzer module serves the generic test functions called out in the HDMI 2.0 Generic CTS. Refer to the table below:

Item	Quantum Data Equipment	
1	980 Advanced Test Platform series:	
	Equipped with:	980 HDMI Protocol Analyzer module
		HDMI CTS 2.0 Compliance Test Package #1

980 HDMI Protocol Analyzer Module with 980 Series Platform Configurations

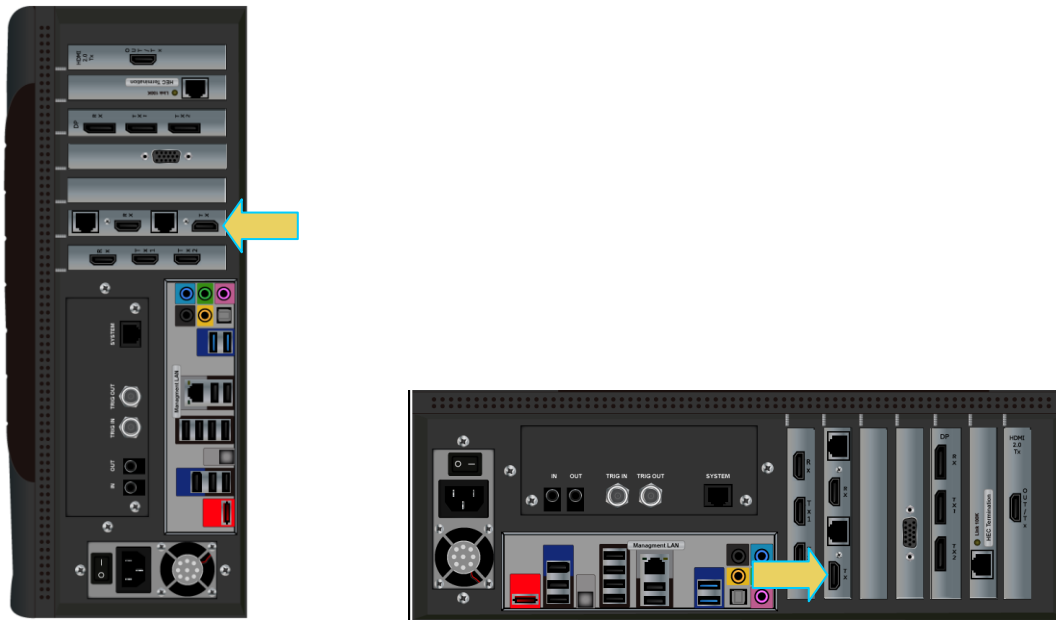
The figures below show depictions of the 980 HDMI Protocol Analyzer module equipped in various 980 series platforms. **Note:** Card positioning may vary depending on configuration.



Current 980 HDMI Protocol Analyzer board rev.



Previous 980 HDMI Protocol Analyzer board rev.



Sink EDID YCbCr 4:2:0 Data Blocks

Test ID HF2-31 – Sink EDID - YCbCr 4:2:0 – Data Blocks

1. Objective

Confirm that a YCbCr 4:2:0 capable Sink DUT EDID contains a valid Video Data Block and/or YCbCr 4:2:0 Capability Map Data Block.

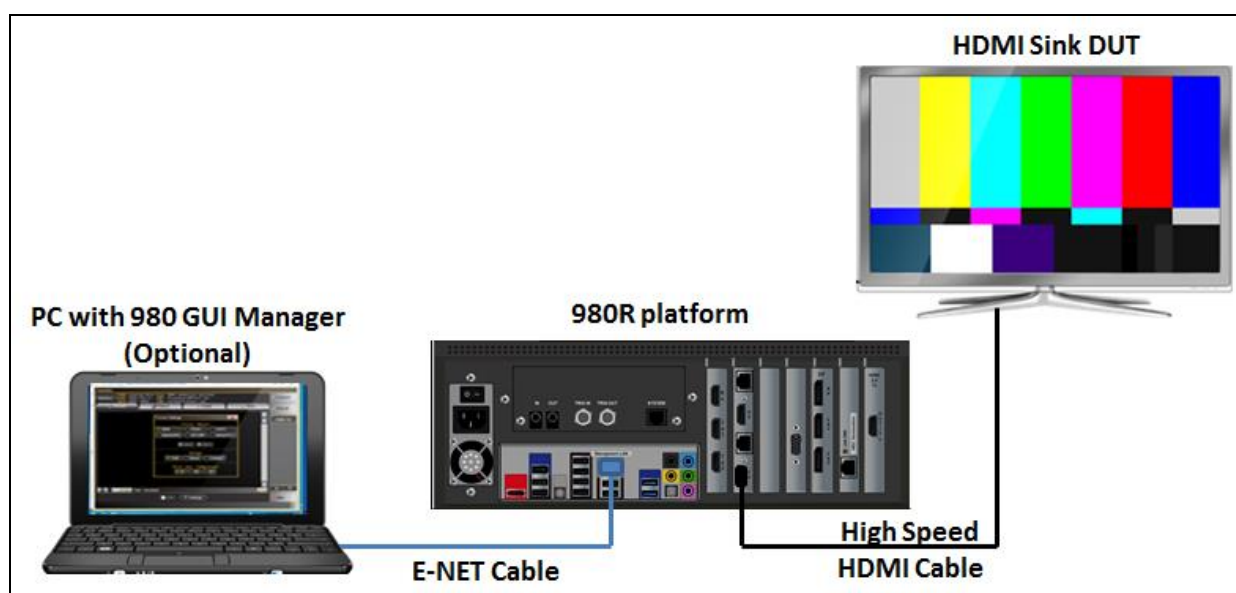
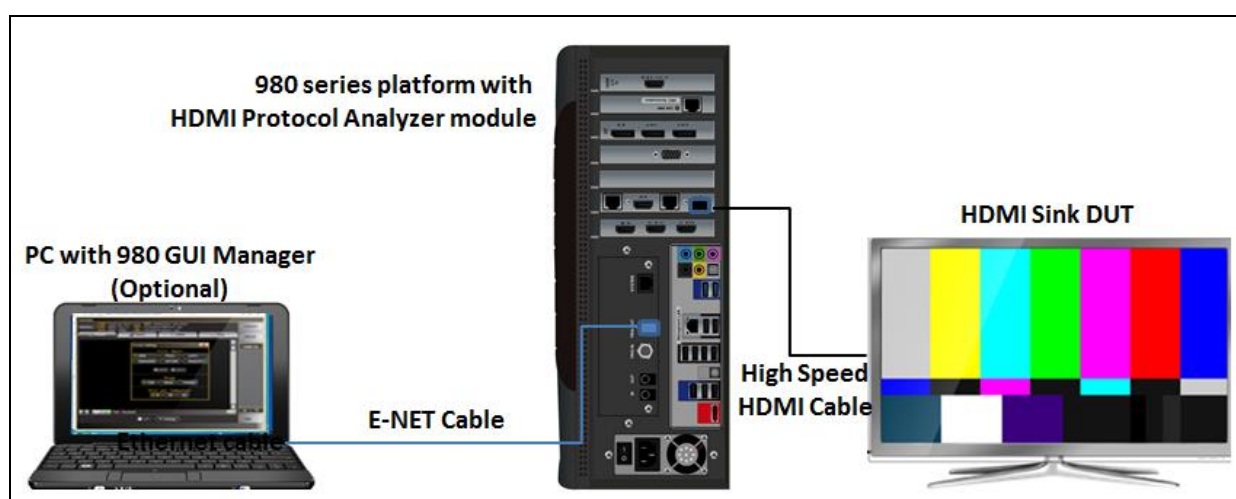
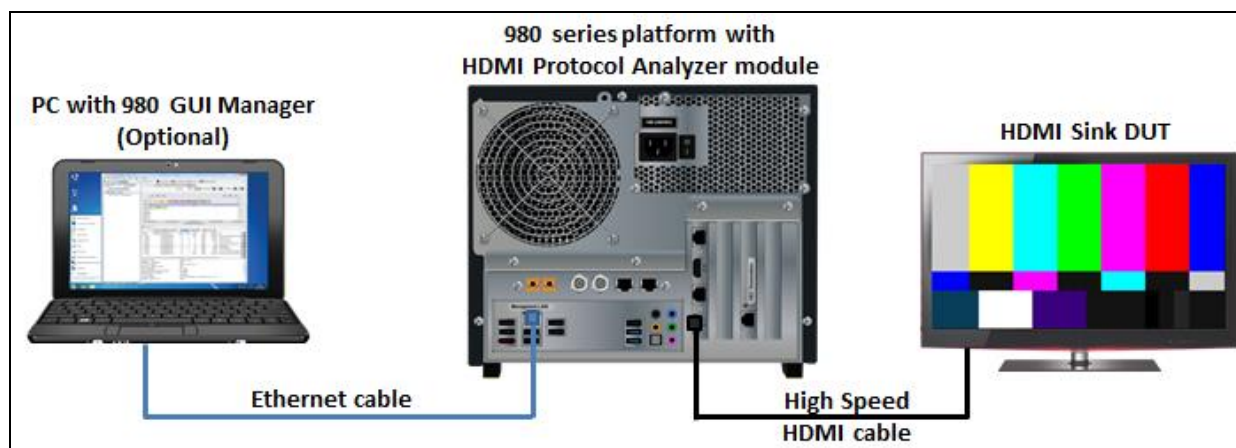
2. Test Overview

The Pass/Fail criteria for this test is assessed by the 980 HDMI Compliance Test application which provides the EDID Analyzer function. No human analysis or observation required.

3. Procedure

Use the following procedure to conduct this test.

1. Connect Sink DUT to the Quantum Data 980 HDMI Protocol Analyzer module. Use a High Speed HDMI cable. Refer to the figures below for reference.

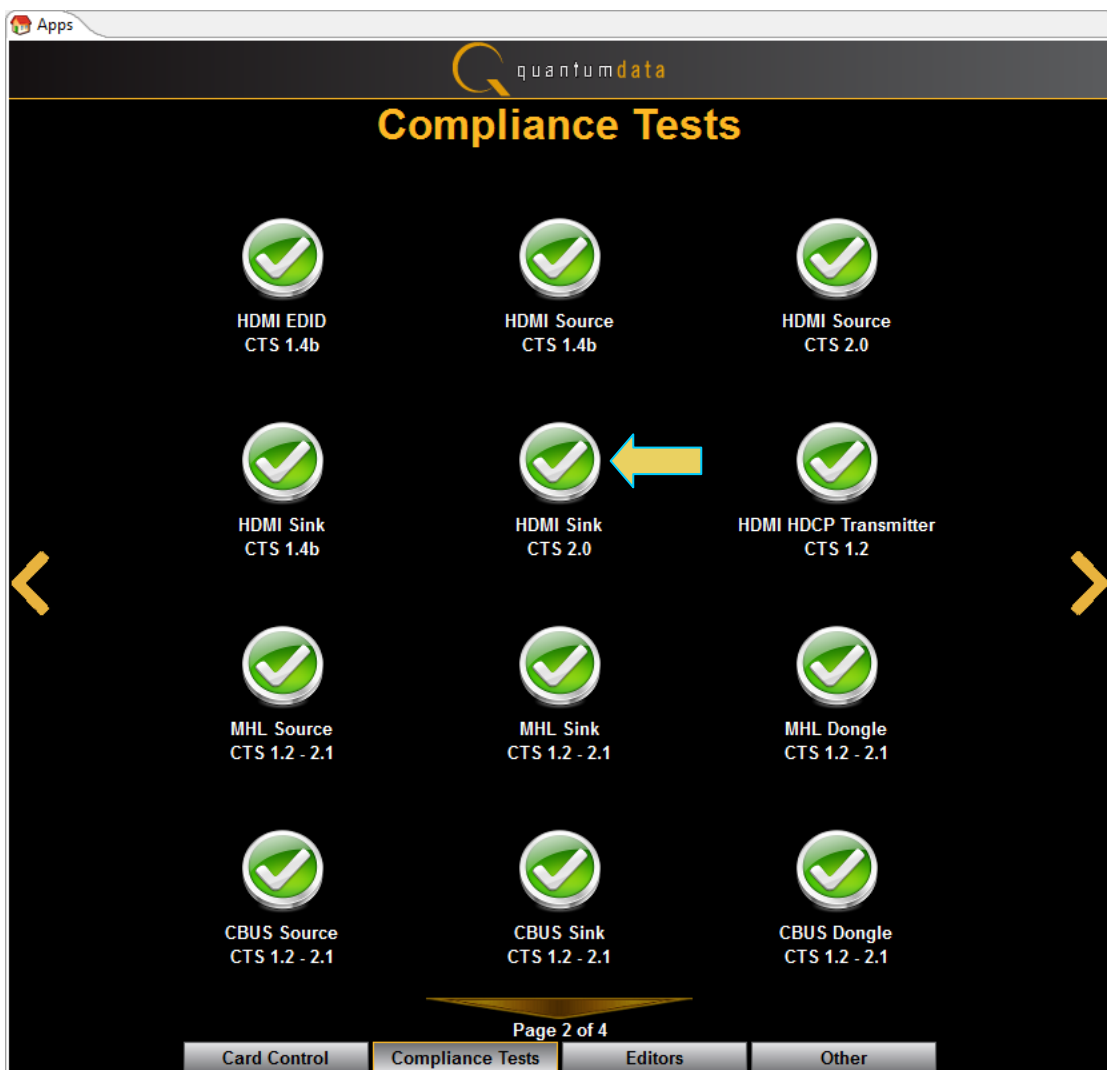


2. Use Quantum Data 980 Embedded Manager GUI (touchscreen) or invoke Quantum Data 980 External Manager GUI (Windows application).

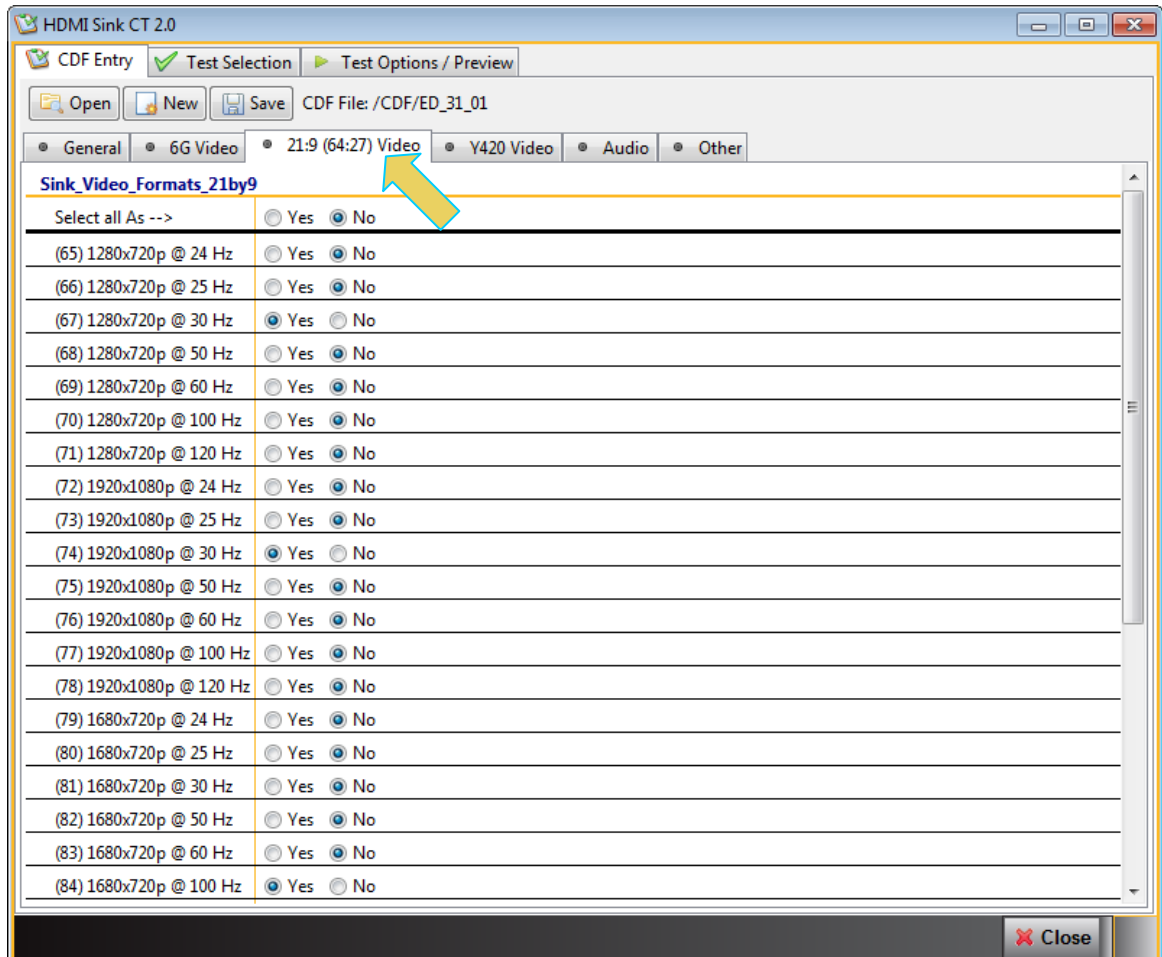
Note: You will not need to connect the PC shown in the figures above if you are running the compliance test through the 980's embedded display. The PC running the 980 HDMI Protocol Analyzer module's compliance test application is connected to the 980 through a standard Ethernet cable.

3. Complete the following steps:

- 3.1 Click on the HDMI Sink CTS 2.0 icon in the Compliance Tests page of the Apps panel. Refer to the screen example below.



- 3.2 Navigate to the CDF tab if not already there. Complete the General sub tab and the remaining tabs in the CDF. If there is a saved CDF file, then click on Open and select it. Otherwise, enter the DUT's CDF information and optionally click on Save to save the CDF. Refer to the screen examples below which show the important settings for this test.



HDMI Sink CT 2.0

CDF Entry ☒ Test Selection ☐ Test Options / Preview

Open New Save CDF File: /CDF/ED_31_01

General 6G Video 21:9 (64:27) Video **Y420 Video** Audio Other

Sink_HDMI_YCBCR_420 Does the DUT support YCbCr 4:2:0 Pixel decoding?
☒ Yes ☐ No

Sink_HDMI_YCBCR_420_DC10 Does the DUT support YCbCr 4:2:0 Deep Color Pixel decoding with 10-bits per component?
☒ Yes ☐ No

Sink_HDMI_YCBCR_420_DC12 Does the DUT support YCbCr 4:2:0 Deep Color Pixel decoding with 12-bits per component?
☒ Yes ☐ No

Sink_HDMI_YCBCR_420_DC16 Does the DUT support YCbCr 4:2:0 Deep Color Pixel decoding with 16-bits per component?
☐ Yes ☒ No

Sink_HDMI_YCBCR_420_BT2020_YCC Does the DUT support YCC 4:2:0 Pixel encoding in BT.2020 Y'Cb'Cr' Colorimetry?
☐ Yes ☒ No

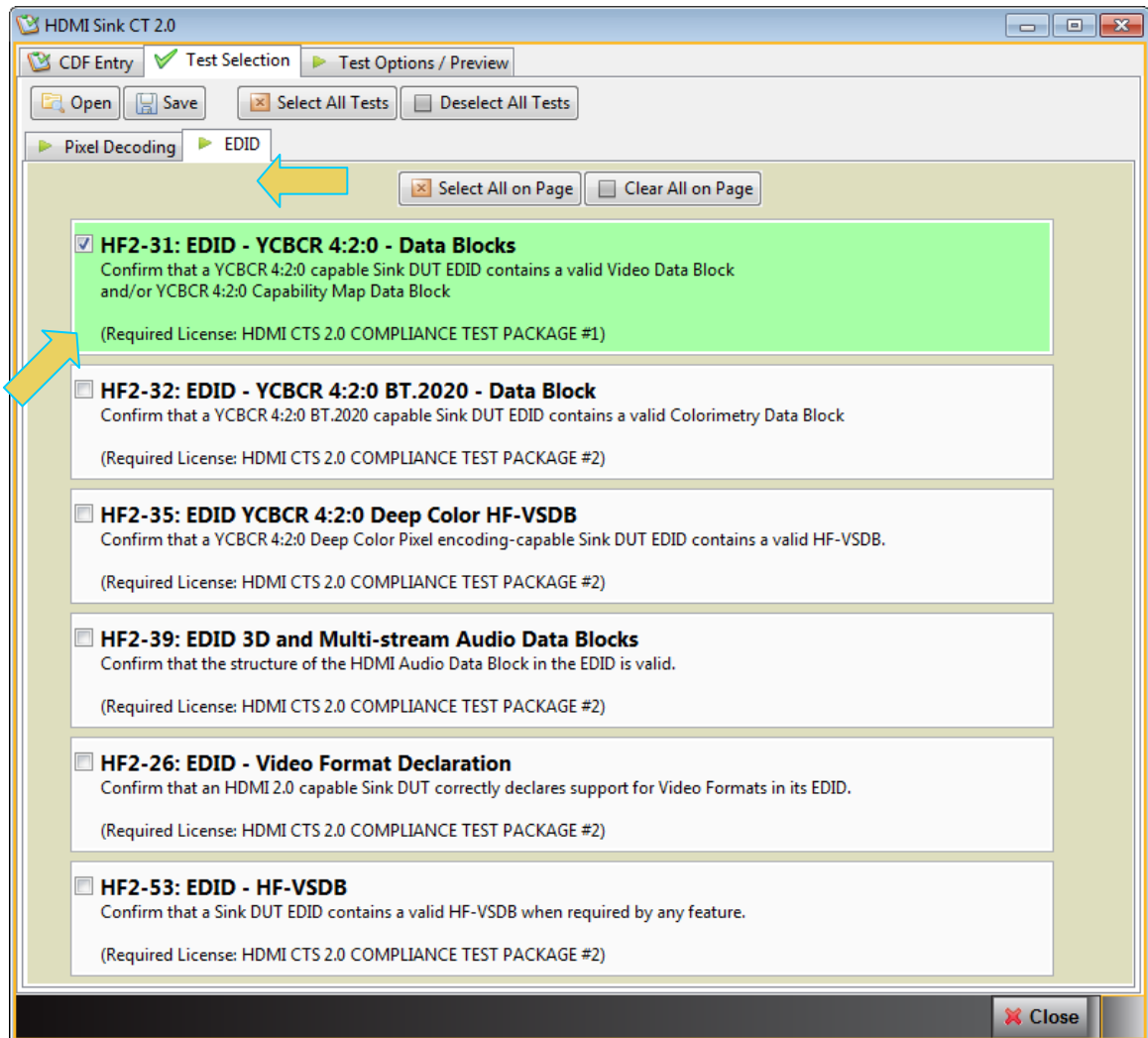
Sink_HDMI_YCBCR_420_BT2020_cYCC Does the DUT support YCC 4:2:0 Pixel encoding in BT.2020 Yc'Cb'Cr' Colorimetry?
☐ Yes ☒ No

Sink_HDMI_YCBCR_420_Video_Formats

(97) 3840x2160p @ 60 Hz 16:9	<input checked="" type="checkbox"/> 24 <input type="checkbox"/> 30 <input type="checkbox"/> 36 <input type="checkbox"/> 48	(bits per pixel)
(96) 3840x2160p @ 50 Hz 16:9	<input type="checkbox"/> 24 <input type="checkbox"/> 30 <input type="checkbox"/> 36 <input type="checkbox"/> 48	(bits per pixel)
(102) 4096x2160p @ 60 Hz	<input checked="" type="checkbox"/> 24 <input type="checkbox"/> 30 <input type="checkbox"/> 36 <input type="checkbox"/> 48	(bits per pixel)
(101) 4096x2160p @ 50 Hz	<input type="checkbox"/> 24 <input type="checkbox"/> 30 <input type="checkbox"/> 36 <input type="checkbox"/> 48	(bits per pixel)
(107) 3840x2160p @ 60 Hz 64:27	<input type="checkbox"/> 24 <input type="checkbox"/> 30 <input type="checkbox"/> 36 <input type="checkbox"/> 48	(bits per pixel)
(106) 3840x2160p @ 50 Hz 64:27	<input type="checkbox"/> 24 <input type="checkbox"/> 30 <input type="checkbox"/> 36 <input type="checkbox"/> 48	(bits per pixel)

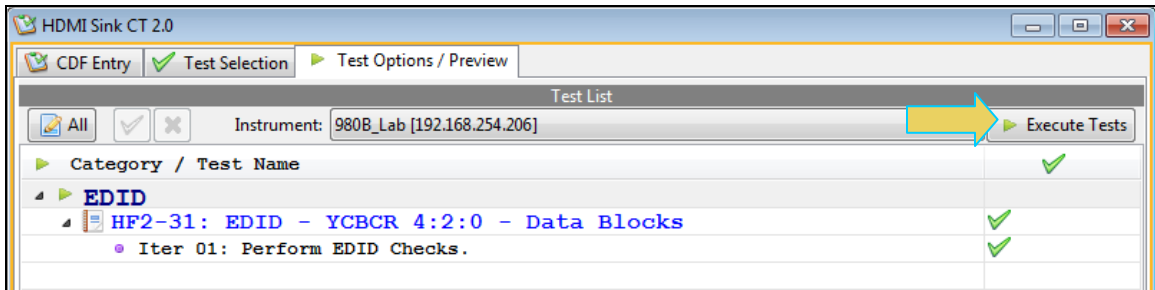
Close

- 3.3 Click on the Test Selection tab, and select the EDID tab and then the HF2-31 EDID - YCBCR 4:2:0 - Data Block Test. Refer to the screen example below.

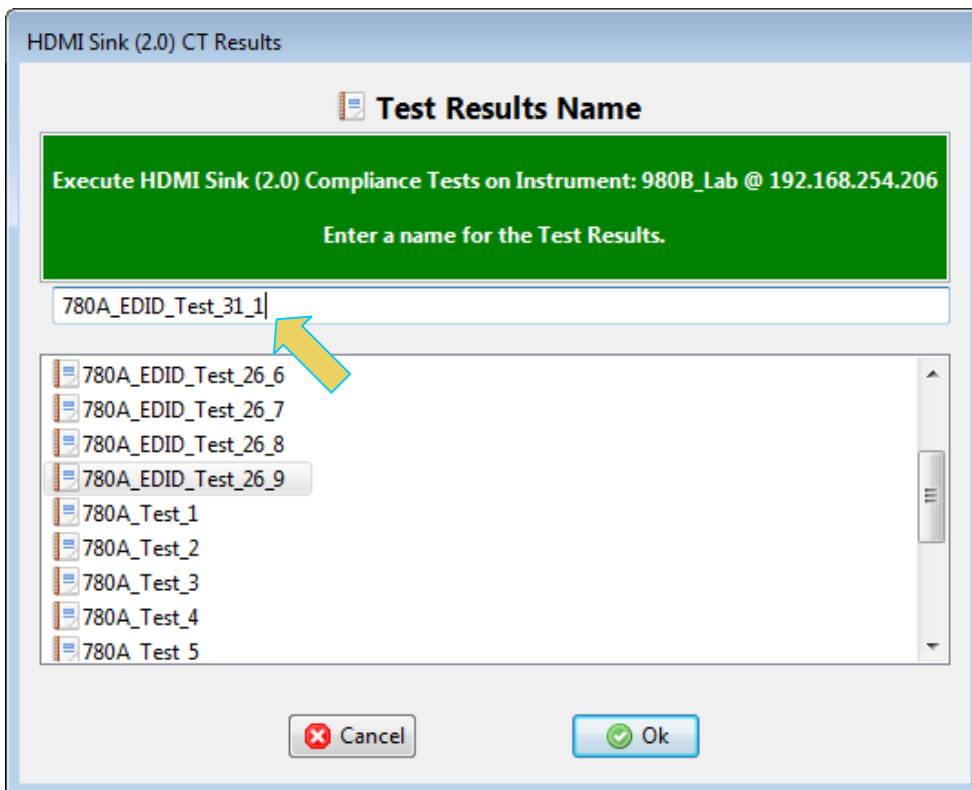


- [illegible]

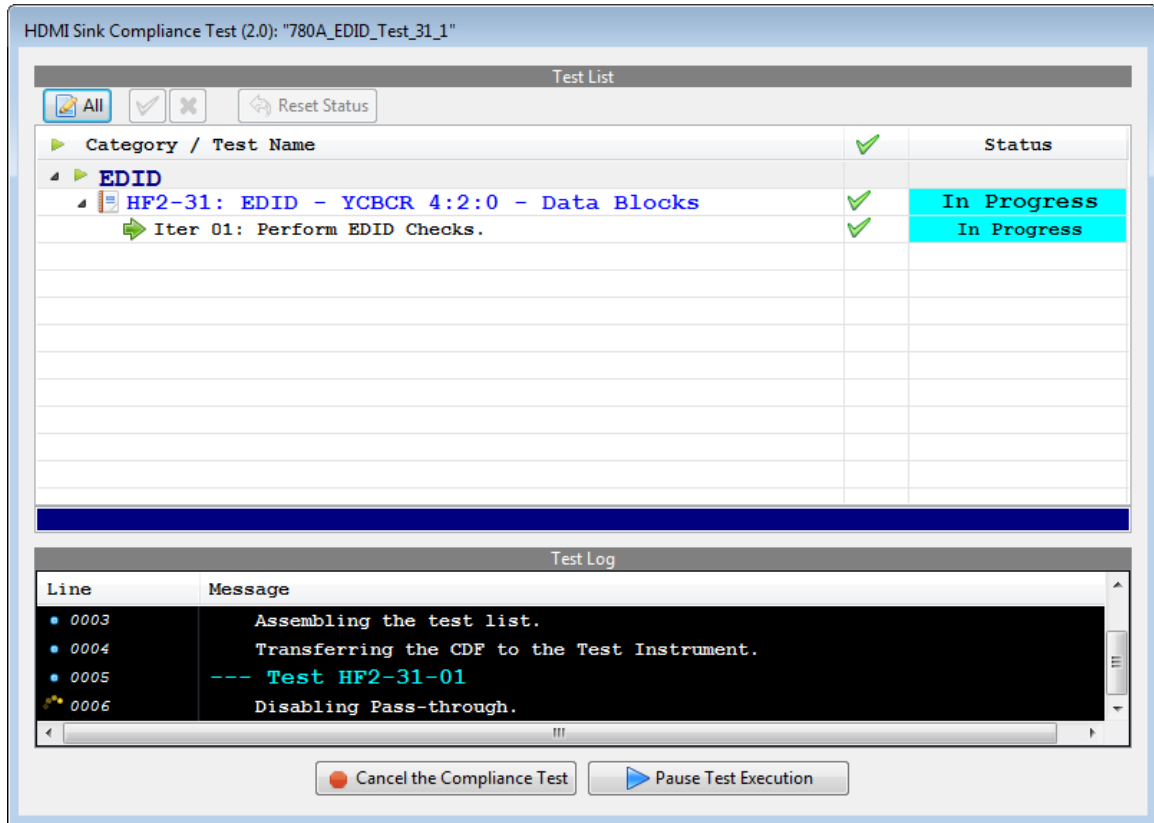
- 3.5 Click on the Execute tests activation button to initiate the test. Refer to the screen example below.



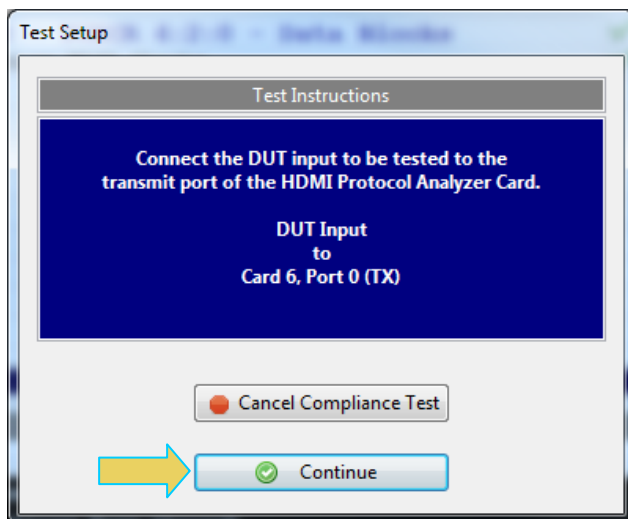
Note: You will be prompted with a dialog box to assign a name to the test results. Refer to the screen example below.



A Test Results window and log will appear as shown below.



You will be prompted with the test setup description. Verify the test setup and click on Continue to run the test.



The test results will be assessed without any user examination required.

4. If the 980 HDMI Protocol Analyzer's compliance test application reports PASS, then PASS.
If the 980 HDMI Protocol Analyzer's compliance test application reports FAIL, then FAIL.

When the test is completed a Test Results Viewer screen will appear.

