

High-Definition Multimedia Interface

Version 2.0

Quantum Data MOI v1.0

Test ID: HF1-10

April 24, 2014

Preface

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Document Revision History

1.0 April 24, 2014 - Initial Release.

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Contact Information

The URL for the HDMI Forum web site is: <http://www.hdmiforum.org/>

The URL for the Quantum Data website is: <http://www.quantumdata.com>.

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Introduction

This document provides a set of Method of Implementation for test method described in HDMI Compliance Test Specification Version 2.0 (HDMI CTS 2.0). HDMI Forum created HDMI CTS 2.0 to specify a set of tests that should be performed to verify features described in HDMI Specification Version 2.0.

Scope

This document provides testing procedures for HDMI CTS 2.0 Test ID HF1-10: Source TMDS Protocol – 6G – TMDS Bit Clock Ratio.” The procedure below deals with single resolution and only one Test ID is considered at a time.

References

Normative References

High-Definition Multimedia Interface Specification Version 1.4b, October 11, 2011.
HDMI Compliance Test Specification Version 1.4b, October 11, 2011.
High-Definition Multimedia Interface Specification Version 2.0, August, 2013.
HDMI Compliance Test Specification Version 2.0.

Informative Reference

No additional informative references.

Test ID HF1-10: Source TMDS Protocol – 6G – TMDS Bit Clock Ratio

Objective

Confirm that the Source changes the TMDS Bit Clock Ratio correctly according to the output signal.

Table 7-21 Source TMDS Protocol - 6G – TMDS Bit Clock Ratio Requirements

| Reference | Requirement |
|--|-----------------------------|
| [HDMI 2.0: 6.1.3.2] Control for TMDS Bit Period/TMDS Clock-Period Ratio | <See reference for details> |
| [HDMI 2.0: 10.4.1.4] TMDS Configuration | <See reference for details> |

Capability(s)

The Source DUT supports any Video Format/color mode for TMDS Character Rate above 340Mcsc up to 600Mcsc.

Test Equipment

| Item | Generic Equipment | Vendor Specific Equipment | Quantity |
|------|--------------------|--|----------|
| 1 | DDC (I2C) Analyzer | 980 Advanced Test Platform series: 980 HDMI Protocol Analyzer module HDMI CTS 2.0 Compliance Test Package #2 | 1 |

Generic Procedure

- 1 If the CDF field Source_Above_340 is “N”, then SKIP this test.

Setup:
- 2 Configure the EDID, which indicates all Video Formats necessary for this test.

Measure:
- 3 Operate the Source DUT to output any DUT-Supported Video Format for a TMDS Character Rate above 340Mcsc up to 600Mcsc:
- 4 If the Source DUT does not write 1 to the TMDS_Bit_Clock_Ratio bit, then FAIL.
- 5 Operate the Source DUT to output either 640x480p or 720x480p.

5.1 If neither 640x480p or 720x480p are supported, then use 720x576p.
- 6 If the Source DUT does not write 0 to the TMDS_Bit_Clock_Ratio bit, then FAIL.

- 7 If the Source DUT outputs or can be operated to output a YCBCR 4:2:0 pixel encoded signal, then FAIL.

Vendor Specific Test Procedure

Test Equipment

A variety of equipment is needed for testing HDMI products. Each piece is authorized and included by name in this Compliance Test Specification. This section describes the Quantum Data test equipment.

HDMI Protocol Analyzer module

The Quantum Data 980 HDMI Protocol Analyzer module can be installed in any of the 980 series Advanced Test Platforms. This 980 HDMI Protocol Analyzer module serves the generic test functions called out in the HDMI 2.0 Generic CTS. Refer to the table below:

| Item | Quantum Data Equipment | |
|------|------------------------------------|---|
| 1 | 980 Advanced Test Platform series: | |
| | Equipped with: | 980 HDMI Protocol Analyzer module |
| | | HDMI CTS 2.0 Compliance Test Package #1 |

980 HDMI Protocol Analyzer Module with 980 Series Platform Configurations

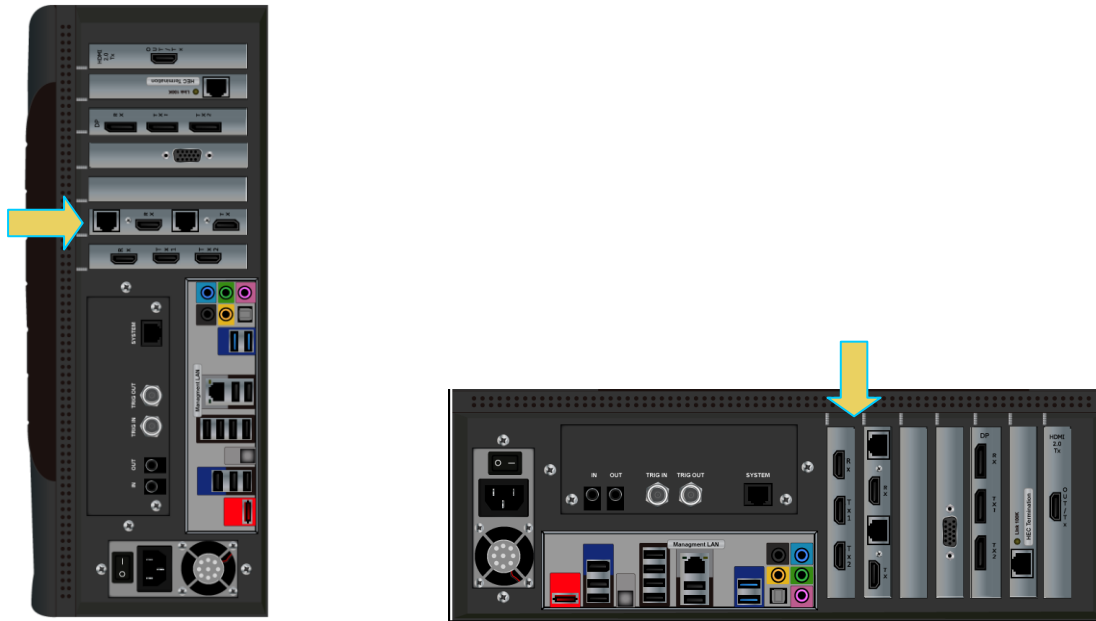
The figures below show depictions of the 980 HDMI Protocol Analyzer module equipped in various 980 series platforms. **Note:** Card positioning may vary depending on configuration.



Current 980 HDMI Protocol Analyzer board rev.



Previous 980 HDMI Protocol Analyzer board rev.



Source TMDS Bit Clock Ratio

Test ID HF1-10 - Source TMDS Protocol – 6G – TMDS Bit Clock Ratio

1. Objective

Confirm that the Source changes the TMDS Bit Clock Ratio correctly according to the output signal.

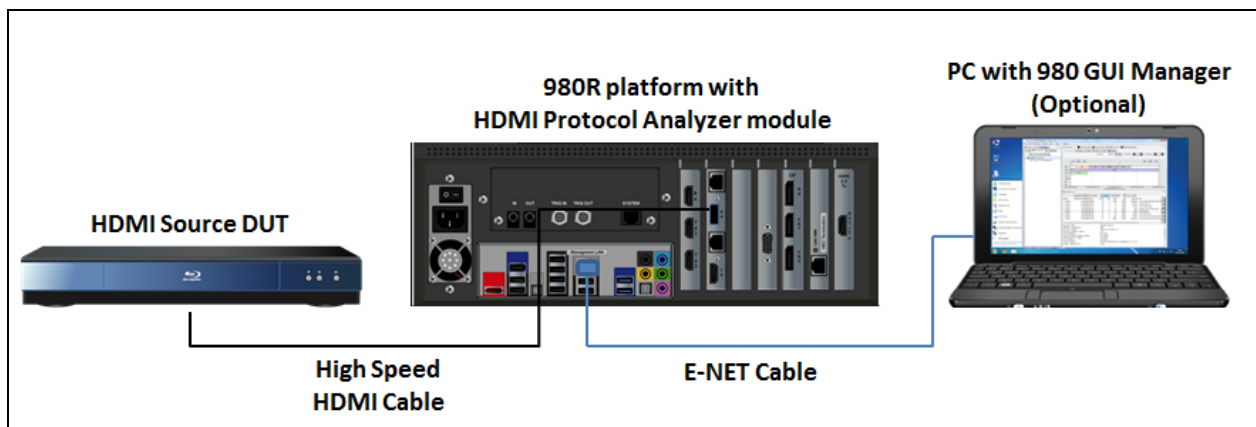
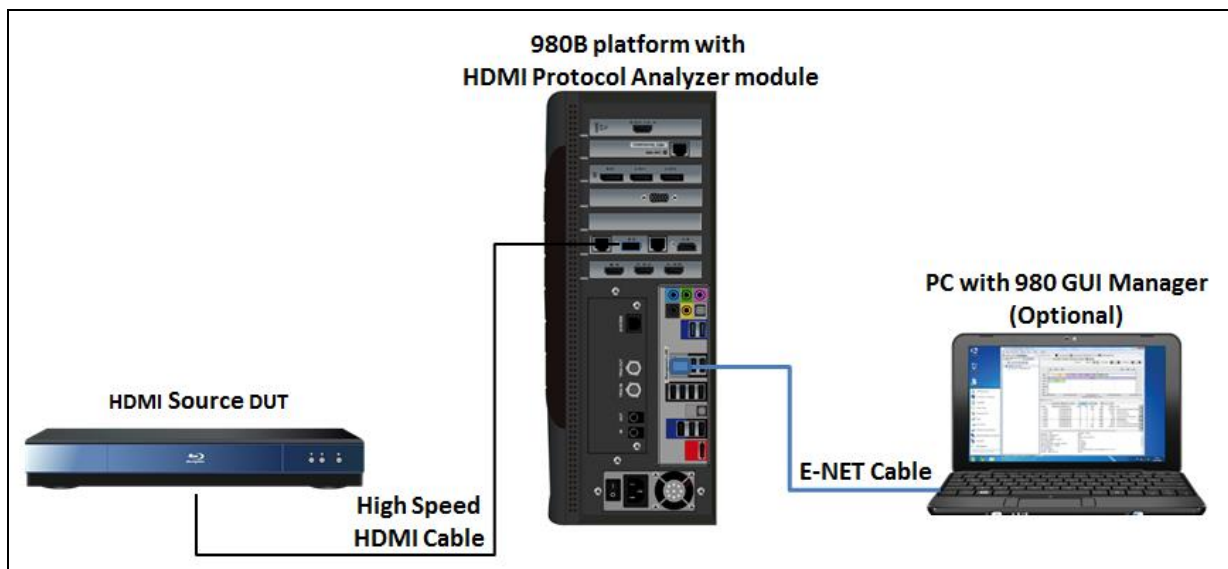
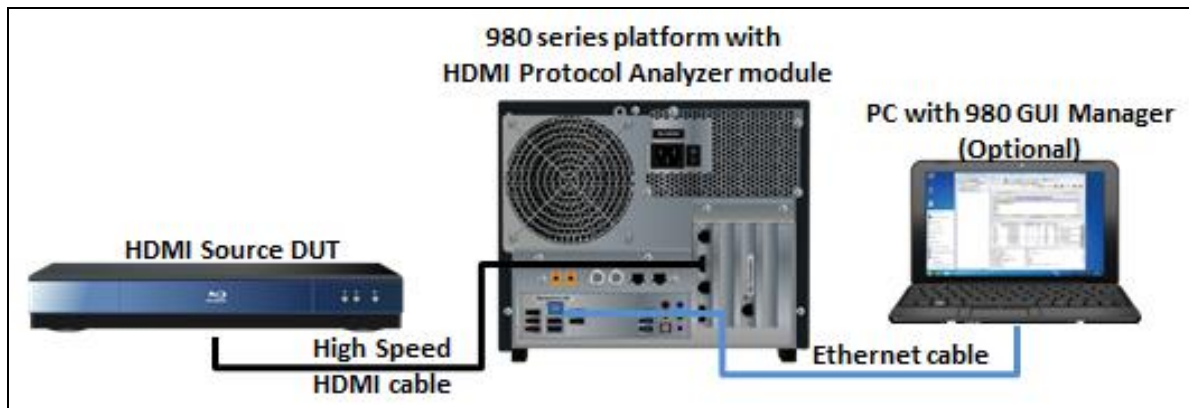
2. Test Overview

This test is run for one compliant format timing with a character rate above 340MB/s up to 600MB/s. The 980 HDMI Protocol Analyzer's Compliance Test application automatically provisions the EDIDs during the test to facilitate the source's outputting of the appropriate format. The Pass/Fail criteria is assessed by the application with no human examination required.

3. Procedure

Use the following procedure to conduct this test.

- 1 Connect Source DUT to the Quantum Data 980 HDMI Protocol Analyzer at the module's port labeled Rx. Use a High Speed HDMI cable. The figures below show depictions of connections to the 980 HDMI Protocol Analyzer module residing in various 980 series chassis.

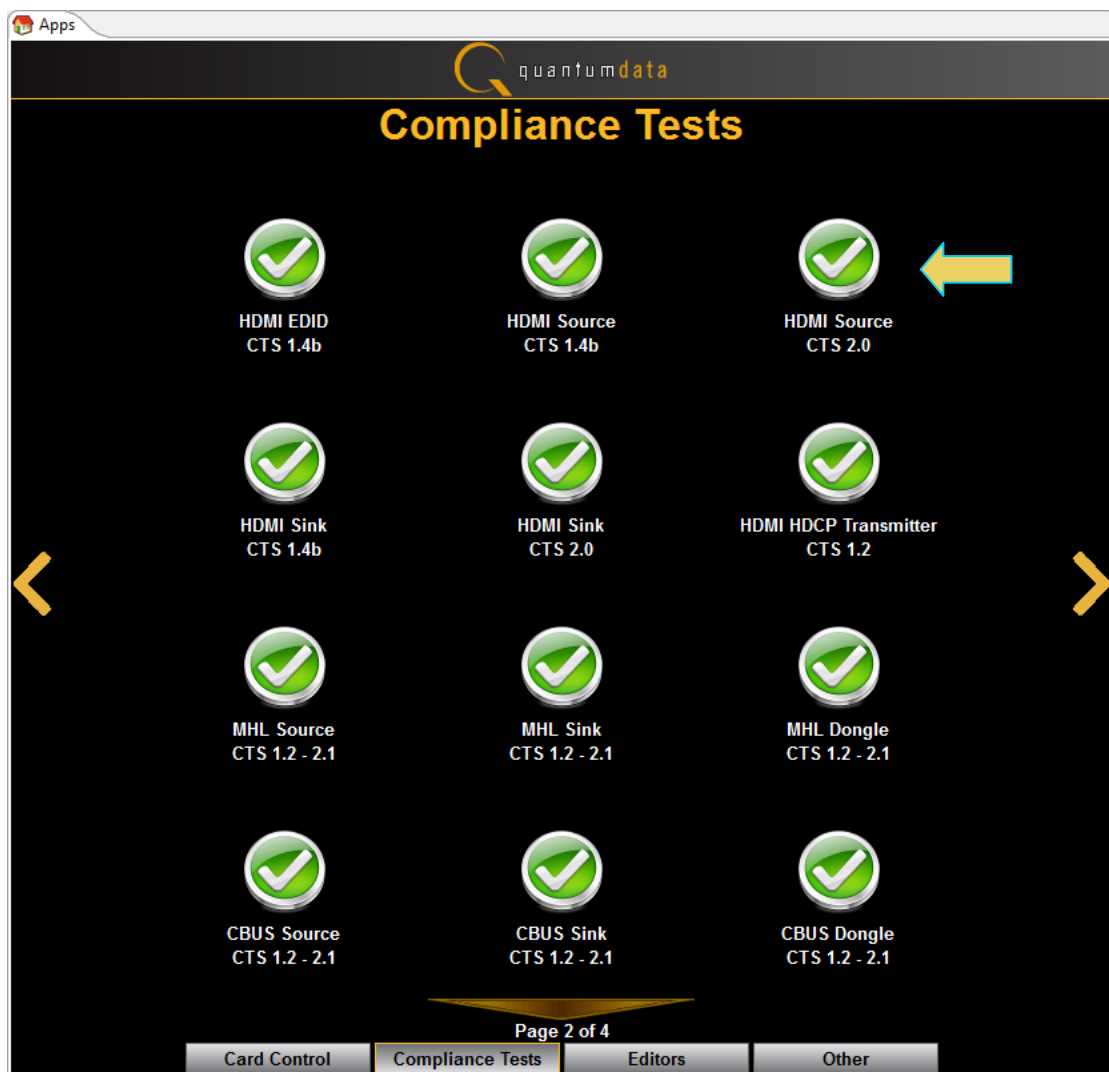


1. Operate the Source DUT to output any DUT-Supported Video Format for a TMDS Character Rate above 340Mcsc up to 600Mcsc.

2. Use Quantum Data 980 Embedded Manager GUI (touchscreen) or invoke Quantum Data 980 External Manager GUI (Windows application).

Note: You will not need to connect the PC shown in the figures above if you are running the compliance test through the 980's embedded display. The PC running the 980 HDMI Protocol Analyzer module's compliance test application is connected to the 980 through a standard Ethernet cable.

3. Complete the following steps:
 - 3.1 Click on the HDMI Source CTS 2.0 icon in the Compliance Tests page of the Apps panel. Refer to the screen shot below.



- 3.2 Navigate to the CDF tab if not already there. If there is a saved CDF file, then click on Open and select it. Otherwise, enter the DUT's CDF information for the General sub tab and the 6G Video sub tab and optionally click on Save button to save the CDF.

HDMI Src CT 2.0

CDF Entry Test Selection Test Options / Preview

Open Save CDF File: <not saved>

General Y420 Video 21:9 (64:27) Video 6G Video Read Request

Source_Above_340 Does the product support any bit/color mode for TMDS Character Rate above 340Mscs? up to 600Mscs?

☒ Yes ☐ No

Source_2160p_Video_Above_340

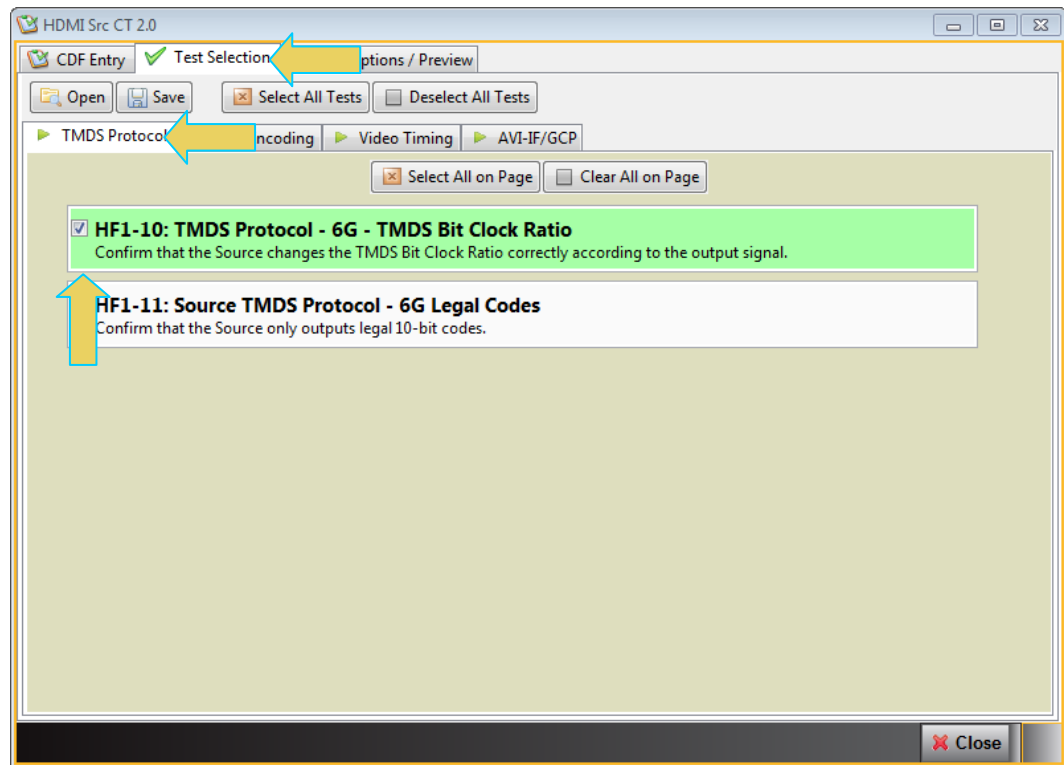
| | |
|----------------------------------|---|
| (96) 3840x2160p @ 50 Hz 16:9 | <input type="radio"/> Yes <input checked="" type="radio"/> No |
| (97) 3840x2160p @ 60 Hz 16:9 | <input checked="" type="radio"/> Yes <input type="radio"/> No |
| (101) 4096x2160p @ 50 Hz 256:135 | <input type="radio"/> Yes <input checked="" type="radio"/> No |
| (102) 4096x2160p @ 60 Hz 256:135 | <input checked="" type="radio"/> Yes <input type="radio"/> No |
| (106) 3840x2160p @ 50 Hz 64:27 | <input type="radio"/> Yes <input checked="" type="radio"/> No |
| (107) 3840x2160p @ 60 Hz 64:27 | <input type="radio"/> Yes <input checked="" type="radio"/> No |

Source_2160p_DC_Video_Formats_Above_340

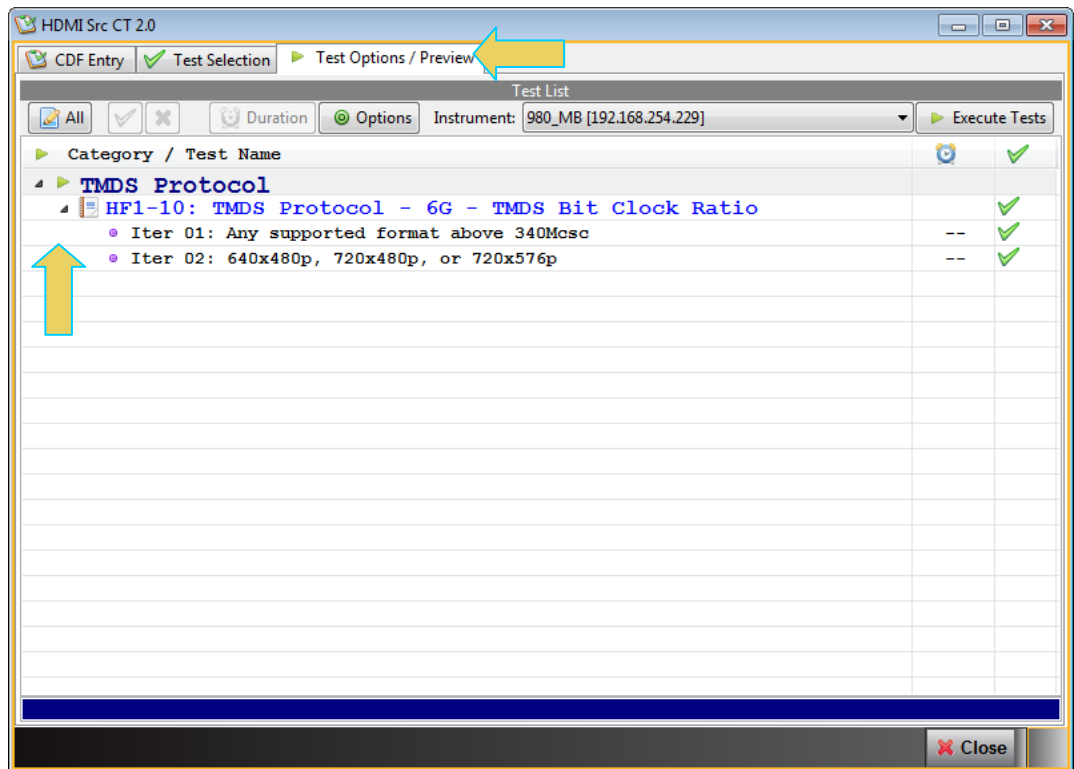
| Mode | 30 | 36 | 48 | bits per pixel |
|----------------------------------|--------------------------|--------------------------|--------------------------|------------------|
| (93) 3840x2160p @ 24 Hz 16:9 | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | (bits per pixel) |
| (94) 3840x2160p @ 25 Hz 16:9 | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | (bits per pixel) |
| (95) 3840x2160p @ 30 Hz 16:9 | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | (bits per pixel) |
| (98) 4096x2160p @ 24 Hz 256:135 | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | (bits per pixel) |
| (99) 4096x2160p @ 25 Hz 256:135 | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | (bits per pixel) |
| (100) 4096x2160p @ 30 Hz 256:135 | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | (bits per pixel) |
| (103) 3840x2160p @ 24 Hz 64:27 | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | (bits per pixel) |

Close

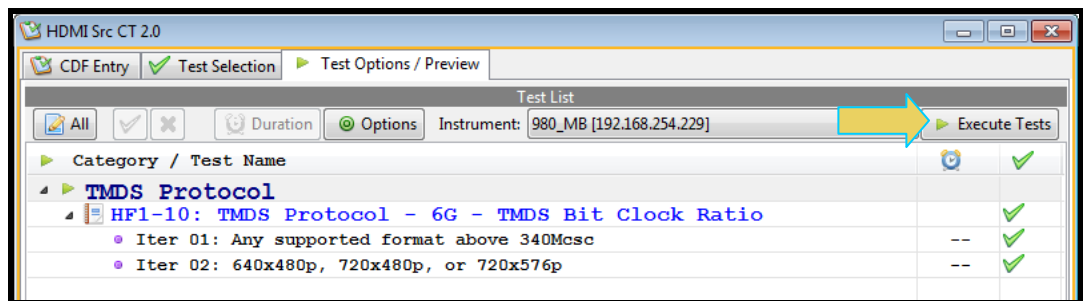
- 3.3 Click on the Test Selection tab, and select the HF1-10 TMDS Protocol – 6G – TMDS Bit Clock Ratio Test. Refer to the screen example below.



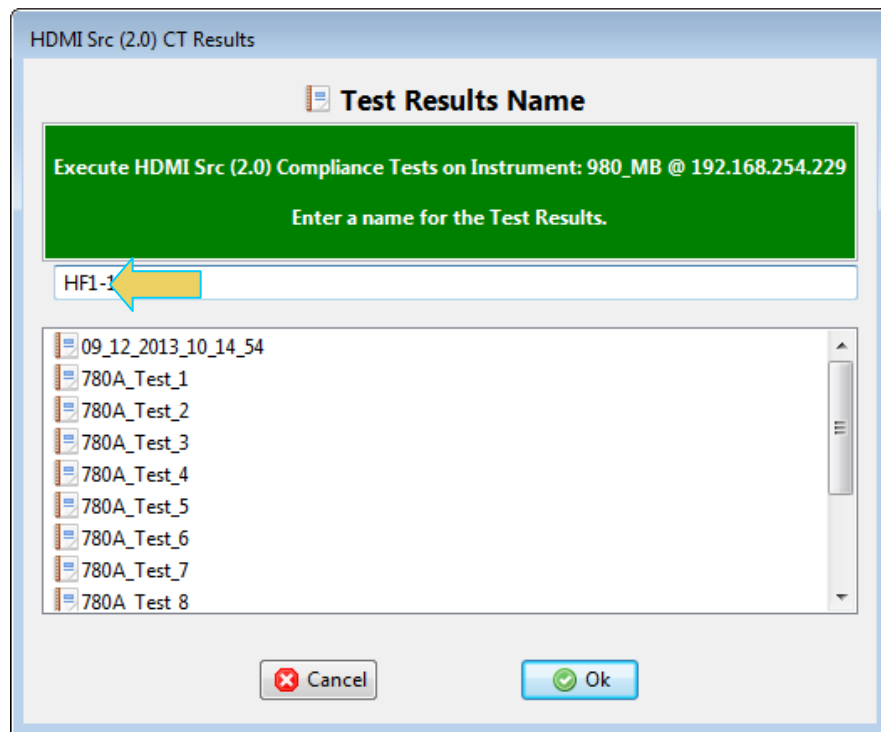
- 3.3 Click on Test Options / Preview tab and review the list of tests. Refer to the screen example below.



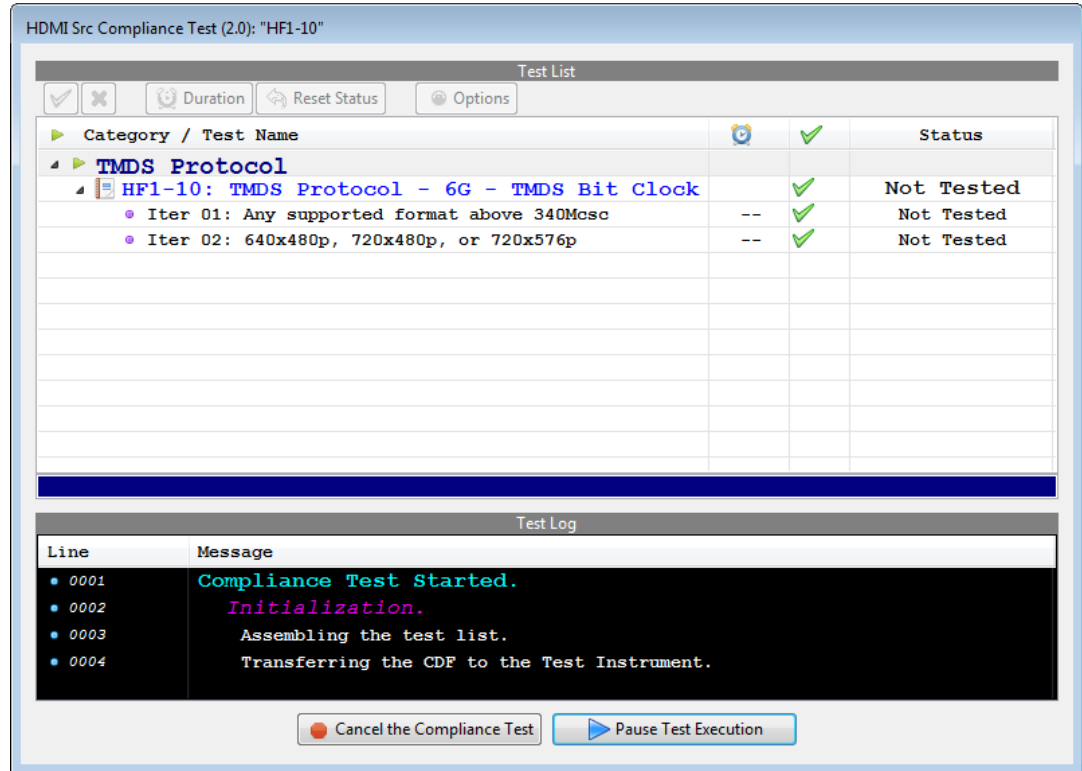
- 3.4 Click on Execute tests activation button to initiate the test. Refer to the screen example below.



Note: You will be prompted with a dialog box to assign a name to the test results. Refer to the screen example below:




The test will start and a new Test Window will appear as shown below.



You will also be prompted with a dialog box informing you of the requirements of the DUT. Verify that the source is outputting the required HDMI format and pixel encoding and press Continue to run the test.

DUT Configuration

 **Required DUT Configuration**

Test HF1-10, Iter-01

Confirm that the Source changes the TMDS Bit Clock Ratio correctly according to the output signal.

Please verify that the DUT is configured per the requirements below.
NOTE: The test EDID has been applied and hot-plug has been toggled
and the DUT may already be configured per the EDID.
You can use the 980 Real-Time to help verify that the DUT is configured and stable.
Press "Continue" when the DUT is ready to be tested.

Format:

- Any Video Format with TMDS Character Rate above 340Mscs up to 600Mscs


Content:


- There is no content requirement for this test.


Audio:


- There is no audio requirement for this test.


EDID (Default): <generated>


 Change EDID

 Default EDID

 View EDID

 Cancel Compliance Test

 Pause Execution

 Continue

- When the test is complete a Test Results screen appears. Refer to the screen example below.

