

High-Definition Multimedia Interface

Version 2.0

Quantum Data MOI v1.0

Test ID: HF1-33

April 11, 2014

Preface

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Document Revision History

1.0 April 11, 2014 - Initial Release.

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Contact Information

The URL for the HDMI Forum web site is: <http://www.hdmiforum.org/>

The URL for the Quantum Data website is: <http://www.quantumdata.com>.

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Introduction

This document provides a set of Method of Implementation for test method described in HDMI Compliance Test Specification Version 2.0 (HDMI CTS 2.0). HDMI Forum created HDMI CTS 2.0 to specify a set of tests that should be performed to verify features described in HDMI Specification Version 2.0.

Scope

This document provides testing procedures for HDMI CTS 2.0 Test ID HF1-33: “Source Video Timing - YCBCR 4:2:0 Tests.” The procedure below deals with single resolution and only one Test ID is considered at a time.

References Document

Normative References

High-Definition Multimedia Interface Specification Version 1.4b, October 11, 2011.
HDMI Compliance Test Specification Version 1.4b, October 11, 2011.
High-Definition Multimedia Interface Specification Version 2.0, August, 2013.
HDMI Compliance Test Specification Version 2.0.

Informative Reference

No additional informative references.

Test ID HF1-33: Source Video Timing - YCbCr 4:2:0 Tests

Objective

Confirm that the Source outputs a correct timing for YCbCr 4:2:0 timings.

Table 7-56 Source Video Timing – YCbCr 4:2:0 Requirements

Reference	Requirement
[HDMI 2.0: 7.1]	“YCbCr 4:2:0 video is carried at a TMDS Character Rate equal to 1/2 the Pixel Clock Rate”
CEA 861-F, Section 4	<See reference for details on Video Timings>

Capability(s)

The Source DUT supports at least one Video Format in YCbCr 4:2:0 color sampling mode.

Test Equipment

Item	Generic Equipment	Vendor Specific Equipment	Quantity
1	Video Timing Analyzer	980 Advanced Test Platform series: 980 HDMI Protocol Analyzer module HDMI CTS 2.0 Compliance Test Package #1	1

Generic Procedure

- 1 If the CDF field Source_HDMI_YCbCr_420 is “N”, then SKIP this test.
- 2 Connect the Source DUT to a 297MHz Video Protocol Analyzer with the DDC Slave Emulator and EDID Emulator.
- 3 Program the EDID Emulator to reveal an EDID containing the following:
 - 3.1 YCbCr 4:2:0 Video Data Block with:
 - 3.1.1 YCbCr 4:2:0-only with SVDs = 96, 97, 101, 102, 106 and 107 (NOTE: If a regular Video Data Block is also present, then it shall not contain SVDs = 96, 97, 101, 102, 106, or 107).
 - 3.1.2 No HF-VSDB shall be included.
- 4 Operate the Source DUT to output a 24-bit/Pixel YCbCr 4:2:0 Pixel encoded signal at a Video Format for which it supports 4:2:0 transmission (see CDF field Source_HDMI_YCbCr_420), repeating all of the following tests for at least one of the supported Video Formats.
- 5 If the Pixel Clock frequency is outside the range -0.5% (-0.6% when frame rate is 60Hz) to +0.5% relative to the nominal Pixel Clock frequency value listed in the Video Timing table referenced above (under Requirement), then FAIL.

- 6 If any of the measured values do not exactly match one half of the corresponding values listed for Htotal, Hactive, Hfront, Hsync, and Hback in the Video Timing table referenced above (under Requirement) for the Video Timing indicated by PB4 of the AVI InfoFrame, then FAIL.

(NOTE: all horizontal timing is reduced by half including the Htotal, Hactive, Hblank, Hfront, Hsync, and Hback parameters)
- 7 If any of the measured values do not exactly match the corresponding values listed for Vtotal, Vactive, Vfront, Vsync, and Vback in the Video Timing table referenced above (under Requirement) for the Video Timing indicated by PB4 of the AVI InfoFrame, then FAIL.
- 8 If any of the measured Hsync and Vsync polarities do not match the corresponding values listed in the Video Timing table referenced above (under Requirement) for the Video Timing indicated by PB4 of the AVI InfoFrame, then FAIL.
- 9 If the leading edges of Hsync and Vsync are not perfectly aligned to the exact Pixel (i.e. + or - 0 Pixels), then FAIL.
- 10 Program the EDID Emulator to reveal an EDID containing the following and repeat steps 4 to 9 above:
 - 10.1 Video Data Block with SVDs for 96, 97, 101, 102, 106 and 107 (NOTE: YCbCr BCR 4:2:0 Video Data Block shall be removed).
 - 10.2 YCbCr 4:2:0 Capability Map Data Block with a Capability Bit Map, where the bits corresponding to SVDs for 96, 97, 101, 102, 106 and 107 are set (=1).

Vendor Specific Test Procedure

Test Equipment

A variety of equipment is needed for testing HDMI products. Each piece is authorized and included by name in this Compliance Test Specification. This section describes the Quantum Data test equipment.

HDMI Protocol Analyzer module

The Quantum Data 980 HDMI Protocol Analyzer module can be installed in any of the 980 series Advanced Test Platforms. This 980 HDMI Protocol Analyzer module serves the generic test functions called out in the HDMI 2.0 Generic CTS. Refer to the table below:

Item	Quantum Data Equipment	
1	980 Advanced Test Platform series:	
	Equipped with:	980 HDMI Protocol Analyzer module
		HDMI CTS 2.0 Compliance Test Package #1

980 HDMI Protocol Analyzer Module with 980 Series Platform Configurations

The figures below show depictions of the 980 HDMI Protocol Analyzer module equipped in various 980 series platforms. **Note:** Card positioning may vary depending on configuration.



Current 980 HDMI Protocol Analyzer board rev.



Previous 980 HDMI Protocol Analyzer board rev.



Source TMDS Pixel Encoding

Test ID HF1-33 - Source Video Timing - YCbCr 4:2:0 Tests

1. Objective

Confirm that a YCbCr 4:2:0 Pixel encoding-capable source DUT outputs the correct YCbCr 4:2:0 timings.

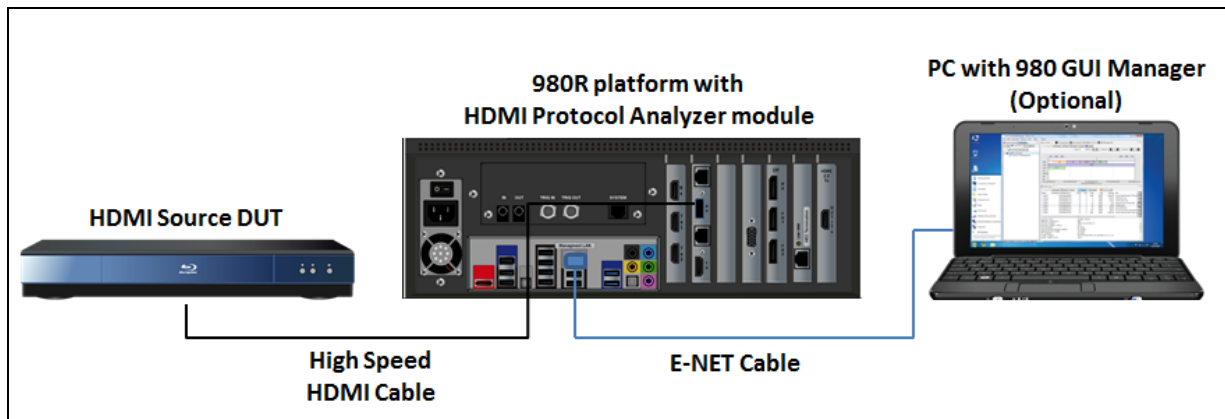
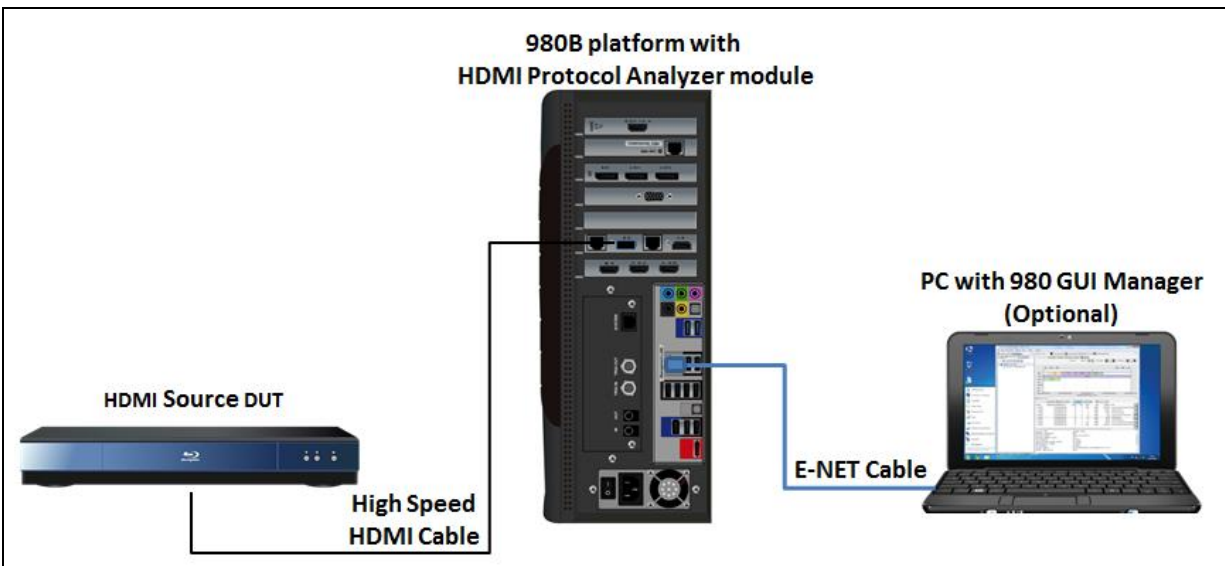
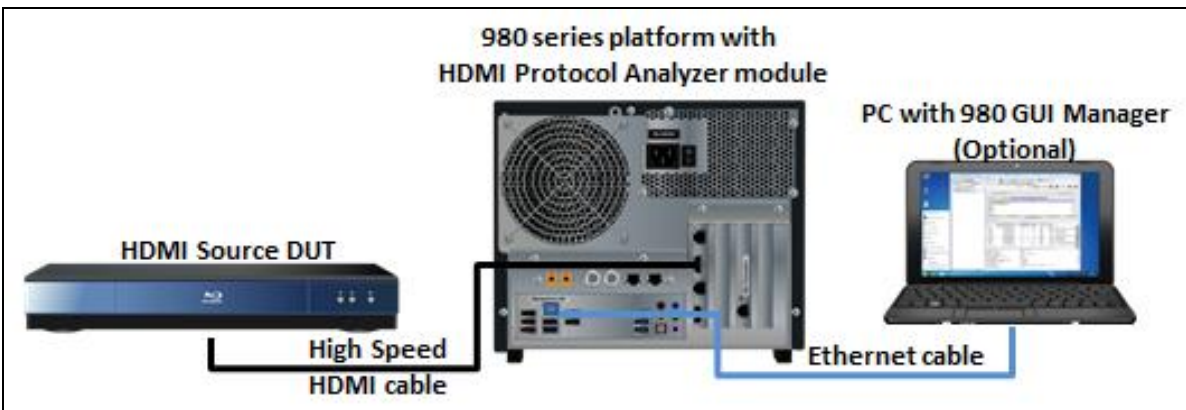
2. Test Overview

This test is run for one YCbCr 4:2:0 compliant format timing with two EDID configurations. The 980 HDMI Protocol Analyzer's Compliance Test application automatically provisions the EDIDs during the test to facilitate the source's outputting of the appropriate YCbCr 4:2:0 format. The Pass/Fail criteria is assessed by the application with no human examination required.

3. Procedure

Use the following procedure to conduct this test.

- 1 Connect Source DUT to the Quantum Data 980 HDMI Protocol Analyzer at the module's port labeled Rx. Use a High Speed HDMI cable. Refer to the figures below for reference.



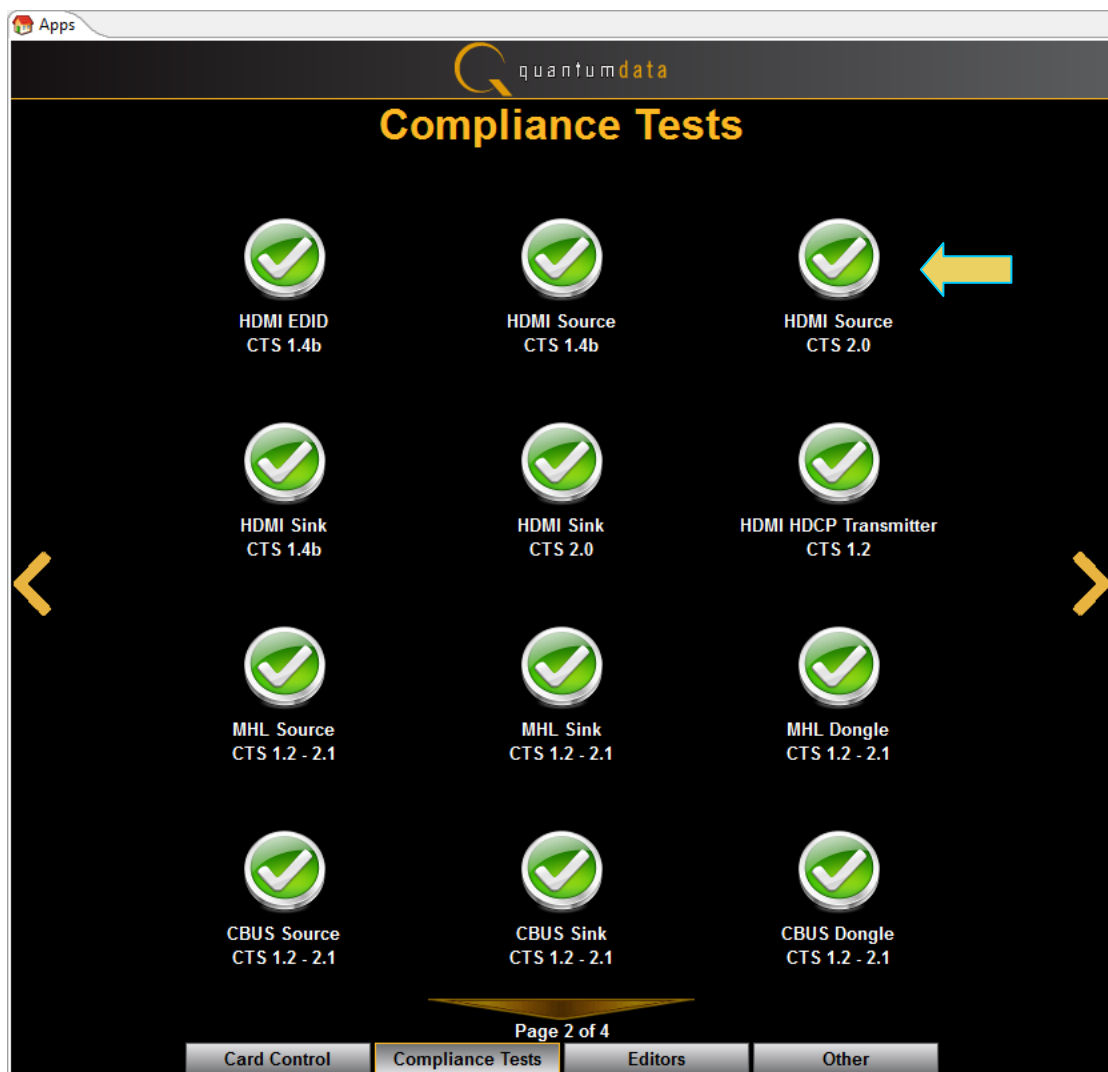
- 2 Operate the Source DUT to output a YCbCr 4:2:0 Pixel encoded signal at a Video Format for which it supports YCbCr 4:2:0 transmission.

- 3 Use Quantum Data 980 Embedded Manager GUI (touchscreen) or invoke Quantum Data 980 External Manager GUI (Windows application).

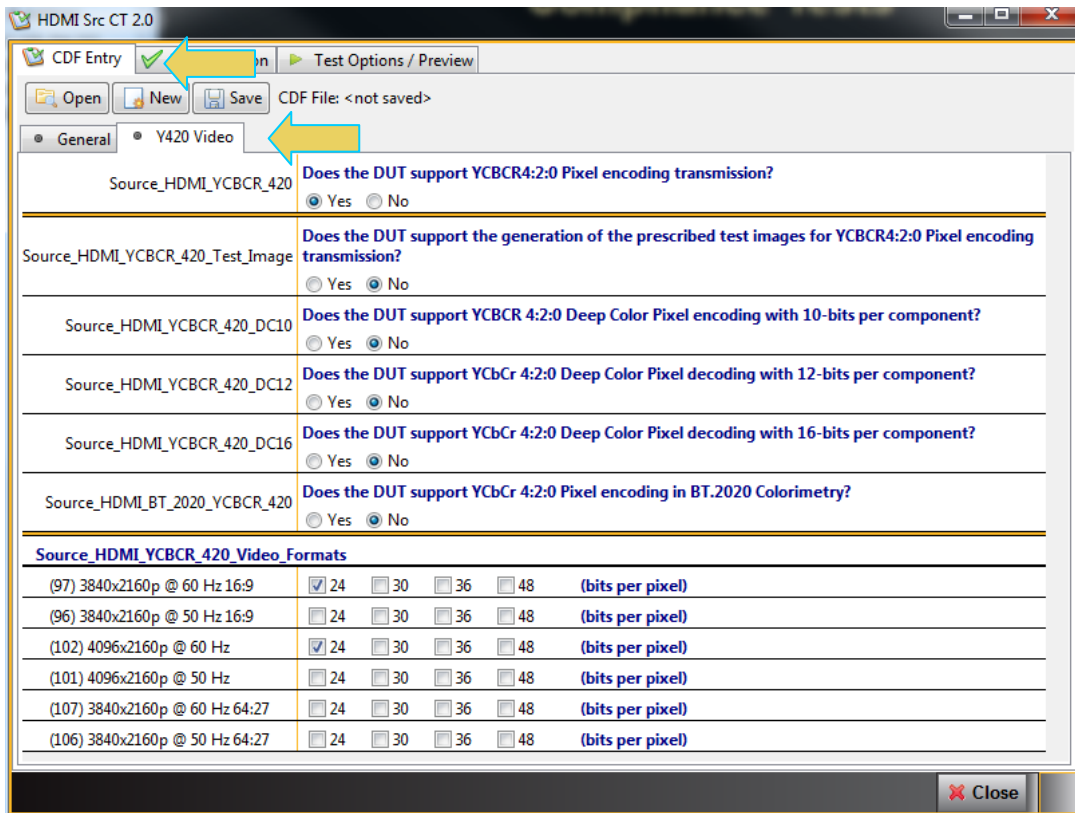
Note: You will not need to connect the PC shown in the figures above if you are running the compliance test through the 980's embedded display. The PC running the 980 HDMI Protocol Analyzer module's compliance test application is connected to the 980 through a standard Ethernet cable.

- 4 Complete the following steps:

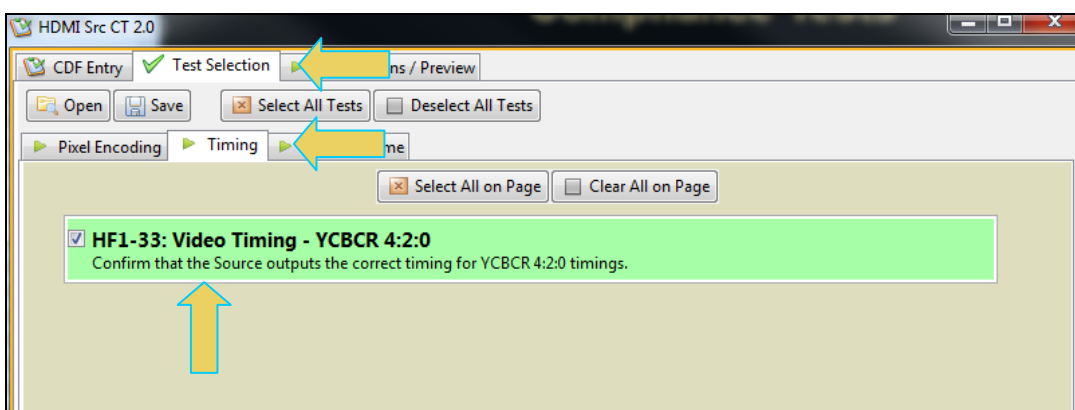
- 4.1 Click on the HDMI Source CTS 2.0 icon in the Compliance Tests page of the Apps panel.



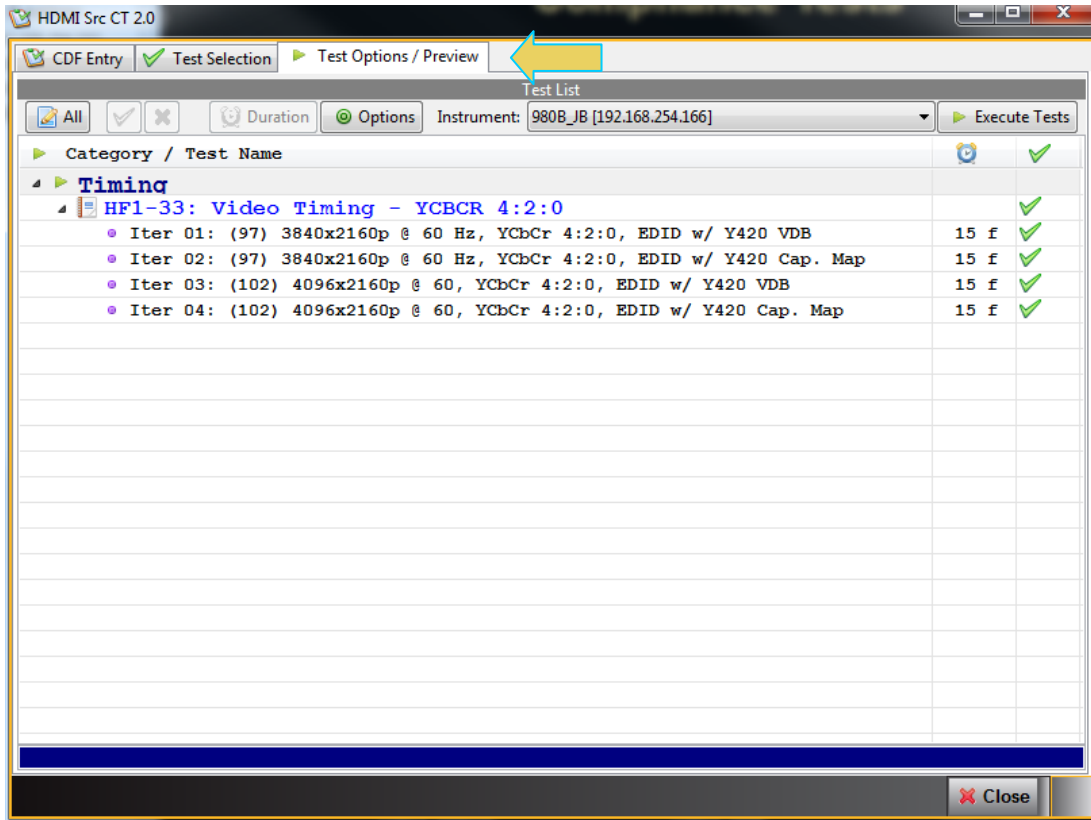
- 4.2 Navigate to the CDF tab if not already there. If there is a saved CDF file, then click on Open and select it. Otherwise, enter the DUT's CDF information for the General sub tab and the Y420 sub tab and optionally click on Save button to save the CDF.



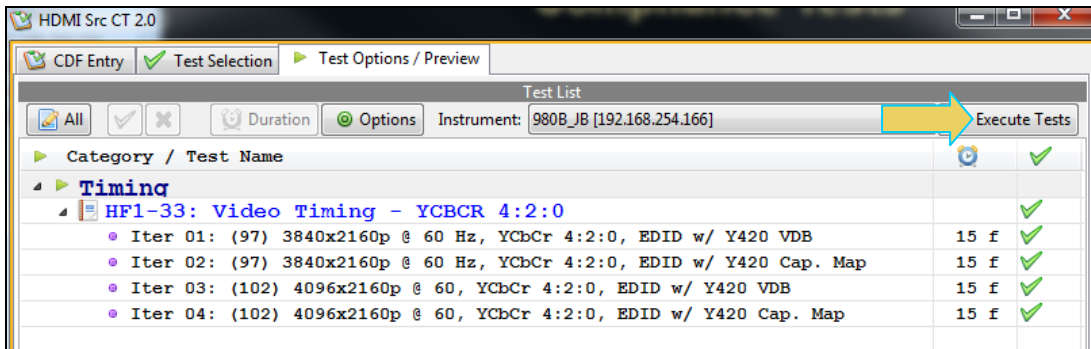
- 4.3 Click on the Test Selection tab, and select the HF1-33 Video Timing - YCbCr 4:2:0 Test. Refer to the screen example below.



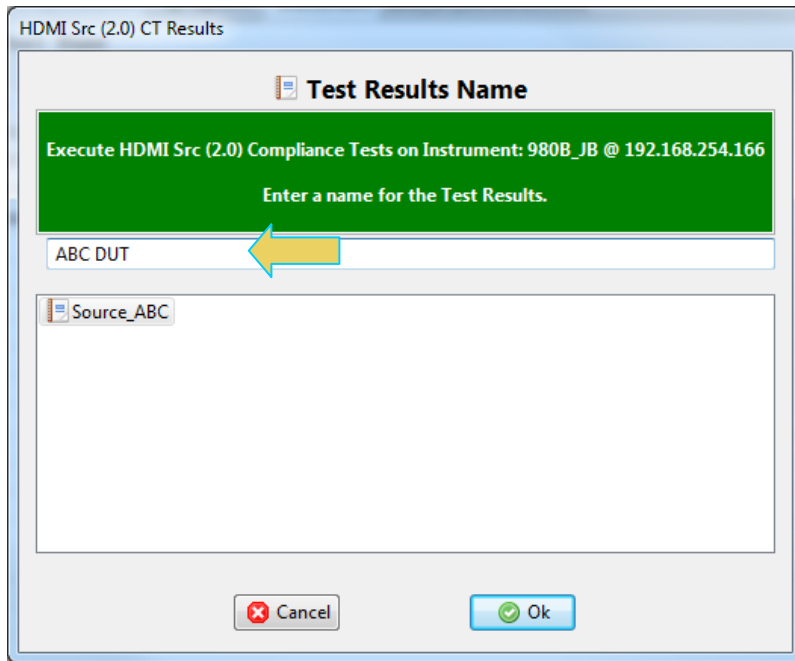
- 4.4 Click on Test Options / Preview tab and review the list of tests. Refer to the sample screen below.



4.5 Click on Execute tests activation button to initiate the test. Refer to the sample screen below.



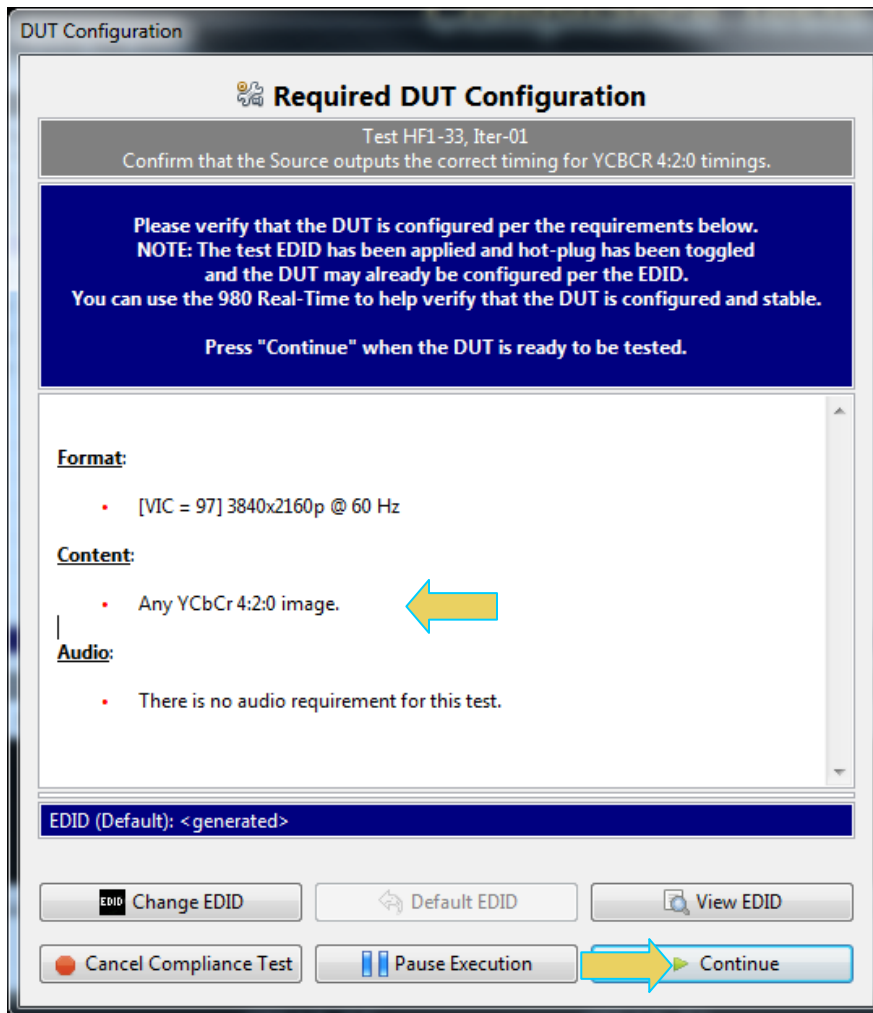
Note: You will be prompted with a dialog box to assign a name to the test results. Refer to the screen example below:



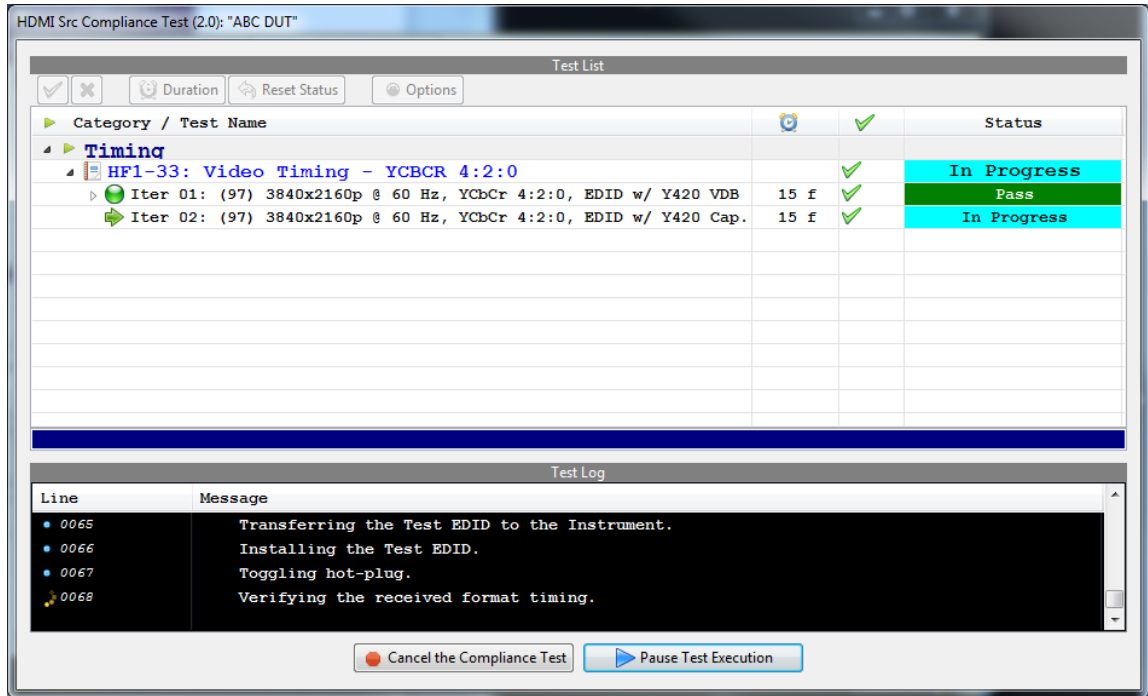
Enter a name and the test will begin.

A Test Window will appear (below) indicating the progress of the test.

You will be prompted with a dialog box informing you of the requirements of the source DUT. Verify that the source is outputting the required HDMI format and pixel encoding and press Continue to run the test.



- 4.6 Follow the prompts issued by the 980 HDMI Protocol Analyzer's compliance test application.



- 5 If the 980 HDMI Protocol Analyzer's compliance test application reports PASS, then PASS.
If the 980 HDMI Protocol Analyzer's compliance test application reports FAIL, then FAIL.

When the test is complete a Test Results screen appears. Refer to the screen example below.

