

High-Definition Multimedia Interface

Version 2.0

Quantum Data MOI v1.0

Test ID: HF2-23

April 11, 2014

Preface

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1.0 April 11, 2014 - Initial Release.

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Contact Information

The URL for the HDMI Forum web site is: <http://www.hdmiforum.org/>

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Introduction

This document provides a set of Method of Implementation for test method described in HDMI Compliance Test Specification Version 2.0 (HDMI CTS 2.0). HDMI Forum created HDMI CTS 2.0 to specify a set of tests that should be performed to verify features described in HDMI Specification Version 2.0.

Scope

This document provides testing procedures for HDMI CTS 2.0 Test ID HF2-23: “Sink Pixel Decoding – YCBCR 4:2:0”. The procedure below deals with single resolution and only one Test ID is considered at a time.

References Document

Normative References

High-Definition Multimedia Interface Specification Version 1.4b, October 11, 2011.
HDMI Compliance Test Specification Version 1.4b, October 11, 2011.
High-Definition Multimedia Interface Specification Version 2.0, August, 2013.
HDMI Compliance Test Specification Version 2.0.

Informative Reference

No additional informative references.

Test ID HF2-23: Sink Pixel Decoding – YC_BC_R 4:2:0

Objective

Confirm that a YC_BC_R 4:2:0 Pixel encoding-capable Sink DUT supports YC_BC_R 4:2:0 Pixel decoding and signaling.

Table 8-27 Sink Pixel Decoding – YC_BC_R 4:2:0 Requirements

Reference	Requirement
[HDMI 2.0: 7.1]	“Figure 7-1 shows the signal mapping and timing for transferring YC _B C _R 4:2:0 Pixel encoded progressive video data across HDMI. The two horizontally successive 8-bit Y components are transmitted in TMDS Channel 1 and 2, respectively in order. The 8-bit CB or CR components are alternately transmitted in TMDS Channel 0, line by line.” See Figure 7-1, which shows the mapping between lines, Pixels, and TMDS Channel data.”
[HDMI 2.0: 7.1]	“When transmitting a Video Format listed in Table 7-1, Source Devices may utilize the YC _B C _R 4:2:0 Pixel Encoding method defined in this section with the VIC set to the corresponding value.”

Capability(s)

The Source DUT supports at least one Video Format in YC_BC_R 4:2:0 color sampling mode.

Test Equipment

Item	Generic Equipment	Vendor Specific Equipment	Quantity
1	DDC Slave Emulator	980 Advanced Test Platform series:	1
2	EDID Emulator	980 HDMI Protocol Analyzer module	1
3	297MHz Video Protocol Analyzer w/ YC _B C _R 4:2:0 option	HDMI CTS 2.0 Compliance Test Package #1	1

Generic Procedure

- 1 If the CDF field Sink_HDMI_YC_BC_R_420 is "N", then SKIP this test.
- 2 Connect the Sink DUT to the DDC Master and EDID Analyzer.
- 3 Connect the Sink DUT to the 297MHz Video Generator.
- 4 Turn on the Sink DUT, have the DDC Master output +5V Power and read the Sink DUT's EDID in response to a hot-plug.
 - 4.1 If the Hot Plug Detect signal is not received or the EDID is unreadable, then FAIL.

- 5 Connect the Sink DUT to the 297MHz Video Generator.
- 6 For each supported 24-bit YCBCR 4:2:0 Pixel encoded Video Format supported in the Sink DUT's EDID (see CDF field Sink_HDMI_YCBCR_420_Video_Formats) do the following:
 - 6.1 Operate the 297MHz Video Generator to output the following:
 - 6.1.1 A test image according to Appendix G
 - 6.1.2 AVI InfoFrame with:
 - 6.1.2.1 Y2, Y1, Y0 = 011.
 - 6.1.2.2 VIC7...0, depending on the Video Format being evaluated.
 - 6.2 Operate the 297MHz Video Generator to output the specified Pixel clock frequency -0.5% (or -0.6% when the frame rate is 60Hz).
 - 6.3 Perform visual check as per the following steps (NOTE: any equivalent test image/procedure is permitted).
 - 6.3.1 If the image/video appears to be distorted or disturbed, then FAIL.
 - 6.3.2 If the color bars in the upper half of the active video are not in the order described in Appendix G, then FAIL.
 - 6.3.3 If the black and white bars in the lower half of the active video are not evenly spaced, then FAIL.
 - 6.3.4 If the black and white bars in the lower half of the active video contain a strong blue or red tint when examined at close range, then FAIL.
 - 6.4 Operate the 297MHz Video Generator to output a YCBCR 4:2:0 Pixel encoded signal with specified Pixel clock frequency +0.5% and repeat step 6.3.

Vendor Specific Test Procedure

Test Equipment

A variety of equipment is needed for testing HDMI products. Each piece is authorized and included by name in this Compliance Test Specification. This section describes the Quantum Data test equipment.

HDMI Protocol Analyzer module

The Quantum Data 980 HDMI Protocol Analyzer module can be installed in any of the 980 series Advanced Test Platforms. This 980 HDMI Protocol Analyzer module serves the generic test functions called out in the HDMI 2.0 Generic CTS. Refer to the table below:

Item	Quantum Data Equipment	
1	980 Advanced Test Platform series:	
	Equipped with:	980 HDMI Protocol Analyzer module
		HDMI CTS 2.0 Compliance Test Package #1

980 HDMI Protocol Analyzer Module with 980 Series Platform Configurations

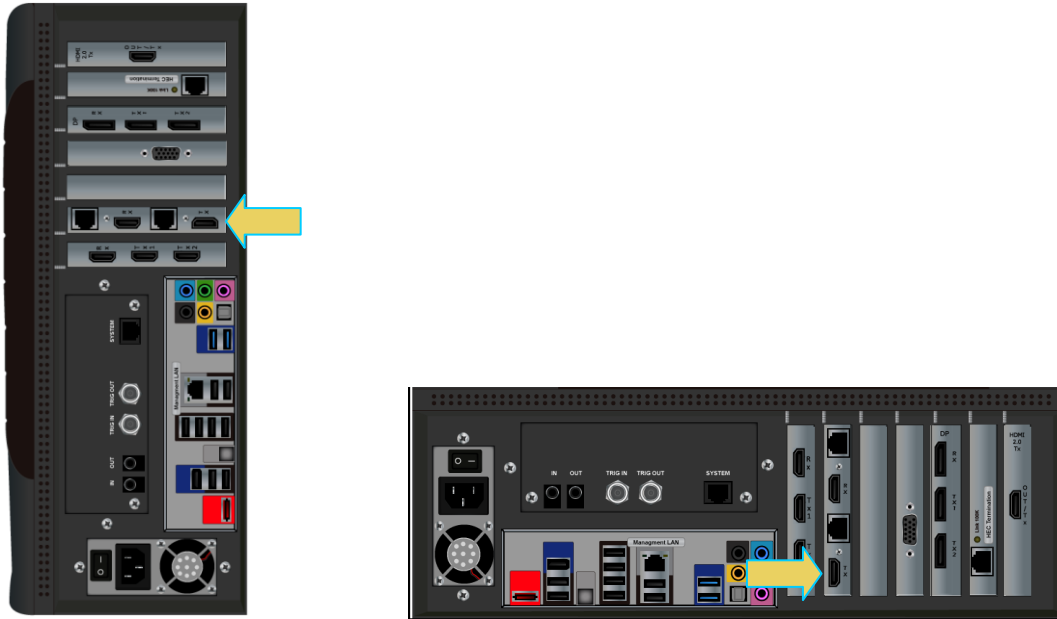
The figures below show depictions of the 980 HDMI Protocol Analyzer module equipped in various 980 series platforms. **Note:** Card positioning may vary depending on configuration.



Current 980 HDMI Protocol Analyzer board rev.



Previous 980 HDMI Protocol Analyzer board rev.



Sink Pixel Decoding

Test ID HF2-23 - Sink Pixel Decoding YCbCr 4:2:0 Tests

1. Objective

Confirm that a YCbCr 4:2:0-capable sink DUT supports the Pixel Decoding - YCbCr 4:2:0 Test.

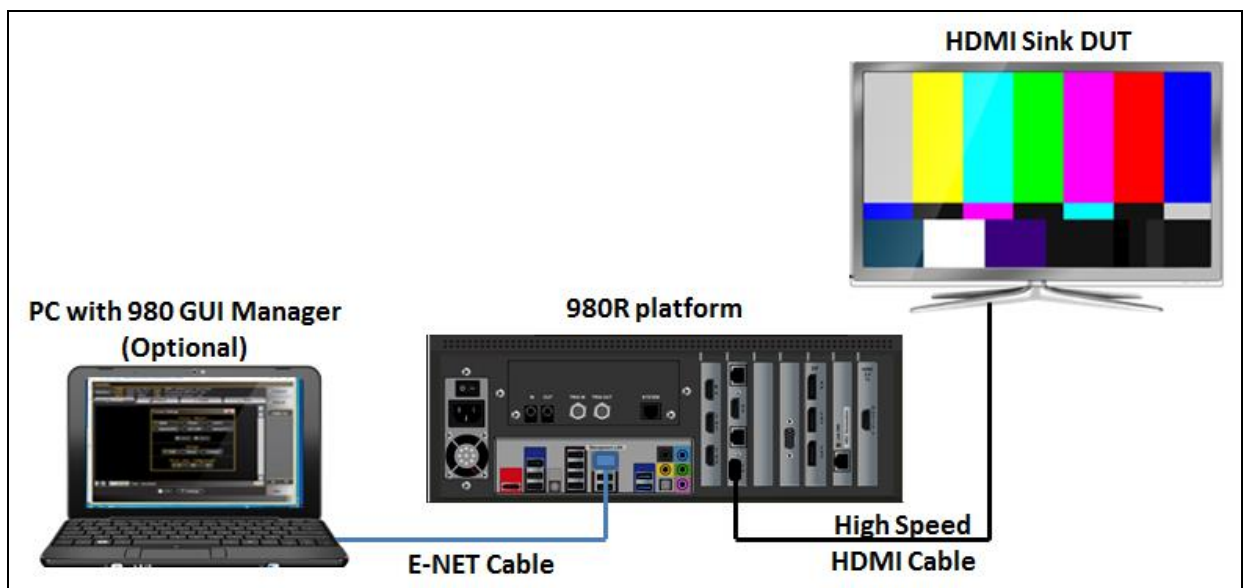
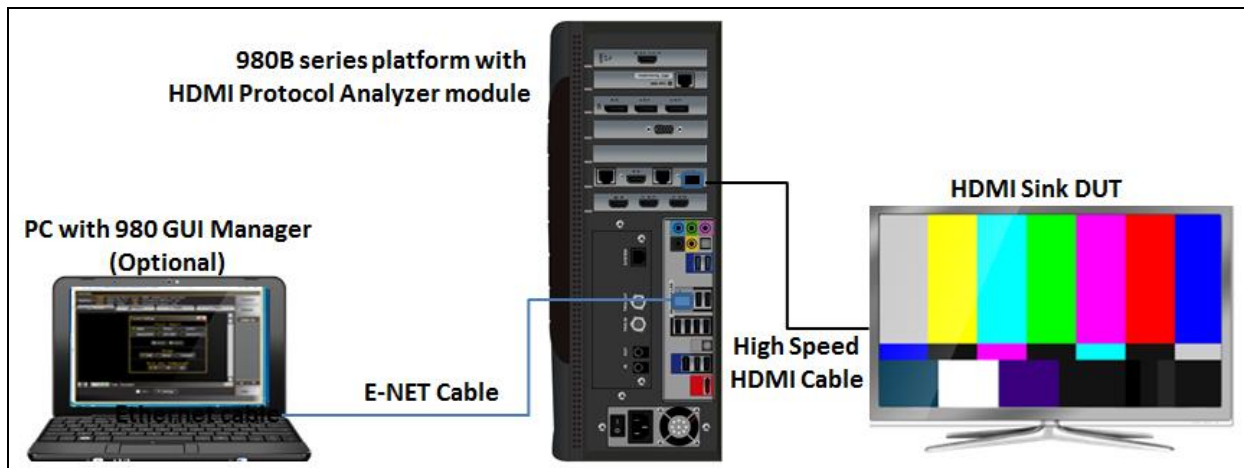
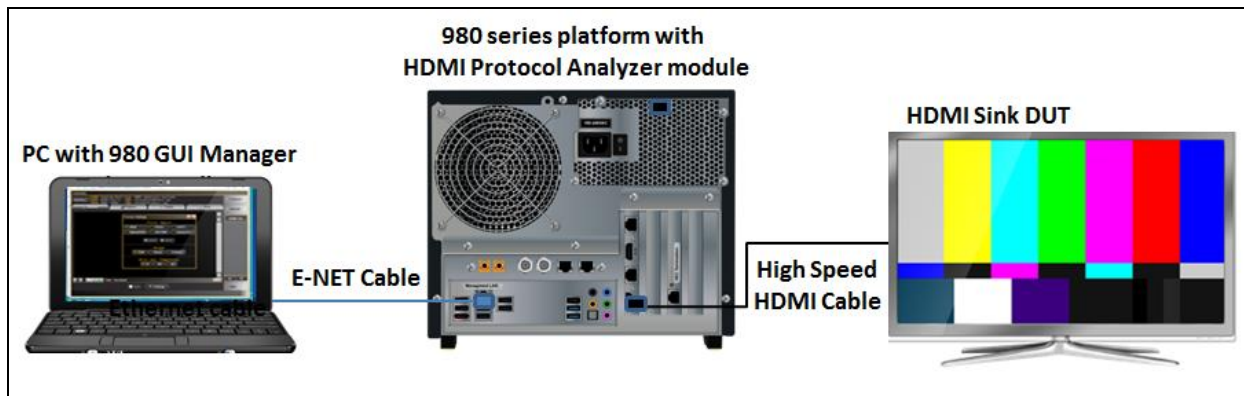
2. Test Overview

This test is run for all YCbCr 4:2:0 supported video format timings using the colorbar test image specified in the HDMI 2.0 CTS. The 980 HDMI Protocol Analyzer's Compliance Test application automatically transmits the required video timings in sequence. The Pass/Fail criteria is assessed by human examination of the test pattern displayed on the Sink DUT.

3. Procedure

Use the following procedure to conduct this test.

1. Connect Sink DUT to the Quantum Data 980 HDMI Protocol Analyzer module Use a High Speed HDMI cable. Refer to the figures below for reference.

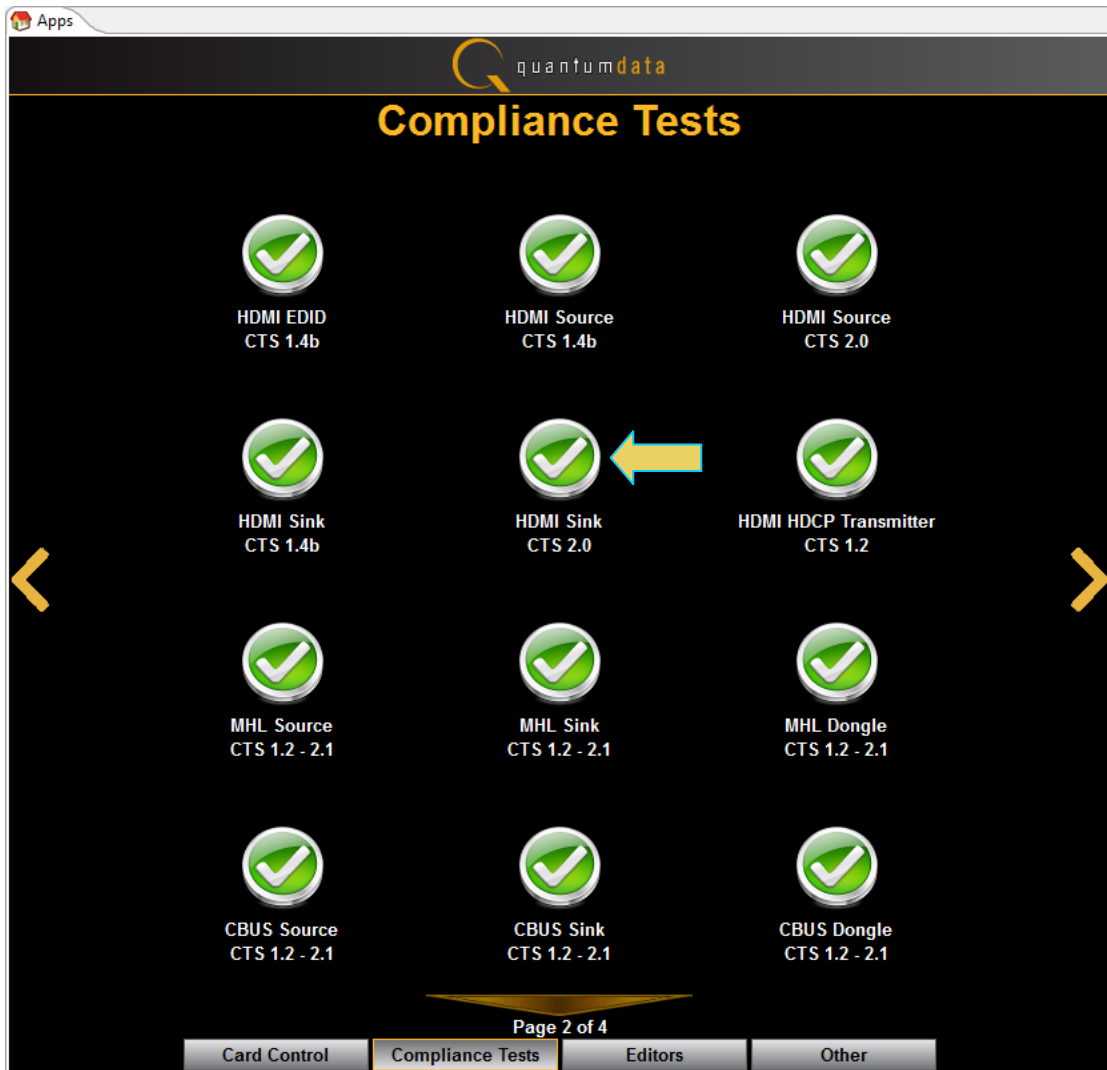


2. Use Quantum Data 980 Embedded Manager GUI (touchscreen) or invoke Quantum Data 980 External Manager GUI (Windows application).

Note: You will not need to connect the PC shown in the figures above if you are running the compliance test through the 980's embedded display. The PC running the 980 HDMI Protocol Analyzer module's compliance test application is connected to the 980 through a standard Ethernet cable.

3. Complete the following steps:

- 3.1 Click on the HDMI Sink CTS 2.0 icon in the Compliance Tests page of the Apps panel.



- 3.2 Navigate to the CDF tab if not already there. Complete the General sub tab and the Y420 sub tab in the CDF. If there is a saved CDF file, then click on Open and select it. Otherwise, enter the DUT's CDF information and click on Save to save the CDF. Refer to the screen example below.

HDMI Sink CT 2.0

CDF Entry Test Selection Test Options / Preview

Open New Save CDF File: <not saved>

General 21:9 (64:27) Video Y420 Video Other

Sink_HDMI_YCBCR_420 Does the DUT support YCbCr 4:2:0 Pixel decoding?

☒ Yes ☐ No

Sink_HDMI_YCBCR_420_DC10 Does the DUT support YCbCr 4:2:0 Deep Color Pixel decoding with 10-bits per component?

☐ Yes ☒ No

Sink_HDMI_YCBCR_420_DC12 Does the DUT support YCbCr 4:2:0 Deep Color Pixel decoding with 12-bits per component?

☐ Yes ☒ No

Sink_HDMI_YCBCR_420_DC16 Does the DUT support YCbCr 4:2:0 Deep Color Pixel decoding with 16-bits per component?

☐ Yes ☒ No

Sink_HDMI_BT_2020_YCBCR_420 Does the DUT support YCbCr 4:2:0 Pixel encoding in BT.2020 Colorimetry?

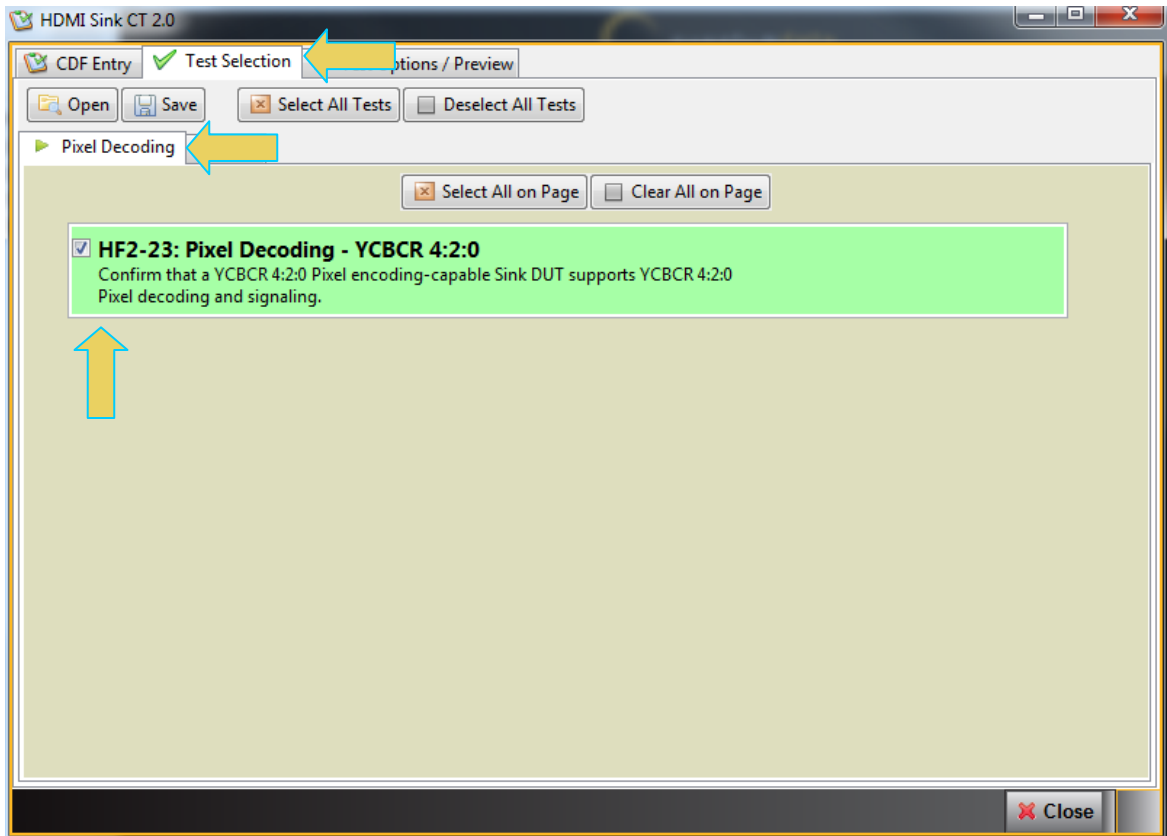
☐ Yes ☒ No

Sink_HDMI_YCBCR_420_Video_Formats

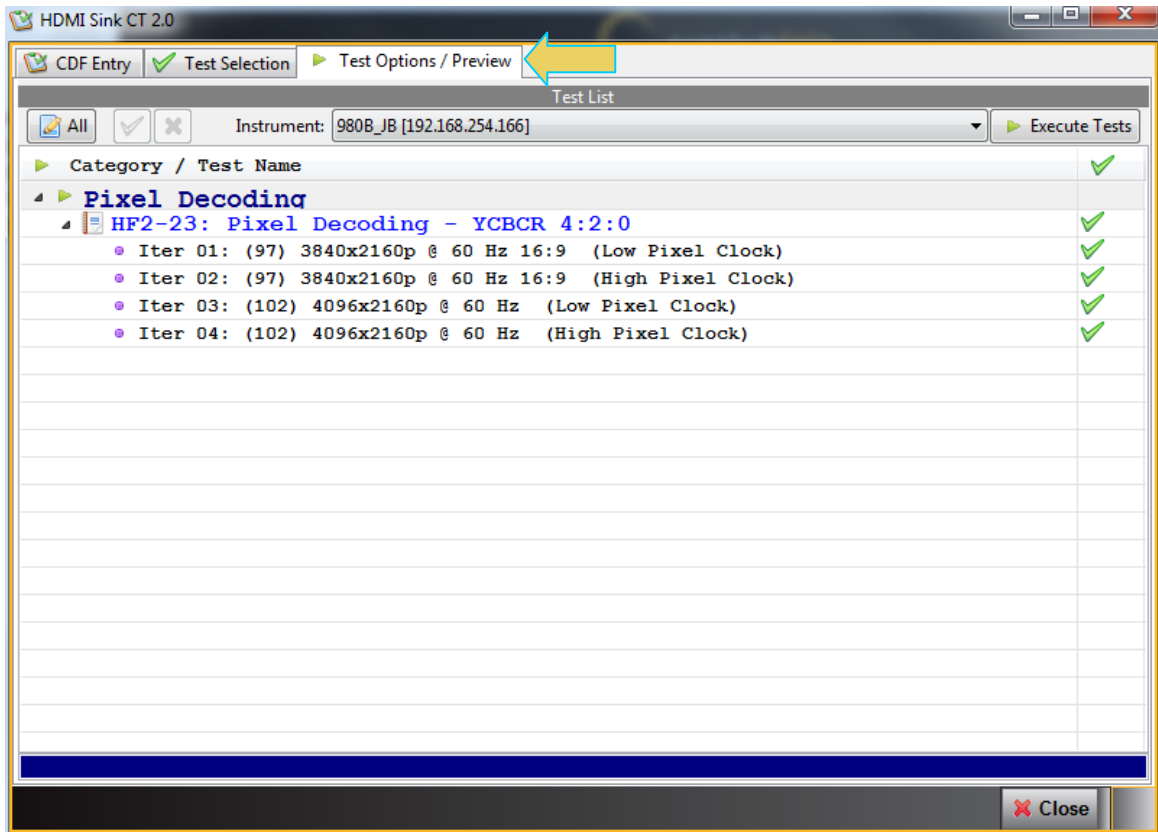
(97) 3840x2160p @ 60 Hz 16:9	<input checked="" type="checkbox"/> 24	<input type="checkbox"/> 30	<input type="checkbox"/> 36	<input type="checkbox"/> 48	(bits per pixel)
(96) 3840x2160p @ 50 Hz 16:9	<input type="checkbox"/> 24	<input type="checkbox"/> 30	<input type="checkbox"/> 36	<input type="checkbox"/> 48	(bits per pixel)
(102) 4096x2160p @ 60 Hz	<input checked="" type="checkbox"/> 24	<input type="checkbox"/> 30	<input type="checkbox"/> 36	<input type="checkbox"/> 48	(bits per pixel)
(101) 4096x2160p @ 50 Hz	<input type="checkbox"/> 24	<input type="checkbox"/> 30	<input type="checkbox"/> 36	<input type="checkbox"/> 48	(bits per pixel)
(107) 3840x2160p @ 60 Hz 64:27	<input type="checkbox"/> 24	<input type="checkbox"/> 30	<input type="checkbox"/> 36	<input type="checkbox"/> 48	(bits per pixel)
(106) 3840x2160p @ 50 Hz 64:27	<input type="checkbox"/> 24	<input type="checkbox"/> 30	<input type="checkbox"/> 36	<input type="checkbox"/> 48	(bits per pixel)

Close

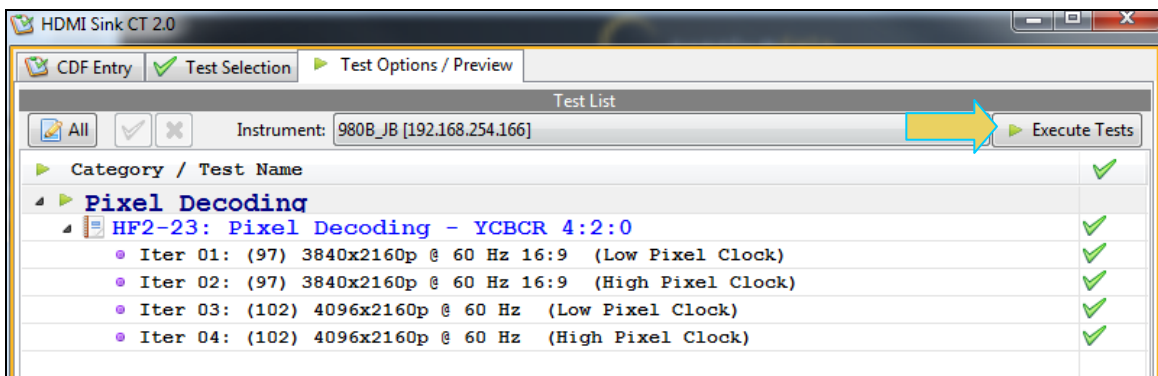
- 3.3 Click on the Test Selection tab, and select HF2-23 Sink Pixel Decoding - YCbCr 4:2:0 Test. Refer to the screen example below.



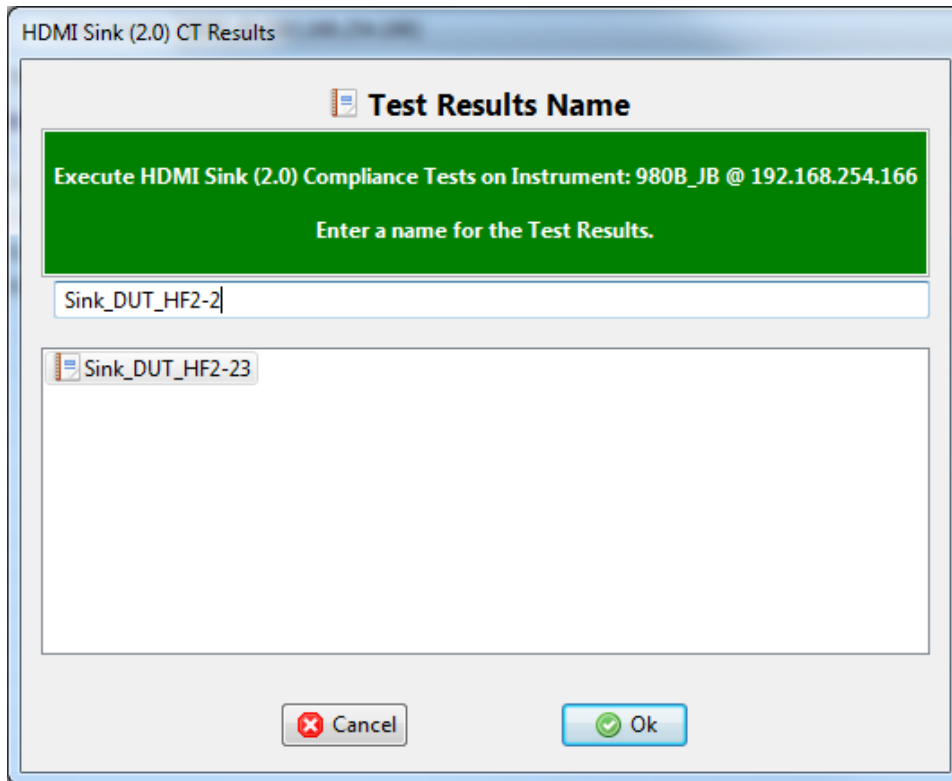
- 3.4 Click on Test Options / Preview tab and review the list of tests. Refer to the screen example below.



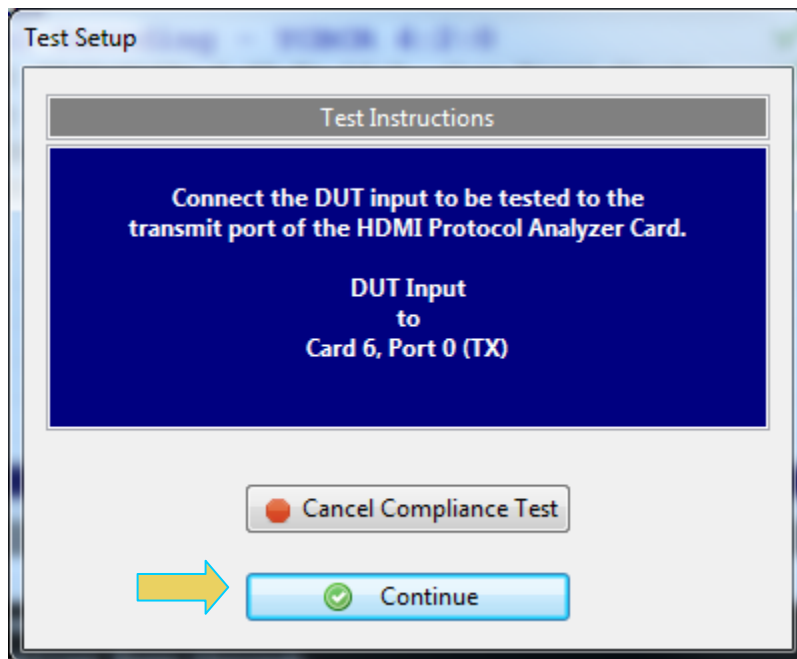
- 3.5 Click on the Execute tests activation button to initiate the test.



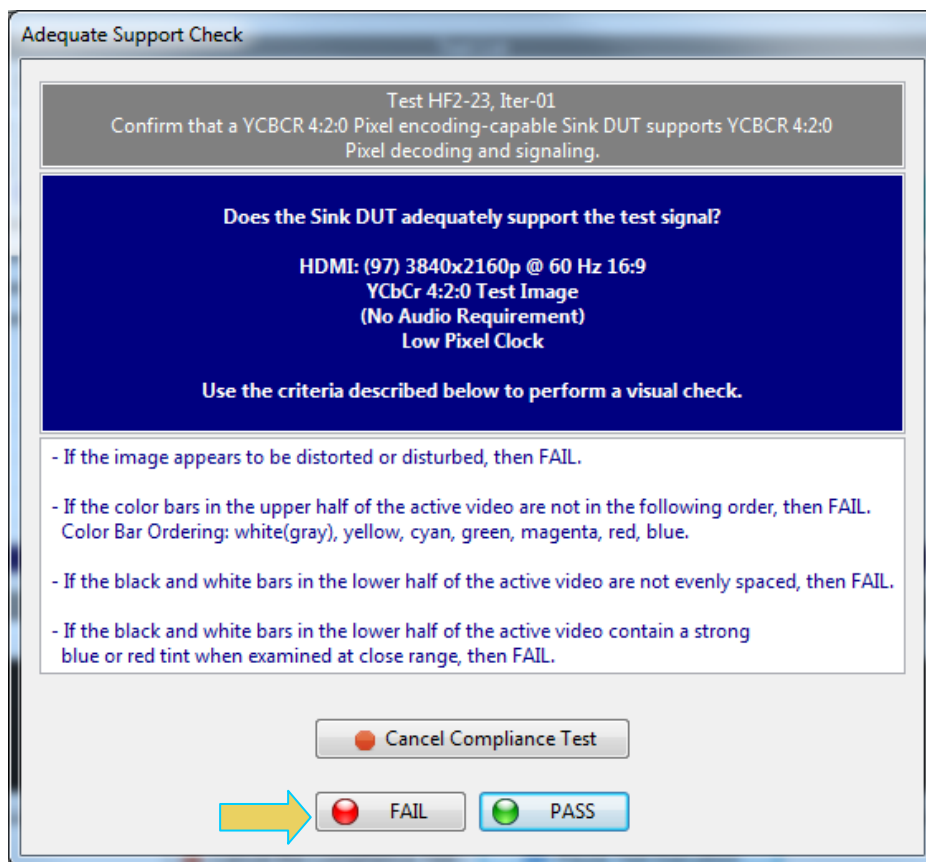
A dialog box will appear enabling you to enter the name for the test results. Refer to the screen example below.



Note: You will be prompted with a dialog box describing the test setup. Verify the setup and then click on the Continue button on the dialog box. Refer to the screen example below.



4. Monitor the Compliance test application for instructions and monitor the Sink DUT display to assess PASS or FAIL when prompted. Refer to the sample screen example below. Click on the Pass or Fail button depending on the image displayed the sink DUT.



Note: The test will be repeated for all YCBCR 4:2:0 video format timings marked in the CDF.

5. If the 980 HDMI Protocol Analyzer's compliance test application reports PASS, then PASS.
If the 980 HDMI Protocol Analyzer's compliance test application reports FAIL, then FAIL.

When the test is completed a Test Results Viewer screen will appear.

