

High-Definition Multimedia Interface

Version 2.0

Quantum Data MOI v1.0

Test ID: HF1-31

April 11, 2014

Preface

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Document Revision History

1.0 April 11, 2014 - Initial Release.

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Contact Information

The URL for the HDMI Forum web site is: <http://www.hdmiforum.org/>

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Introduction

This document provides a set of Method of Implementation for test method described in HDMI Compliance Test Specification Version 2.0 (HDMI CTS 2.0). HDMI Forum created HDMI CTS 2.0 to specify a set of tests that should be performed to verify features described in HDMI Specification Version 2.0.

Scope

This document provides testing procedures for HDMI CTS 2.0 Test ID HF1-31: “Source Pixel Encoding – YCBCR 4:2:0 – TMDS Pixel Encoding.” The procedure below deals with single resolution and only one Test ID is considered at a time.

References

Normative References

High-Definition Multimedia Interface Specification Version 1.4b, October 11, 2011.
HDMI Compliance Test Specification Version 1.4b, October 11, 2011.
High-Definition Multimedia Interface Specification Version 2.0, August, 2013.
HDMI Compliance Test Specification Version 2.0.

Informative Reference

No additional informative references.

Test ID HF1-31: Source Pixel Encoding – YC_BC_R 4:2:0 – TMDS Pixel Encoding

Objective

Confirm that a YC_BC_R 4:2:0 Pixel encoding-capable Source DUT outputs correct YC_BC_R 4:2:0 Pixel encoding and signaling. In the case where a Source DUT can output standardized test images, then ensure the proper position of the Pixels and the order of the color-component data of the test Pixels with fully saturated (extreme-value) color-components. NOTE: Only the spatial /ordering relationship of Pixels/components is evaluated by this test. Therefore, fine color level variations (perhaps due to color/level processing) will not produce false-positive FAIL indications.

Table 7-31 Source TMDS Pixel Encoding – YC_BC_R 4:2:0 – TMDS Pixel Encoding Requirements

Reference	Requirement
[HDMI 2.0: 7.1]	<p>“Figure 7-1 shows the signal mapping and timing for transferring YC_BC_R 4:2:0 Pixel encoded progressive video data across HDMI. The two horizontally successive 8-bit Y components are transmitted in TMDS Channel 1 and 2, respectively in order. The 8-bit C_B or C_R components are alternately transmitted in TMDS Channel 0, line by line.”</p> <p>“A Source shall not send a Video Format with YC_BC_R 4:2:0 Pixel Encoded data to a Sink that does not indicate support for such format in the Y420C MDB (YC_BC_R 4:2:0 Capability Map Data Block) or Y420V DB (YC_BC_R 4:2:0 Video Data Block), as defined in CEA-861-F Section 7.5.10 and 7.5.11.”</p>

Capability(s)

The Source DUT supports at least one Video Format in YC_BC_R 4:2:0 color sampling mode.

Test Equipment

Item	Generic Equipment	Vendor Specific Equipment	Quantity
1	DDC Slave Emulator	980 Advanced Test Platform series: 980 HDMI Protocol Analyzer module HDMI CTS 2.0 Compliance Test Package #1	1
2	EDID Emulator		1
3	297MHz Video Protocol Analyzer w/ YC _B C _R 4:2:0 option		1

Generic Procedure

- If the CDF field Source_HDMI_YC_BC_R_420 is “N”, then SKIP this test.
- Connect the Source DUT to a 297MHz Video Protocol Analyzer with the DDC Slave Emulator and EDID Emulator.
- Program the EDID Emulator to reveal an EDID containing the following:

- 3.1 YCbCr 4:2:0 Video Data Block with:
 - 3.1.1 YCbCr 4:2:0-only with SVDs = 96, 97, 101, 102, 106 and 107 (NOTE: If a regular Video Data Block is also present, then it shall not contain SVDs = 96, 97, 101, 102, 106, or 107)
 - 3.1.2 No HF-VSDB shall be included.
- 4 Operate the Source DUT to output a 24-bit/Pixel YCbCr 4:2:0 Pixel encoded signal at a Video Format for which it supports 4:2:0 transmission (see CDF field Source_HDMI_YCbCr_420), repeating all of the following tests for at least one of the supported Video Formats: The content of the video signal being output from the DUT shall contain visible differentiation of colors/grays (e.g., a natural scene with sufficient color variation).
- 5 If the DUT supports the generation of test image(s) (see the CDF field Source_HDMI_YCbCr_420, operate it to generate these images one by one (see Source_HDMI_YCbCr_420, for images to be used). The TE checks the video signal as received from the DUT.
 - 5.1 Verify that the C_R value is greater than the C_B value in the red color bar. If C_R is less than or equal to C_B , then FAIL.
 - 5.2 Verify that the C_B value is greater than the C_R value in the blue color bar. If C_B is less than or equal to C_R , then FAIL.
 - 5.3 Verify that the Y values are in order. If the lower half of the active video area consists of vertical bars 4 Pixels wide, CONTINUE, otherwise, FAIL. (NOTE: If the Y values are not encoded in the proper order, there will be a repeated pattern of black and white bars 1 Pixel wide, followed by either a black or a white bar 2 Pixels wide).
 - 5.4 Verify that the Y values are not located in the C_B/C_R field and vice-versa, i.e. If the C_B or C_R field in the lower half of the active video contains only values in the range allowed for "Median", and the Y fields contain values not in the range allowed for "Median", then CONTINUE, otherwise, FAIL.
- 6 Decode the video signal being received from the DUT using the YCbCr 4:2:0 mapping into a visual form and perform a visual check.
- 7 If the decoded image/video appears to be distorted (e.g., The aspect ratio of the objects is wrong) or disturbed (e.g., Incorrect color), then FAIL.
- 8 Program the EDID Emulator to reveal an EDID containing the following and repeat steps 4 to 7 above:
 - 8.1 Video Data Block with SVDs for 96, 97, 101, 102, 106 and 107 (NOTE: YCbCr 4:2:0 Video Data Block shall be removed).

- 8.2 YCbCr 4:2:0 Capability Map Data Block with a Capability Bit Map, where the bits corresponding to SVDs 96, 97, 101, 102, 106 and 107 are set (=1).
- 9 Program the EDID Emulator to reveal an EDID containing the following and repeat step 4 above:
 - 9.1 As in step 8, but without YCbCr 4:2:0 Capability Map Data Block.
- 10 If the Source DUT outputs or can be operated to output a YCbCr 4:2:0 pixel encoded signal, then FAIL.

Vendor Specific Test Procedure

Test Equipment

A variety of equipment is needed for testing HDMI products. Each piece is authorized and included by name in this Compliance Test Specification. This section describes the Quantum Data test equipment.

HDMI Protocol Analyzer module

The Quantum Data 980 HDMI Protocol Analyzer module can be installed in any of the 980 series Advanced Test Platforms. This 980 HDMI Protocol Analyzer module serves the generic test functions called out in the HDMI 2.0 Generic CTS. Refer to the table below:

Item	Quantum Data Equipment	
1	980 Advanced Test Platform series:	
	Equipped with:	980 HDMI Protocol Analyzer module
		HDMI CTS 2.0 Compliance Test Package #1

980 HDMI Protocol Analyzer Module with 980 Series Platform Configurations

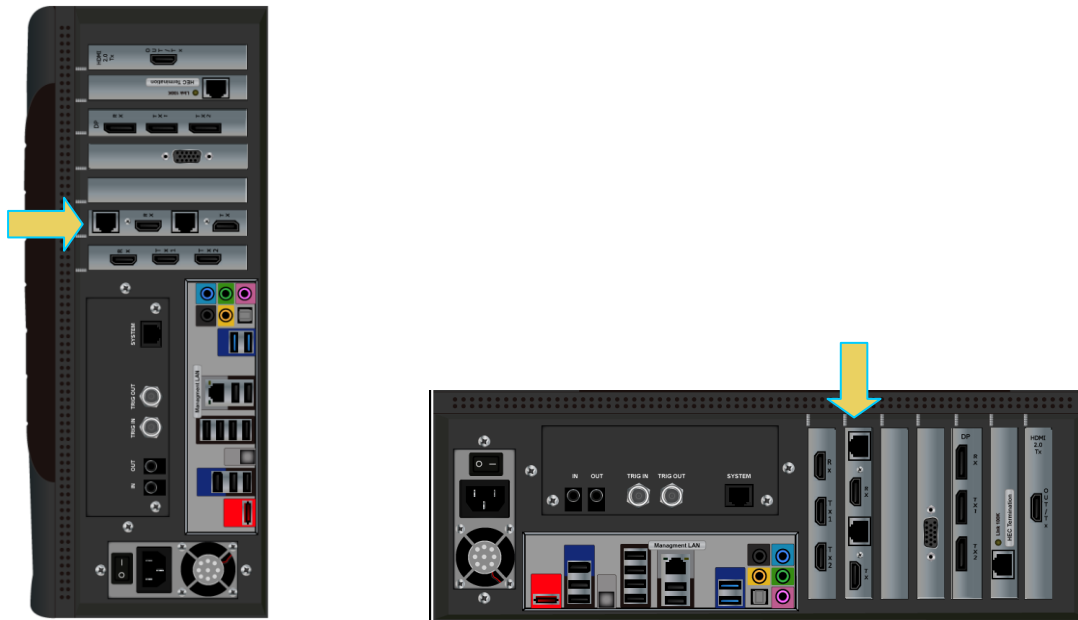
The figures below show depictions of the 980 HDMI Protocol Analyzer module equipped in various 980 series platforms. **Note:** Card positioning may vary depending on configuration.



Current 980 HDMI Protocol Analyzer board rev.



Previous 980 HDMI Protocol Analyzer board rev.



Source TMDS Pixel Encoding

Test ID HF1-31 - Source Pixel Encoding YCBCR 4:2:0 Tests

1. Objective

Confirm that a YCbCr 4:2:0 Pixel encoding-capable Source DUT outputs correct YCbCr 4:2:0 Pixel encoding and signaling. In the case where a Source DUT can output standardized test images, then ensure the proper position of the Pixels and the order of the color-component data of the test Pixels with fully saturated (extreme-value) color components. Note that only the spatial/ordering relationship of Pixels/components is evaluated by this test. Therefore, fine color level variations (perhaps due to color/level processing) will not produce false-positive FAIL indications.

2. Test Overview

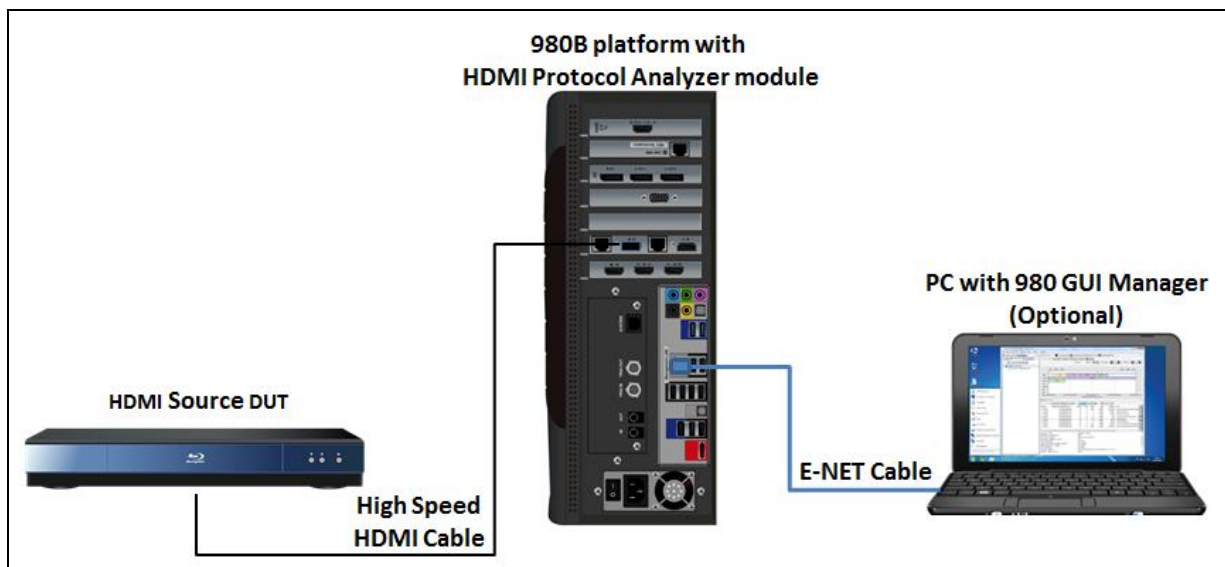
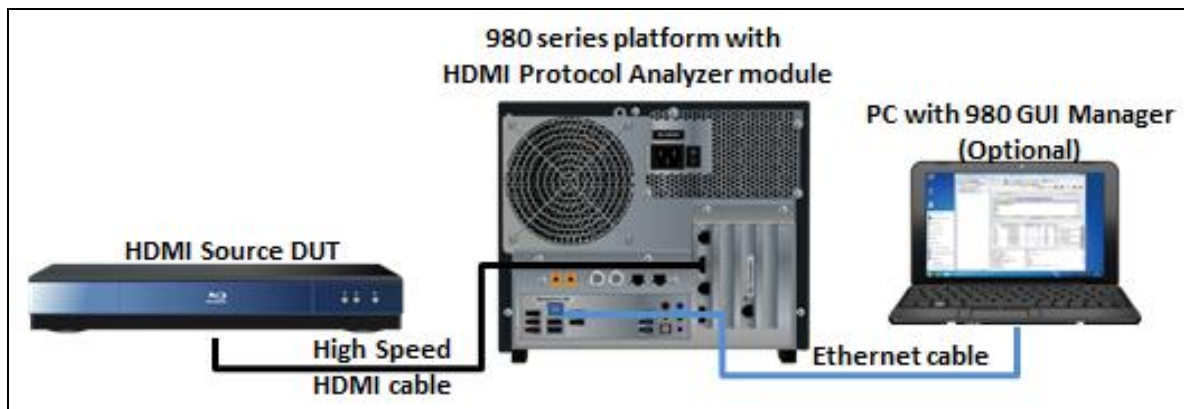
This test can be performed with or without a specific test image (YCbCr 4:2:0 Test Image). If the test image is indicated in the CDF a separate Pass/Fail assessment will be made by the compliance test application. For source DUTs that do not have the prescribed test image, the Pass/Fail results will be assessed strictly through operator examination. In this case (without the test image) an image containing visible differentiation of colors/grays (e.g., a natural scene with sufficient color variation) should be selected and output by the source DUT. Consult the HDMI Compliance Test Specification and HDMI Specification for details. This user examination of the test image is achieved through the 980's embedded display. The 980 Compliance Test application determines whether or not the Source DUT supports the specified test image from the information the user enters in the Capabilities Declaration Form (CDF) (the Source_HDMI_YCbCr_420_Test_Image parameter). The 980 Compliance Test application will

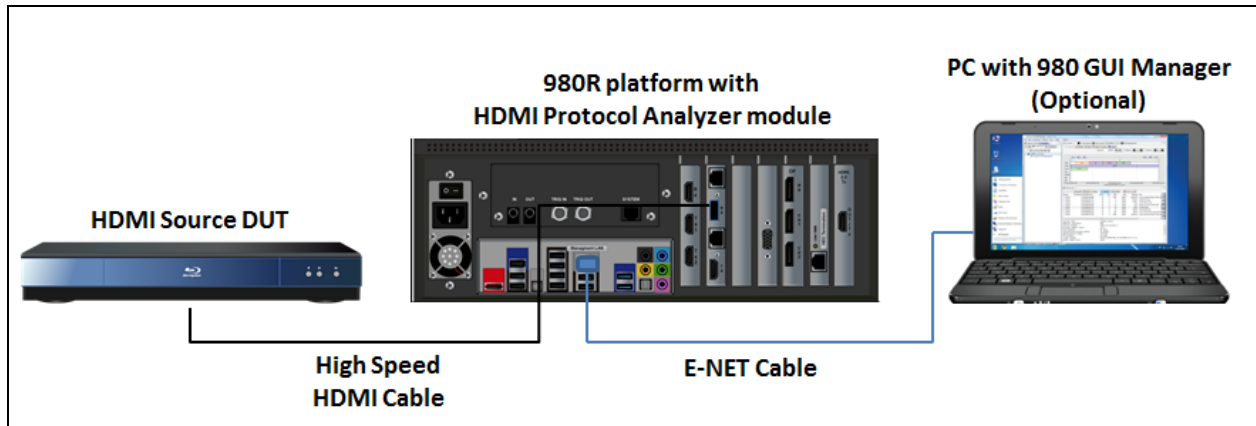
provision itself with an EDID which facilitates the Source DUT in outputting a YCbCr 4:2:0 compliant video timing.

3. Procedure

Use the following procedure to conduct this test.

- 1 Connect Source DUT to the Quantum Data 980 HDMI Protocol Analyzer at the module's port labeled Rx. Use a High Speed HDMI cable. The figures below show depictions of connections to the 980 HDMI Protocol Analyzer module residing in various 980 series chassis.

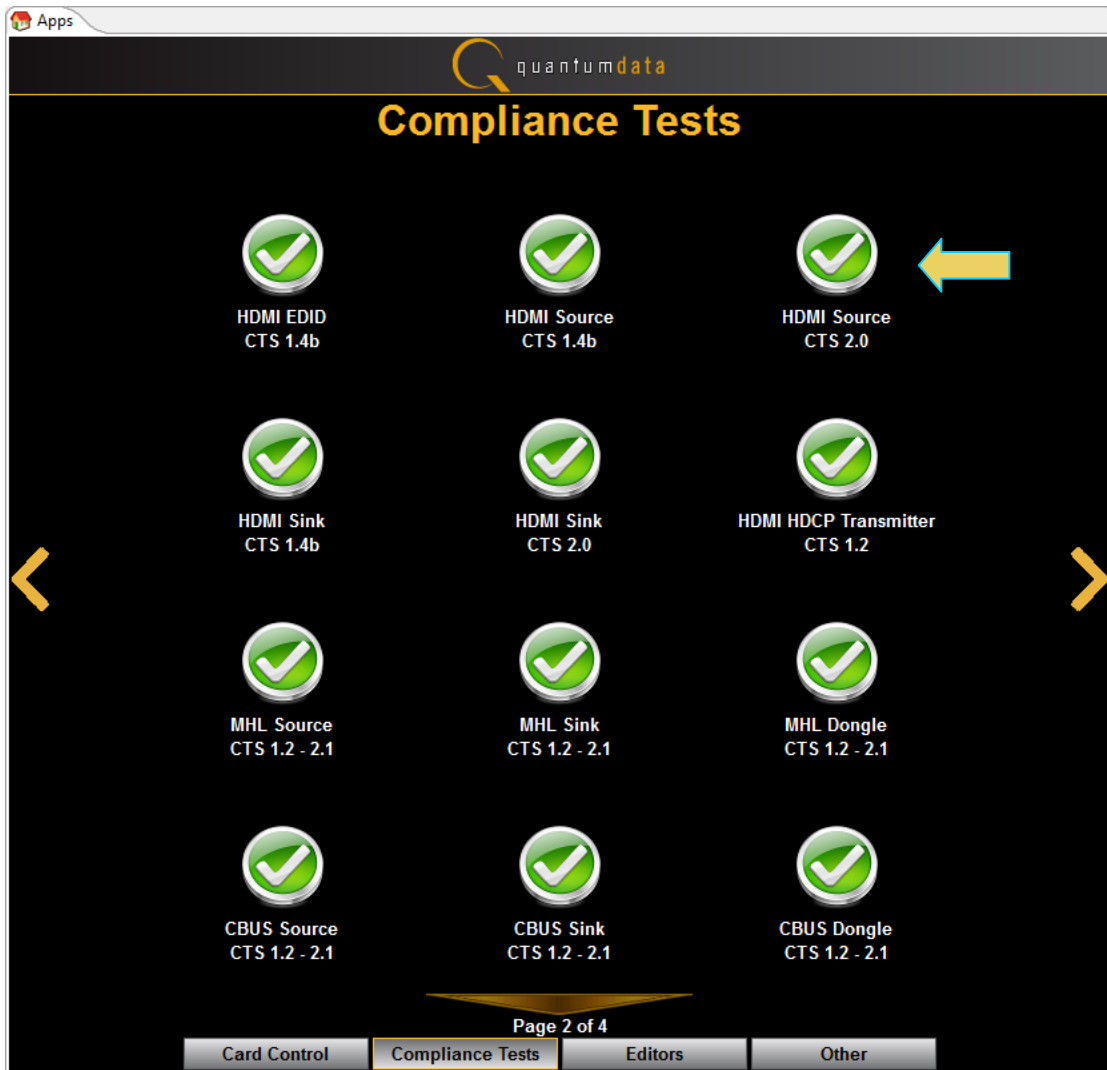




- 2 Operate the Source DUT to output a 24 bit/pixel YCbCr 4:2:0 Pixel encoded signal at a Video Format for which it supports YCbCr 4:2:0 transmission. If the Source DUT supports the compliant colorbar test image specified in the HDMI 2.0 Compliance Test specification, select that test image. Otherwise select a suitable image containing visible differentiation of colors/grays as stated in the HDMI 2.0 CTS.
- 3 Use Quantum Data 980 Embedded Manager GUI (touchscreen) or invoke Quantum Data 980 External Manager GUI (Windows application).

Note: You will not need to connect the PC shown in the figures above if you are running the compliance test through the 980's embedded display. The PC running the 980 HDMI Protocol Analyzer module's compliance test application is connected to the 980 through a standard Ethernet cable.

- 4 Complete the following steps:
 - 4.1 Click on the HDMI Source CTS 2.0 icon in the Compliance Tests page of the Apps panel.



- 4.2 Navigate to the CDF tab if not already there. If there is a saved CDF file, then click on Open and select it. Otherwise, enter the DUT's CDF information for each tab and optionally click on Save to save the CDF.

Test Case #1: with test image. If the DUT has the prescribed test image be sure to check the Source_HDMI_YCBCR_420_Test_Image item as shown on the screen example below.

The screenshot shows the 'HDMI Src CT 2.0' application window. The 'CDF Entry' tab is active, displaying a 'CDF File: <not saved>' status. The 'Y420 Video' sub-tab is selected. The interface contains several configuration sections:

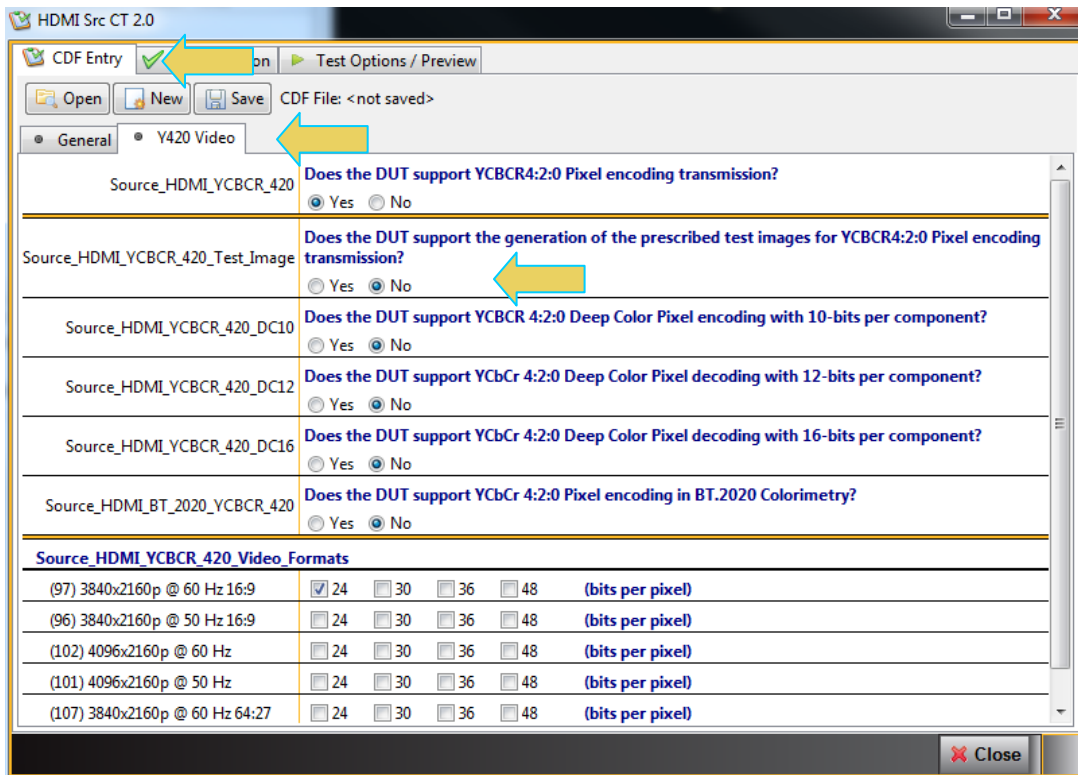
- Source_HDMI_YCBCR_420**: Includes a 'Test Options / Preview' button and a 'CDF File: <not saved>' label.
- Source_HDMI_YCBCR_420_Test_Image**: A checkbox labeled 'Source_HDMI_YCBCR_420_Test_Image' is checked.
- Source_HDMI_YCBCR_420_DC10**: A checkbox labeled 'Source_HDMI_YCBCR_420_DC10' is checked.
- Source_HDMI_YCBCR_420_DC12**: A checkbox labeled 'Source_HDMI_YCBCR_420_DC12' is checked.
- Source_HDMI_YCBCR_420_DC16**: A checkbox labeled 'Source_HDMI_YCBCR_420_DC16' is checked.
- Source_HDMI_BT_2020_YCBCR_420**: A checkbox labeled 'Source_HDMI_BT_2020_YCBCR_420' is checked.

Below these sections is a table titled 'Source_HDMI_YCBCR_420_Video_Formats' with columns for format ID, resolution, frame rate, and bits per pixel. The table lists six formats, all of which are checked.

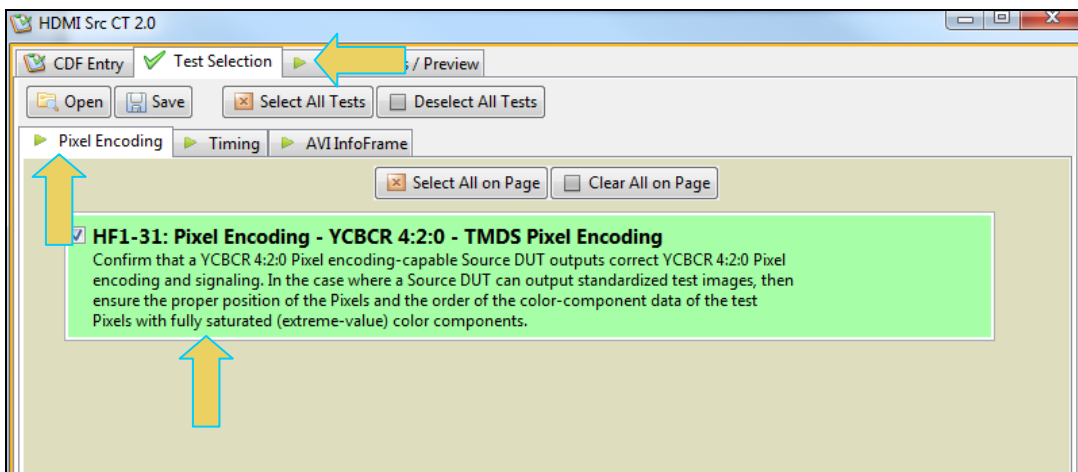
Format ID	Resolution	Frame Rate	Bits per Pixel
(97)	3840x2160p	@ 60 Hz 16:9	24 30 36 48 (bits per pixel)
(96)	3840x2160p	@ 50 Hz 16:9	24 30 36 48 (bits per pixel)
(102)	4096x2160p	@ 60 Hz	24 30 36 48 (bits per pixel)
(101)	4096x2160p	@ 50 Hz	24 30 36 48 (bits per pixel)
(107)	3840x2160p	@ 60 Hz 64:27	24 30 36 48 (bits per pixel)
(106)	3840x2160p	@ 50 Hz 64:27	24 30 36 48 (bits per pixel)

The 'Close' button is located at the bottom right of the window.

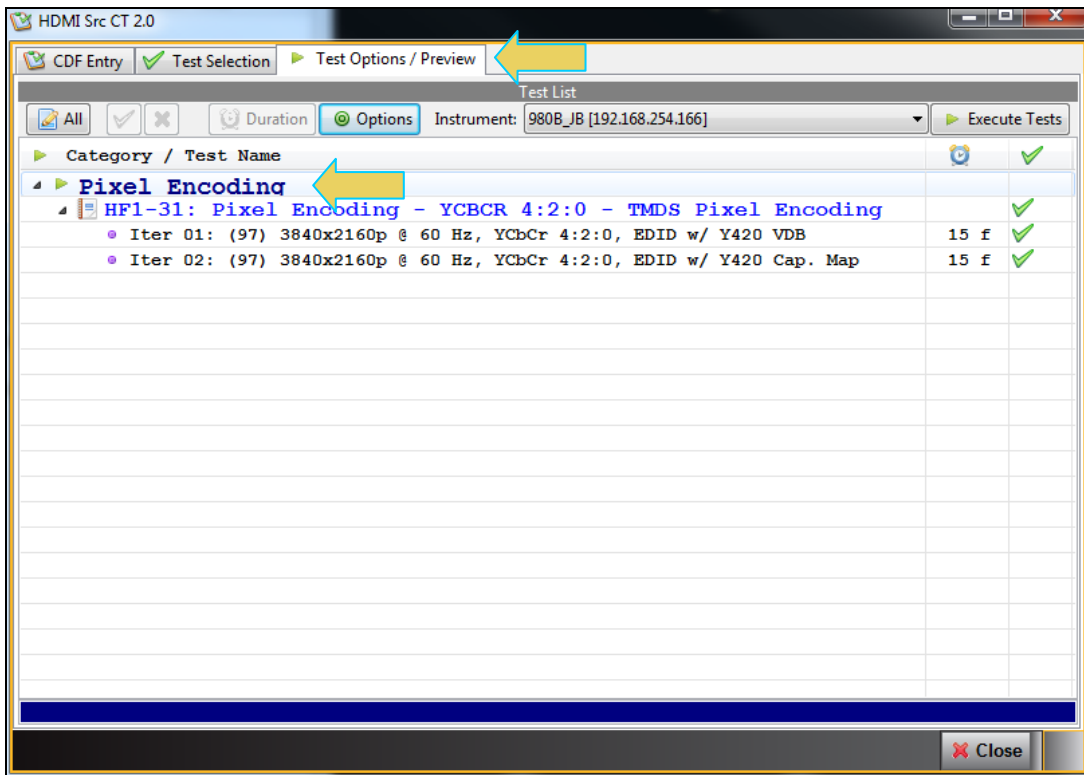
Test Case #2: without test image. If the DUT does not have the prescribed test image be sure to leave the Source_HDMI_YCBCR_420_Test_Image item unchecked as shown on the screen example below.



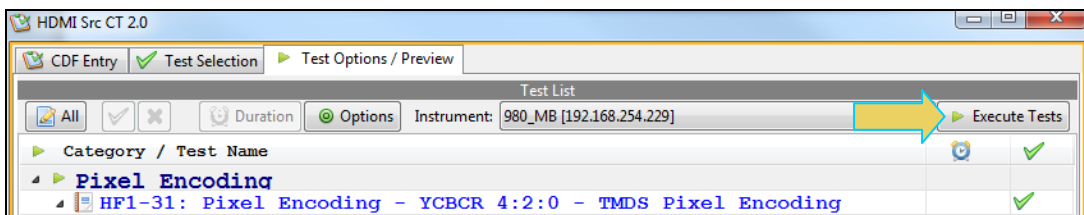
4.3 Click on the Test Selection tab and the Pixel Encoding sub tab and select the HF1-31 Source Pixel Encoding YCbCr 4:2:0 Test. Refer to the sample screen below.



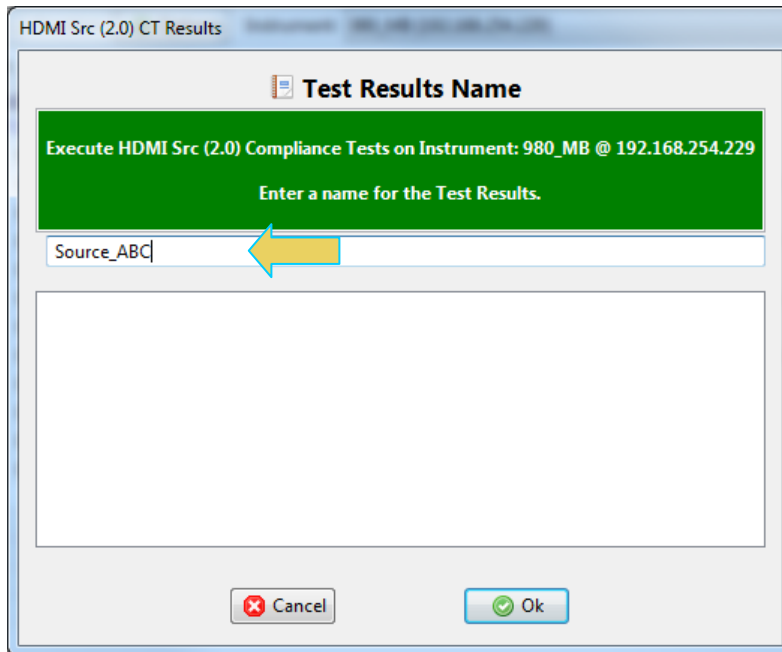
- 4.4 Click on Test Options / Preview tab and review the list of tests. Refer to the sample screen below.



- 4.5 Click on Execute tests activation button to initiate the test. Refer to the sample screen below.

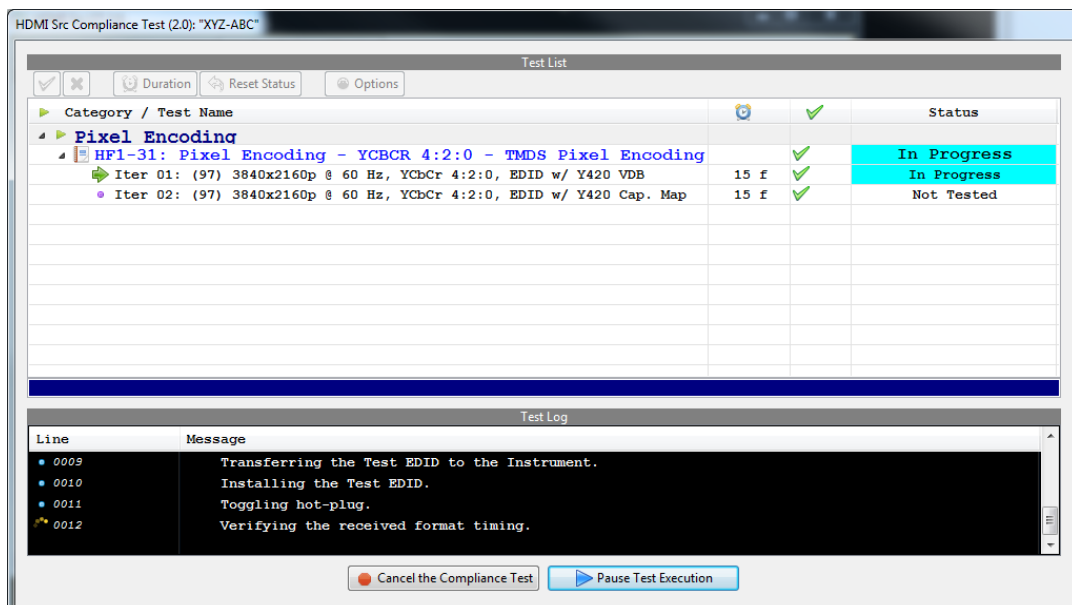


Note: You will be prompted with a dialog box to assign a name to the test results. Refer to the screen example below:

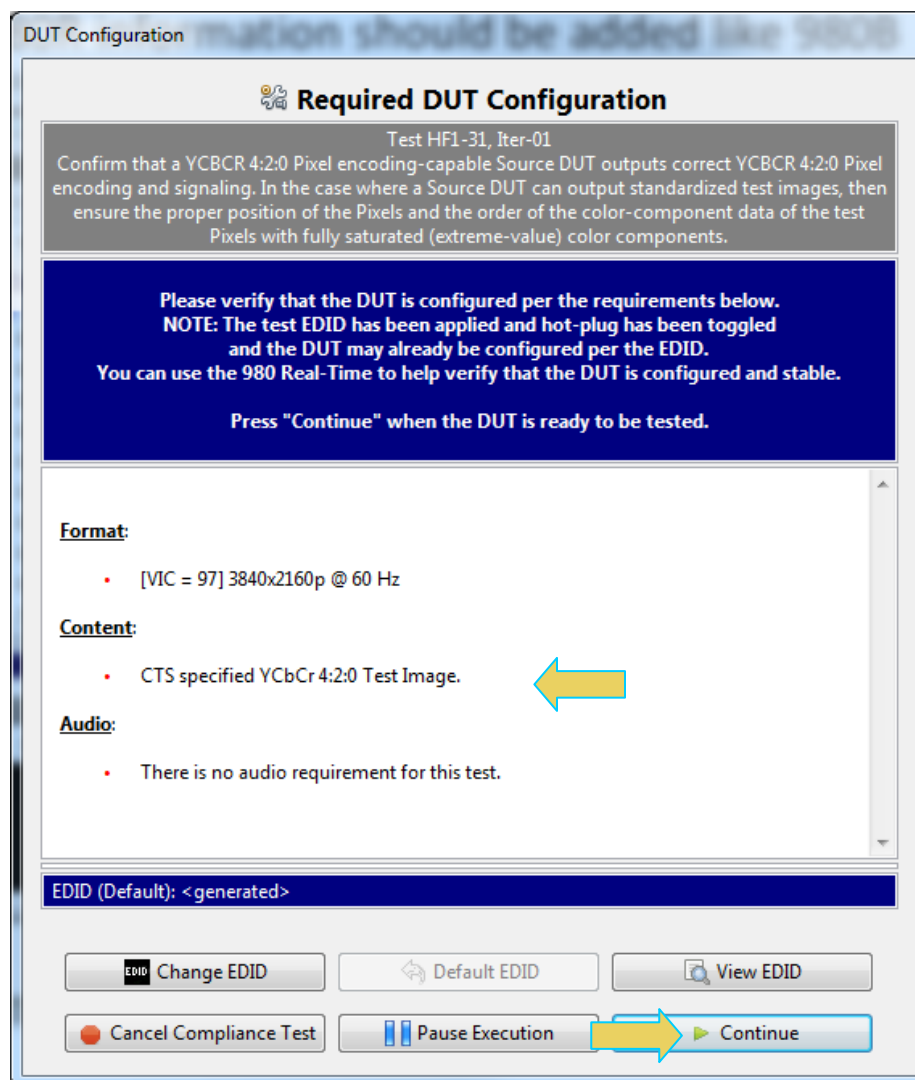


Enter a name and the test will begin.

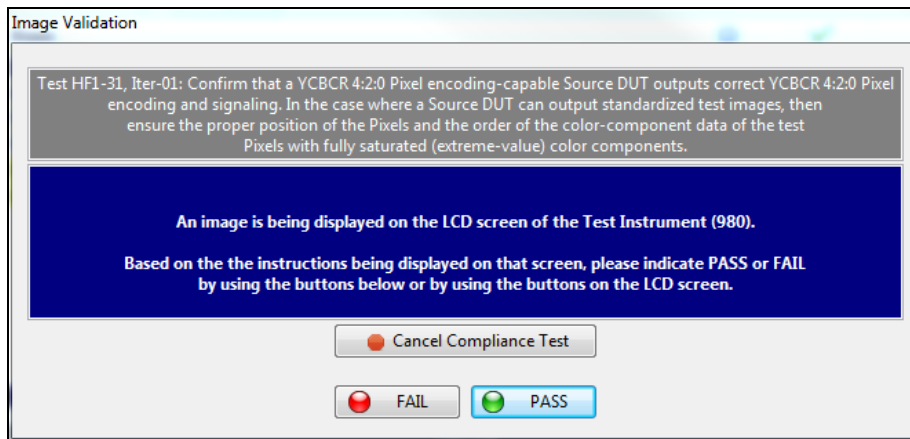
A Test Window will appear (below) indicating the progress of the test.



You will be prompted with a dialog box informing you of the requirements of the source DUT. Verify that the source is outputting the required HDMI format and pixel encoding and press Continue to run the test.



- 4.6 Follow the prompts issued by the 980 HDMI Protocol Analyzer's compliance test application. When asked to indicate Pass or Fail based on the image presented on the 980 embedded display, indicate Pass or Fail appropriately.



- 5 If the 980 HDMI Protocol Analyzer's compliance test application reports PASS, then PASS. If the 980 HDMI Protocol Analyzer's compliance test application reports FAIL, then FAIL.

