High-Definition Multimedia Interface

Version 1.4b

Quantum Data MOI v1.0

Test: DDC Source

October 7, 2015

Preface

Notice

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Document Revision History

1.0 October 7, 2015 – Initial Release.

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Contact Information

The URL for the HDMI Forum web site is: **http://www.hdmiforum.org/**

The URL for the Quantum Data website is: **http://www.quantumdata.com**.

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Introduction

This document provides a set of test methods for tests described in High-Definition Multimedia Interface Compliance Test Specification DDC Clarification.

Scope

This document provides testing procedures for HDMI CTS 1.4b Source DDC tests: 1) I2C Bus LOW-level Output Voltage and 2) Pull-Up Resistance.

References

Normative References

High-Definition Multimedia Interface Specification Version 1.4b, October 11, 2011.
HDMI Compliance Test Specification Version 1.4b, October 11, 2011.
High-Definition Multimedia Interface Compliance Test Specification DDC Clarification, Version 1.04 – May 1, 2014.

Informative Reference

No additional informative references.

Test: Source - I2C Bus LOW-Level Output Voltage

Objective

Confirm that the LOW-level output voltage of the I^2C Bus, formed when connecting the Source DUT to a compliant Sink with a LOW-level output current of 3mA, is less than or equal to the required maximum for DDC signals SCL and SDA.

Reference	Requirement
DDC Rev 4, Section 6.1	For devices and systems compliant with This Specification, the Display Data Channel (DDC) I/Os and wires (SDA, SCL, DDC/CEC Ground), shall meet the requirements specified in the I2C-bus specification and user manual UM10204, Rev. 5 ("I2C Specification"), Section 6.1 for “Standard-mode” devices...
I^2C-bus specification and user manual UM10204, Rev.5, Section 6.1	Maximum LOW-level output voltage, V_{OL} = 0.4V (at 3mA sink current)

Capability(s)

There are no specific product capabilities for this test.

Test Equipment

Item	Generic Equipment	Vendor Specific Equipment	Quantity
1	DDC Slave EDID Emulator	980 Advanced Test Platform series: 980 HDMI Phy & Protocol Aux Channel Analyzer module.	1

Generic Procedure

Setup:

1. Configure EDID Emulator with a valid HDMI EDID.
2. Configure DDC Slave with 42.3K pull-up resistance to +5.5V supply on both SCL and SDA wires.
3. Configure DDC Slave to sink 3mA of current on SDA wires when the DDC Slave drive SDA using open drain or open collector outputs.
4. Connect TPA to Source DUT.
5. Connect DDC Slave with EDID Emulator to TPA.
6. Test LOW-level output voltage of SDA:
    6.1. Pulse HPD low for more than 100ms.

6.2. If the Source does not start a DDC transaction, then FAIL.

6.3. Use the DDC Slave with EDID Emulator (if capable) or the General Oscilloscope to measure the LOW-level output voltage of SDA ($V_{OL\text{-}SDA}$) during the DDC transaction when the Source is outputting the slave address of the I2C read transaction(s), and when the DDC Slave is generating an ACK, and outputting the data from the I2C read transaction(s).

7. Test LOW-level output voltage of SCL:

7.1. Pulse HPD low for more than 100ms.

7.2. If the Source does not start a DDC transaction, then FAIL.

7.3. Use the DDC Slave with EDID Emulator (if capable) or the General Oscilloscope to measure the LOW-level output voltage of SCL ($V_{OL\text{-}SCL}$) during the DDC transaction(s) when the Source is reading the EDID.

7.4. If $V_{OL\text{-}SCL} > 0.4V$, then FAIL.

Test: Source - I2C Bus LOW-Level Output Voltage

Objective

Confirm that the Source meets critical bus timing parameters specified in the I2C bus specification.

Reference	Requirement
DDC Rev 4, Section 6.1	For devices and systems compliant with This Specification, the Display Data Channel (DDC) I/Os and wires (SDA, SCL, DDC/CEC Ground), shall meet the requirements specified in the I2C-bus specification and user manual UM10204, Rev. 5 ("I2C Specification"), Section 6.1 for “Standard-mode” devices…. HDMI Source Devices generate the clock signals on the bus, and hence shall choose a Source pull-up resistance that is consistent with their specific maximum SCL clock frequency, such that the signal high time requirements in the I2C Specification are met.
HDMI 1.4b, Table 4-35	HDMI Source SCL/SDA maximum capacitance = 50pF HDMI Sink SCL/SDA maximum capacitance = 50pF HDMI Cable Assembly SCL/SDA maximum capacitance = 700pF
I2C-bus specification and user manual UM10204, Rev.5, Section 6.1	1) Hold time (repeated) START condition ($t_{HD;STA}$) ≥ 4.0 µs 2) Setup time (repeated) START condition ($t_{SU;STA}$) ≥ 4.7 µs 3) Setup time for STOP condition ($t_{SU;STO}$) ≥ 4.0 µs 4) Bus free time between STOP and START condition (t_{BUF}) ≥ 4.7 µs 5) Data hold time ($t_{HD;DAT}$) ≥ 0 µs 6) Data setup time ($t_{SU;DAT}$) ≥ 250 ns

Capability(s)

There are no specific product capabilities for this test.

Test Equipment

Item	Generic Equipment	Vendor Specific Equipment	Quantity
1	DDC Slave EDID Emulator	980 Advanced Test Platform series: 980 HDMI Phy & Protocol Aux Channel Analyzer module.	1

Generic Procedure

Setup:

1. Configure EDID Emulator with a valid HDMI EDID.
2. Configure DDC Slave with 51.7K pull-up resistance to +5.5V supply on SCL wire, and 42.3K pull-up resistance to +5.5V supply on SDA wire.

3. Configure DDC Slave to achieve 750pF total capacitance (including emulator, TPA, probes, etc.) on SCL and SDA wires.

4. Connect TPA to Source DUT.

5. Connect DDC Slave with EDID Emulator to TPA.

6. Pulse HPD low for more than 100ms.

7. Observe the Source DUT reading the EDID from the EDID Emulator.

8. If the Source does not start a DDC transaction, then FAIL

9. Use the DDC Slave (if capable) or the General Oscilloscope to measure the specified timing parameters for each occurrence during the EDID read.

    9.1. If any occurrence of $t_{HD;STA} < 4.0\mu s$, then FAIL.

    9.2. If any occurrence of $t_{SU;STA} < 4.7\mu s$, then FAIL.

    9.3. If any occurrence of $t_{SU;STO} < 4.0\mu s$, then FAIL.

    9.4. If any occurrence of $t_{BUF} < 4.7\mu s$, then FAIL.

    9.5. If any occurrence of $t_{HD;DAT} < 0\mu s$, then FAIL.

    9.6. If any occurrence of $t_{SU;DAT} < 250ns$, then FAIL.

Vendor Specific Test Procedure

Test Equipment

A variety of equipment is needed for testing HDMI products. Each piece is authorized and included by name in this Compliance Test Specification. This section describes the Quantum Data test equipment.

HDMI Phy & Protocol Aux Channel Analyzer Module

The Quantum Data 980 HDMI Phy & Protocol Aux Channel Analyzer module can be installed in the 980B or 980R series Advanced Test Platforms. This 980 HDMI Phy & Protocol Aux Channel Analyzer module serves the generic test functions called out in the HDMI CTS DDC Clarification. Refer to the table below:

Item	Quantum Data Equipment	
1	980 Advanced Test Platform series:	
	Equipped with:	980 Advanced Test Platform series: 980 HDMI Phy & Protocol Aux Channel Analyzer module.

980 HDMI Phy & Protocol Aux Channel Analyzer with 980B Series Platform Configuration

The figure below shows a depiction of the 980 Phy & Protocol Aux Channel Analyzer module equipped in various 980B platform. **Note**: Card positioning may vary depending on configuration.

Tests: Source DDC Tests

1. Objectives

I2C Bus LOW-Level Output Voltage - Confirm that the LOW-level output voltage of the I2C Bus, formed when connecting the Source DUT to a compliant Sink with a LOW-level output current of 3mA, is less than or equal to the required maximum for DDC signals SCL and SDA.

Bus Timing - Confirm that the Source meets critical bus timing parameters specified in the I2C bus specification.

2. Test Overview

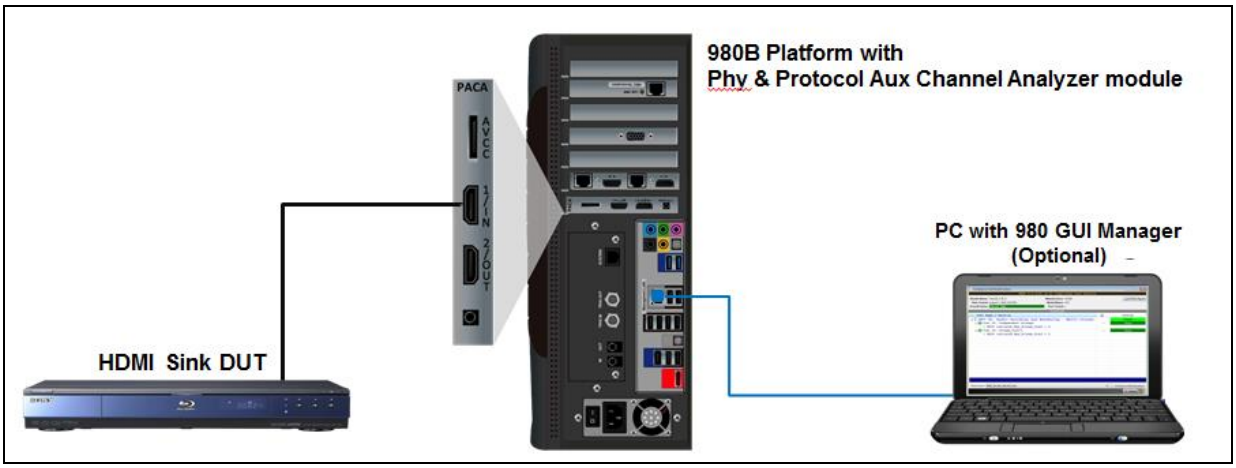
The Pass/Fail criteria is assessed by the application with no human examination required.

3. Procedure

Use the following procedure to conduct this test.

1 Connect Source DUT to the Quantum Data 980 HDMI Phy & Protocol Aux Channel Analyzer at the module's port labeled IN. Use a High Speed HDMI cable. The figure below shows a depiction of connections to the 980 HDMI Phy & Protocol Aux Channel Analyzer module residing in the 980 series chassis.

Note: Be sure to use the supplied HDMI cable. Part No. 30-00219. Description: CBL, HDMI, 7ft High Speed, Heac, Calibrated-Source



2 Operate the Source DUT in a normal mode. The video format and content does not matter.

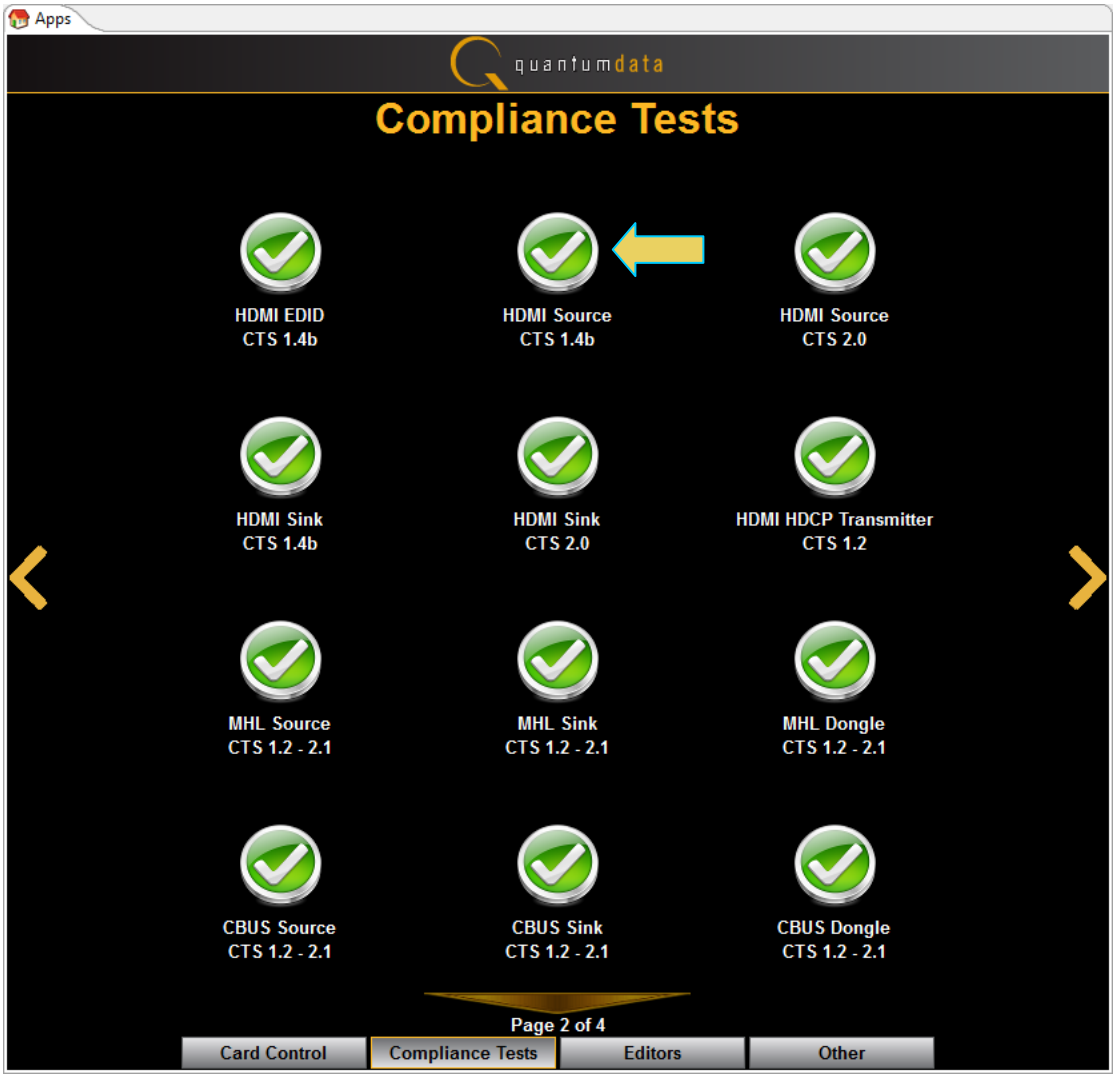
3 Use Quantum Data 980 Embedded Manager GUI (touchscreen) or invoke Quantum Data 980 External Manager GUI (Windows application).

Note: You will not need to connect the PC shown in the figure above if you are running the compliance test through the 980's embedded display. The PC running the 980 HDMI

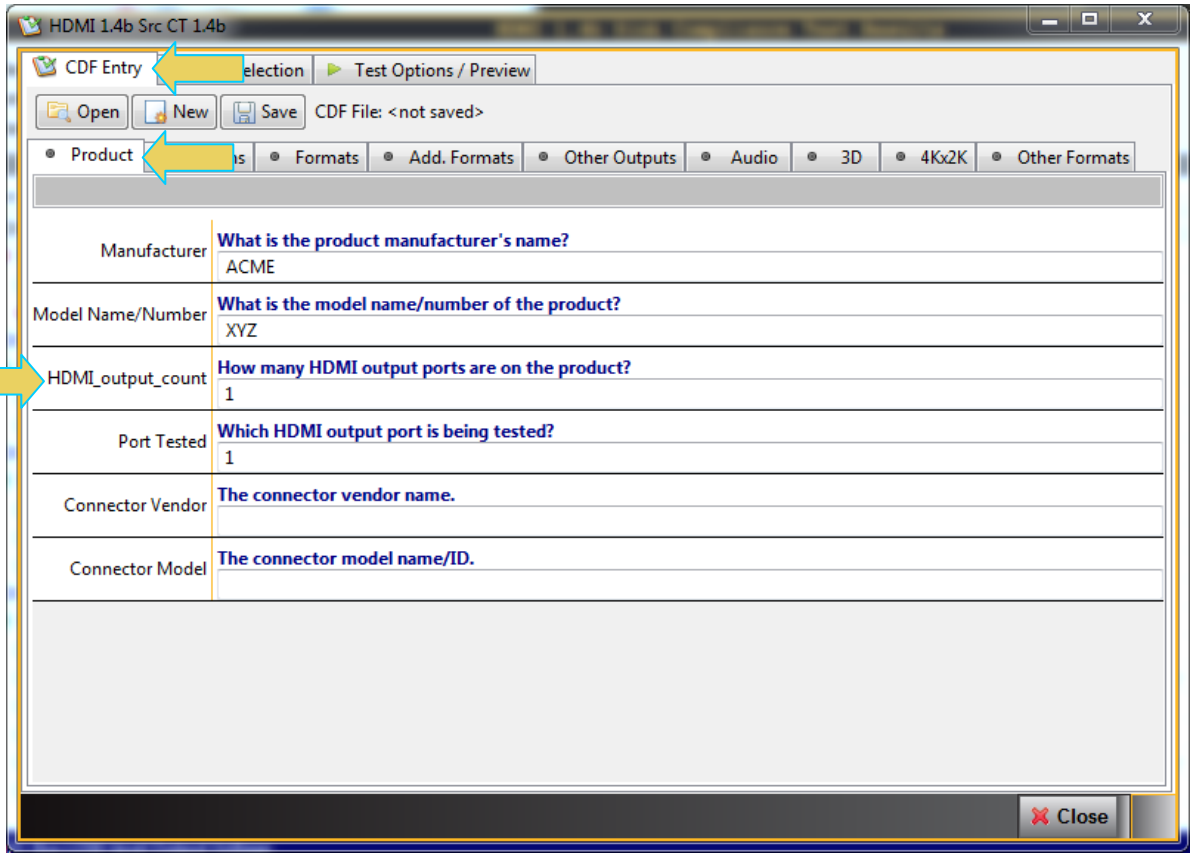
Phy & Protocol Aux Channel Analyzer module's compliance test application is connected to the 980 through a standard Ethernet cable.

4 Complete the following steps:

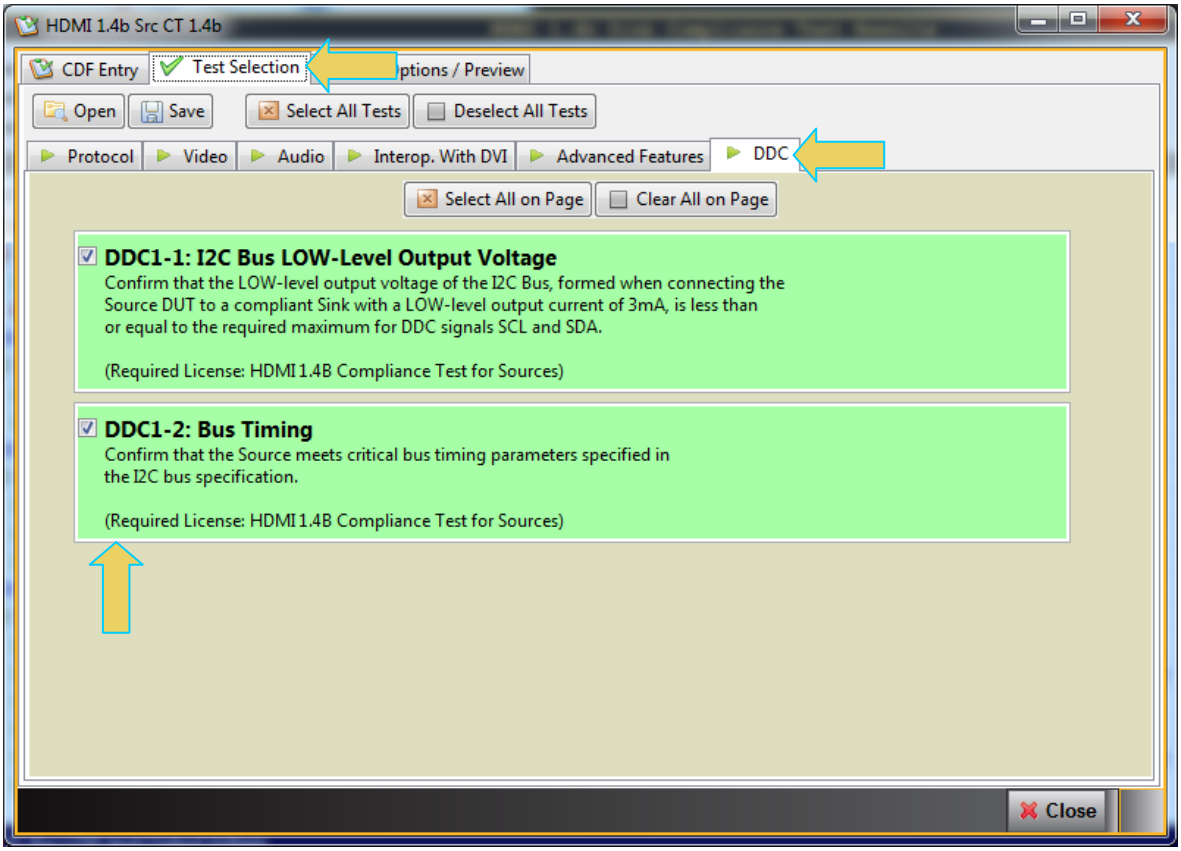
4.1 Click on the HDMI Source CTS 1.4b icon in the Compliance Tests page of the Apps panel.



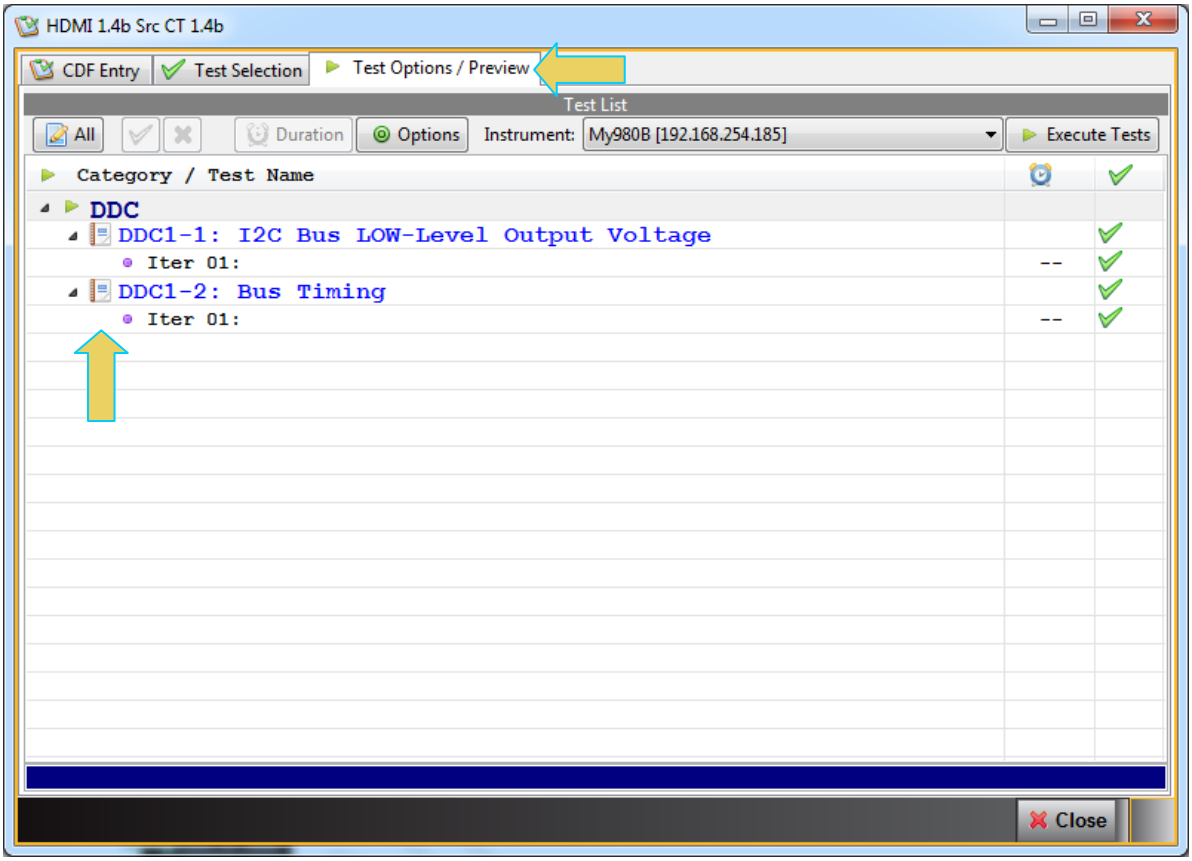
4.2 Navigate to the CDF tab if not already there. There are no CDF requirements to be entered. Simply fill in the name and model number of the device and click OK and optionally save the file.



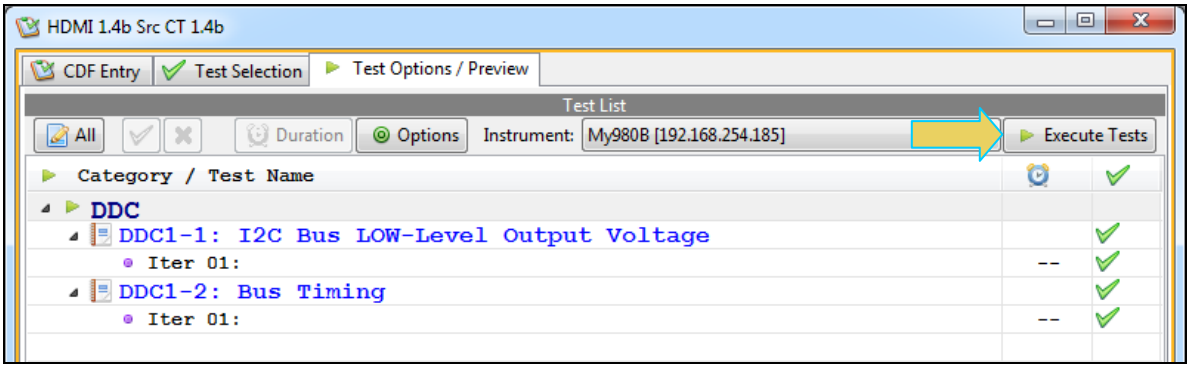
4.3 Click on the Test Selection tab and the DDC sub tab and select the DDC1-1: I2C Bus Low-Level Output Voltage test and the DDC1-2: Bus Timing test. Refer to the sample screen below.



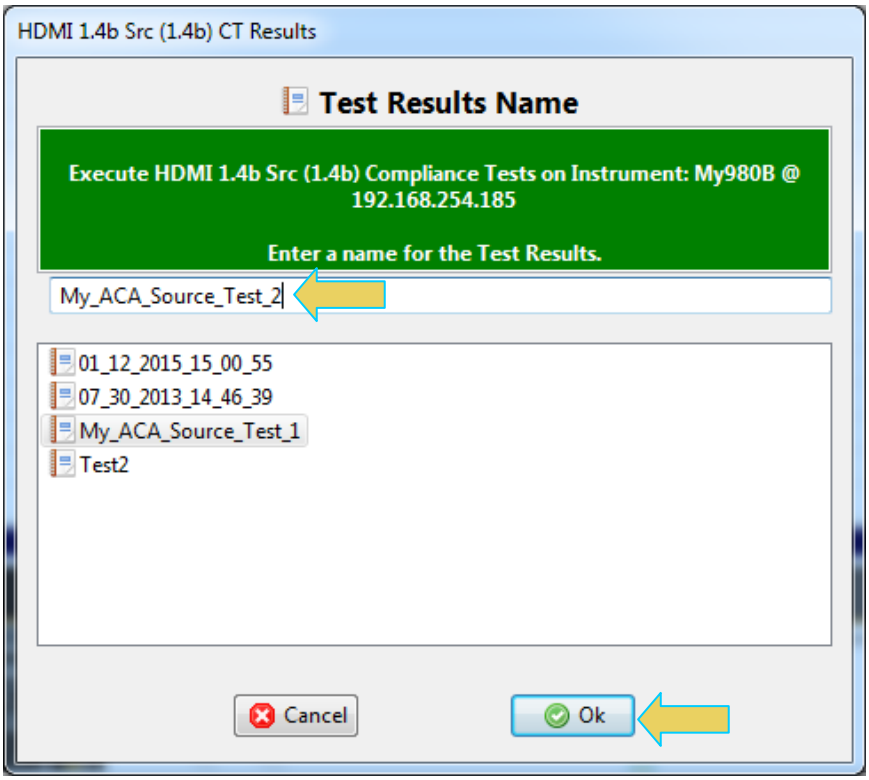
4.4 Click on Test Options / Preview tab and review the list of tests. Refer to the sample screen below.



4.5 Click on Execute tests activation button to initiate the test. Refer to the sample screen below.

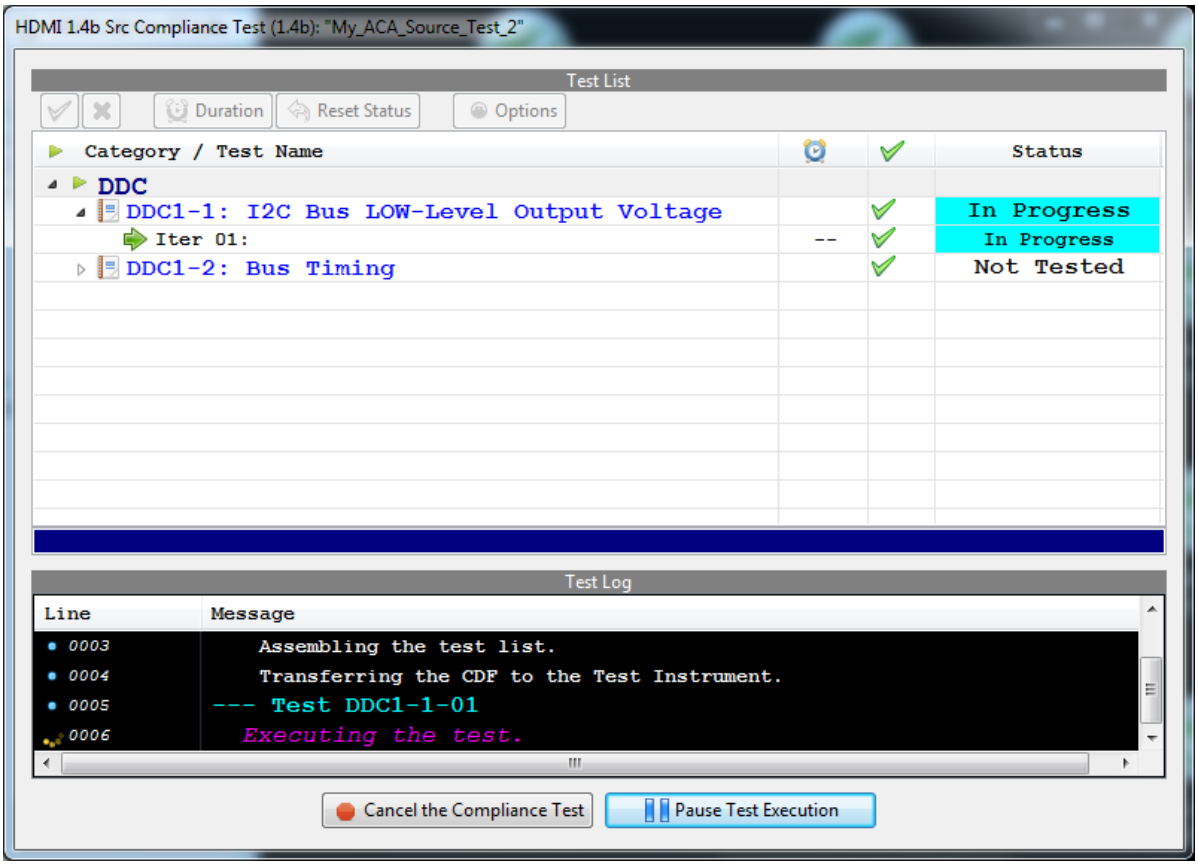


Note: You will be prompted with a dialog box to assign a name to the test results. Refer to the screen example below:

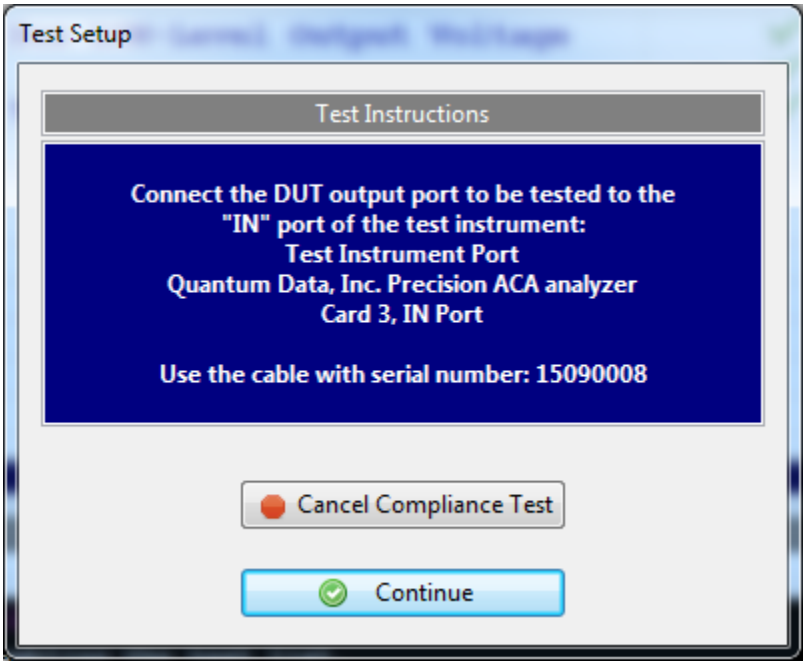


Enter a name, click OK and the test will begin.

A Test Window will appear (below) indicating the progress of the test.

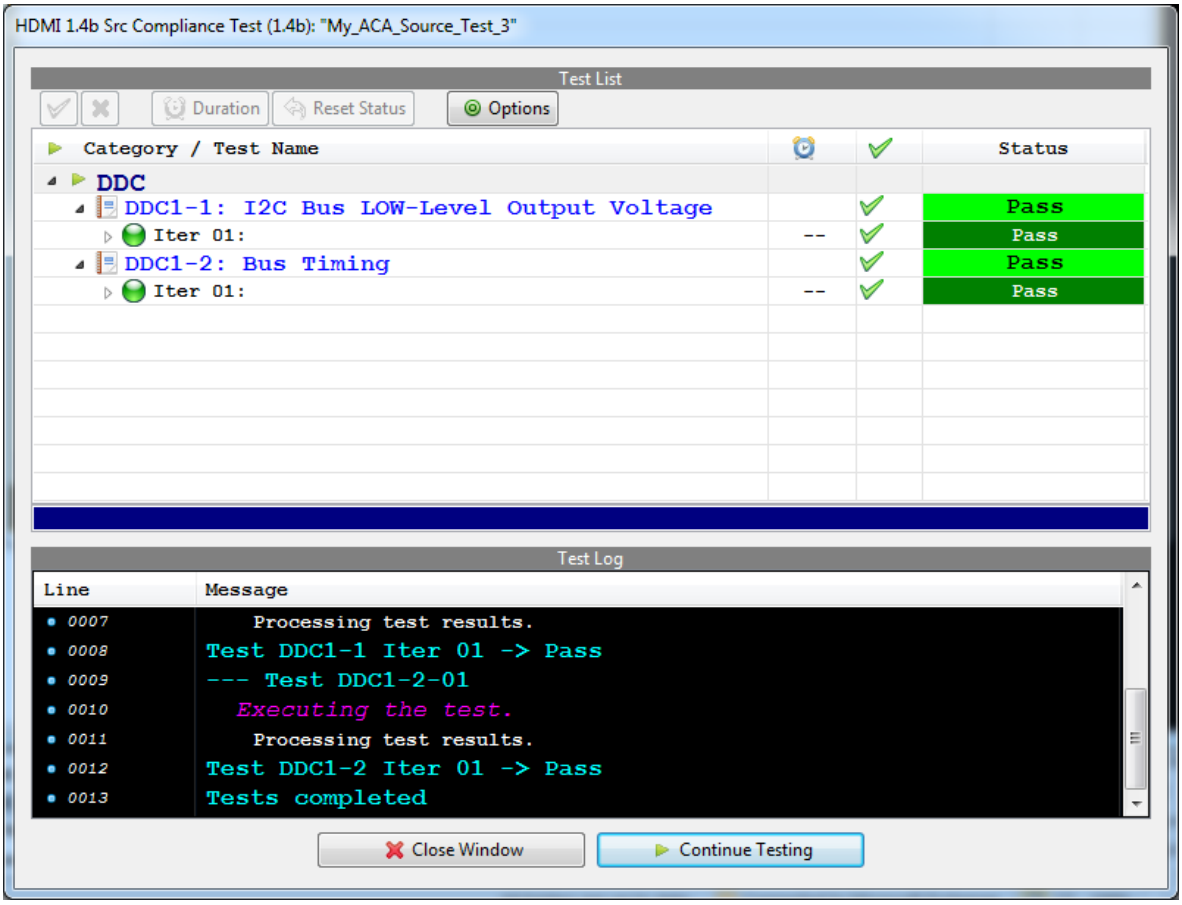


A dialog box will appear (below) indicating the test setup.

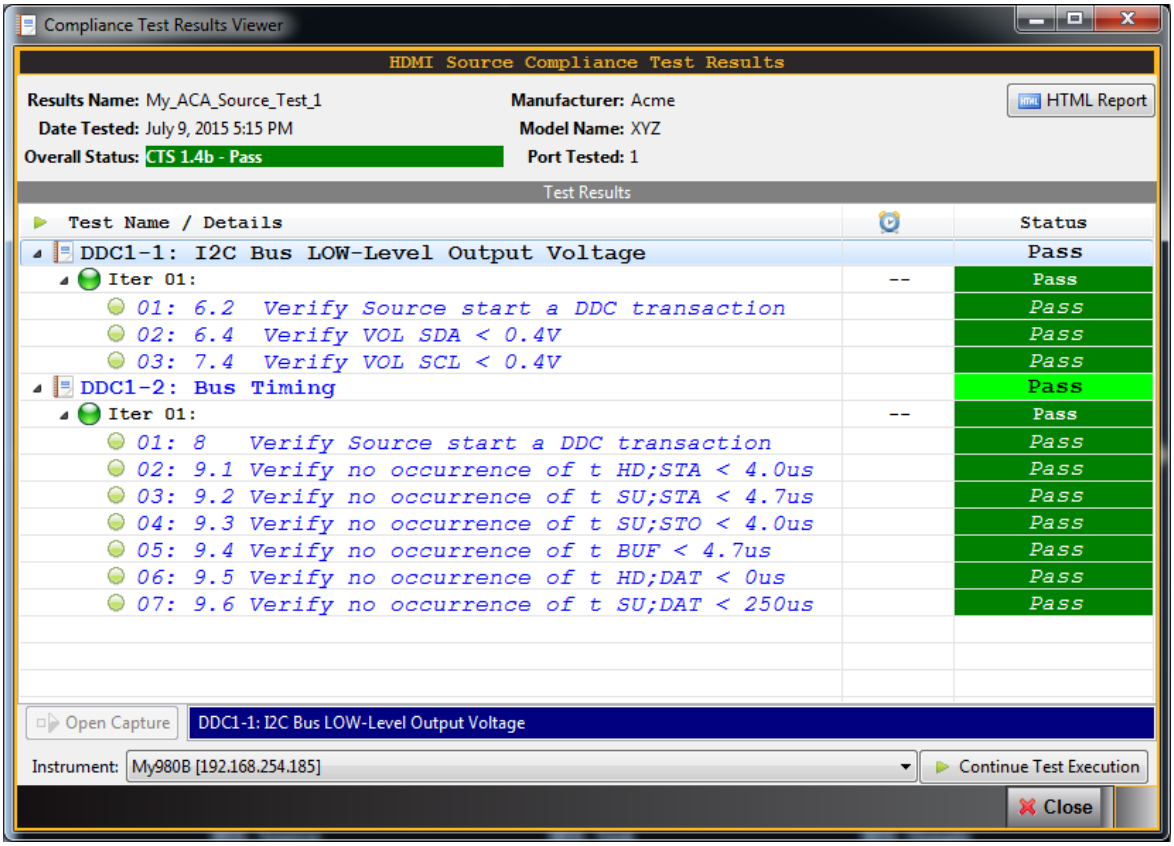


Note: Be sure to use the supplied HDMI cable. Part No. 30-00219.

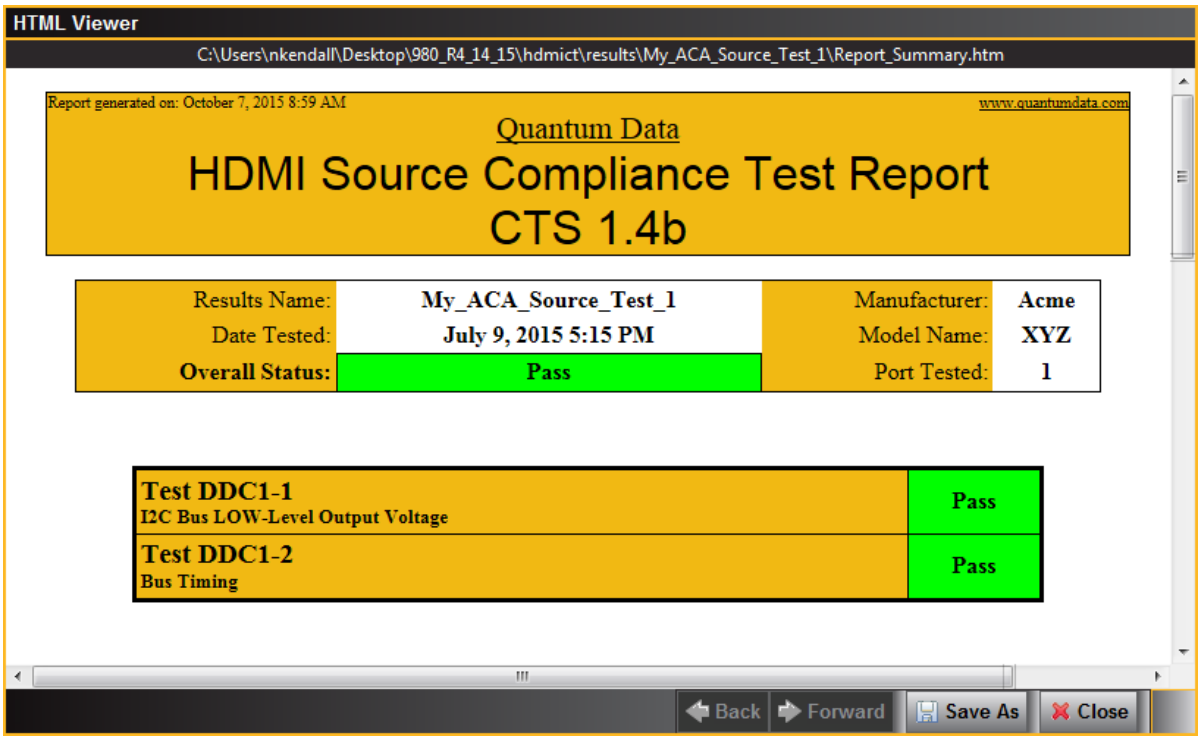
When the tests are complete the results are shown in the test window.

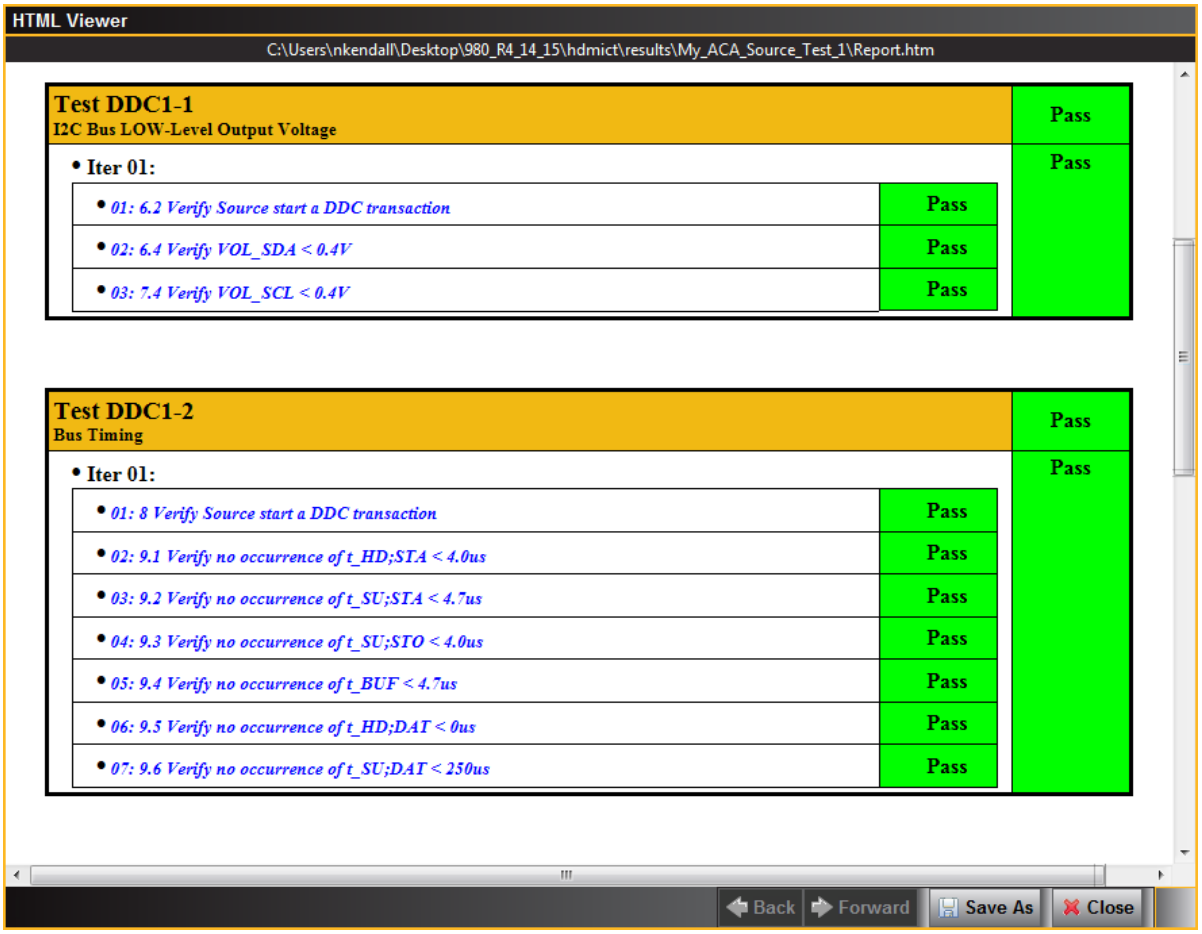


The test will run and the test application will assess pass or fail. The test results screens appears as shown below. If the 980 HDMI Protocol Analyzer's compliance test application reports PASS, then PASS. If the 980 HDMI Phy & Protocol Aux Channel Analyzer compliance test application reports FAIL, then FAIL.



You can also obtain an HTML report. The report can be a summary or include the details of the test results. These are shown below.


HTML Viewer
C:\Users\nkendall\Desktop\980_R4_14_15\hdmict\results\My_ACA_Source_Test_1\Report_Summary.htm
Report generated on: October 7, 2015 8:59 AM
www.quantumdata.com
Quantum Data
HDMI Source Compliance Test Report
CTS 1.4b
Results Name: My_ACA_Source_Test_1
Date Tested: July 9, 2015 5:15 PM
Overall Status: Pass
Manufacturer: Acme
Model Name: XYZ
Port Tested: 1
Test DDC1-1
I2C Bus LOW-Level Output Voltage
Pass
Test DDC1-2
Bus Timing
Pass
Back
Forward
Save As
Close


HTML Viewer
C:\Users\nkendall\Desktop\980_R4_14_15\hdmict\results\My_ACA_Source_Test_1\Report.htm
Test DDC1-1
I2C Bus LOW-Level Output Voltage
Pass
• Iter 01:
Pass
• 01: 6.2 Verify Source start a DDC transaction
Pass
• 02: 6.4 Verify VOL_SDA < 0.4V
Pass
• 03: 7.4 Verify VOL_SCL < 0.4V
Pass
Test DDC1-2
Bus Timing
Pass
• Iter 01:
Pass
• 01: 8 Verify Source start a DDC transaction
Pass
• 02: 9.1 Verify no occurrence of t_HD;STA < 4.0us
Pass
• 03: 9.2 Verify no occurrence of t_SU;STA < 4.7us
Pass
• 04: 9.3 Verify no occurrence of t_SU;STO < 4.0us
Pass
• 05: 9.4 Verify no occurrence of t_BUF < 4.7us
Pass
• 06: 9.5 Verify no occurrence of t_HD;DAT < 0us
Pass
• 07: 9.6 Verify no occurrence of t_SU;DAT < 250us
Pass
Back
Forward
Save As
Close