

# 980 MHL CBUS Compliance Test Module

# **User Guide**

Rev: A4



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### 1 About the 980 MHL CBUS Compliance Test Module

This chapter provides an overview of features of the 980 MHL CBUS Compliance Test module and the 980 GUI Manager. The module can be equipped in either of two 980 Advanced Test Platforms:

- 1) The 980 Advanced Test Platform 2-slot chassis with a 10.4 inch touch display (example shown below).
- 2) The 980B Advanced Test Platform 5-slot chassis with a 15 inch touch display

The 980 MHL CBUS Compliance Test module provides CBUS compliance testing for MHL CTS 1.2 and 2.0 source, sink and dongle devices. The 980 GUI Manager is a PC application to manage and use the 980 MHL CBUS Compliance Test module. The test require no additional external equipment. You can disseminate the test results and Log Plots to colleagues, subject matter experts and Quantum Data support for analysis. Your colleagues and subject matter experts are not required to have a 980 test instrument to view the test results and Log Plots; they simply need to download the 980 GUI Manager application from the Quantum Data website.



980 Advanced Test Platform – Front View



980 Advanced Test Platform – Rear View



980 Advanced Test Platform

### 1.1 Scope of this User Guide

This User Guide provides descriptive and procedural information on the 980 MHL CBUS compliance test module for testing MHL sources, sinks and dongles.

Although you can run the compliance tests through the 980's "embedded GUI," all the examples used in the procedures in this User Guide are taken from the external standalone PC 980 GUI Manager. The procedures are identical between the embedded GUI running through the 980 front panel display and the external standalone PC application but the look and feel is slightly different.

The following is a list of the User Guides available for the 980 systems:

- 980 HDMI Protocol Analyzer Gen 3 System This User Guide covers source analysis testing for HDMI and MHL source devices as well as various transmitter features. This user guide is specifically for the functions of the 980 HDMI Protocol Analyzer Gen 3 system sold through 2012.
- 980 HDMI Protocol Analyzer module This User Guide covers source analysis features of the 980 HDMI Protocol Analyzer module. Used in conjunction with the 980 Advanced Test Platform Quick Start Guide for purchases in 2013.
- 980 Advanced Test Platform Quick Start Guide This Quick Start Guide covers startup procedures for the 980/980B platform. Used in conjunction with the 980 HDMI Protocol Analyzer Module User Guide for purchases in 2013.
- 980 HDMI Protocol Analyzer module This User Guide covers source analysis testing for HDMI and MHL source devices as well as various transmitter features. This user guide is specifically for the functions of the 980 HDMI Protocol Analyzer module equipped in one of the 980 Advanced Test Platform slots (980 Gen 3 or 980B). Used in conjunction with the 980 Advanced Test Platform Quick Start Guide.
- 980 HDMI Protocol Analyzer HDMI/MHL Source Compliance Test This User Guide covers source compliance testing for both MHL and HDMI sources. These compliance test applications are provided by the

980 HDMI Protocol Analyzer module or the 980 HDMI Protocol Analyzer Gen 3 system. Used in conjunction with the 980 Advanced Test Platform Quick Start Guide.

- 980 HDMI Protocol Analyzer HDMI/MHL Sink Compliance Test This User Guide covers sink compliance testing for both MHL and HDMI sinks (and MHL dongles). These compliance test applications are provided by the 980 HDMI Protocol Analyzer module or the 980 HDMI Protocol Analyzer Gen 3 system. Used in conjunction with the 980 Advanced Test Platform Quick Start Guide.
- 980 MHL CBUS Compliance Test Module This User Guide covers MHL CBUS compliance testing for both MHL sources as well as sinks and dongles. This compliance test applications are provided by the 980 CBUS Compliance Test module. Used in conjunction with the 980 Advanced Test Platform Quick Start Guide.
- 980 HDMI Video Generator module This User Guide covers the features and functions offered by the 980 HDMI Video Generator module. Used in conjunction with the 980 Advanced Test Platform Quick Start Guide.

### **1.2** Changes to this User Guide

The following changes were made to this document:

This User Guide has been updated recently to include the following:

- Include MHL CBUS 2.0 compliance tests.
- Include discussion of the 980B Advanced Test Platform
- Include descriptive and procedural information on the CBUS Event Log Plot.

Note: Please be sure to check the Quantum Data website for updates to this User Guide.

# 1.3 What options are available with the 980 MHL CBUS Compliance Test module?

There are two options that you can purchase with the 980 MHL CBUS Compliance Test module. You must have a license to use these options:

- MHL CBUS Source Compliance module which tests in accordance with MHL 1.2 CTS and MHL CTS 2.0.
- MHL CBUS Sink/Dongle Compliance module which tests in accordance with MHL 1.2 CTS and MHL CTS 2.0.

You can determine what options the 980 is provisioned with by accessing the Instrument Information screen on either the built-in or external 980 GUI manager. When using the external 980 GUI Manager you must be connected to the 980 in order to read the Instrument Information. Refer to the following screen.



Select Information to view the Instrument Information panel.

January 30, 2012

```
1 Instrument Information
```

Instrument: My980B	
TD Address, 100, 160, 054, 026	
IF Address: 192.100.234.230	Ê
Ret Mask. 255.255.255.255.256.0	
Free Space: 116.51 GB of 162.23 GB (71.8%)	
Advanced Test platform Version: 4.6.28	
HDMI 980 protocol Analyzer in slot 0 [DDR 2048MB]:	
Gateware: [Version: 4.6.4 Build Number: 1 (11:07:2012) Gen: 3 pcb: 297b/D]	
Firmware: [Version: 4.6.15 Build Number: 3227 (qd 12:20:2012 09:31:45 CST) ]	
MHL CBUS Protocol Analyzer in slot 1:	
Gateware: [Version: 1 Build Number: 18 (12:04:2012 165900) pcb: 23232323]	
Firmware: [Version: 4.6.16 Build Number: 3227 (qd 12:20:2012 09:32:03 CST)]	
HDMI Video Generator in slot 2:	
Gateware: [Version: 4.5.2 Build Number: 2 (07:20:2012 00) pdb: 2976 C]	
Firmware: [Version: 4.6.2 Build Number: 3224 (qd 12:20:2012 09:30:18 CST)]	
System Information:	
$HDMT DA SM \cdot [ 0/3FOOT2A0221A9A: 10]$	
Main Board · [ "DP67BG"]	
CPUx2 : [ 6,42.7 "Intel(R) Celeron(R) CPU G530 @ 2,40GHz"]	
DDR : [ 3 GB + 512 MB]	Ε
HD : [ SSDSC2CT18]	
OS : [ Linux xpscope-4a 2.6.26-2-686 #1 SMP Sun Mar 4 22:19:19 UTC 2012 i686 GNU/Linux]	
GUI manager : [ Version 4.6.28_40115_201212200922]	
1 : [ lo inet 127.0.0.178 scope host lo]	
2 : [eth1 inet 192.168.10.1/24 brd 192.168.10.255 scope global eth1]	
HDMI SINK CT: [ 4.6.1]	
HDMI SRC CT : [ 4.6.2]	
MHL SINK CT : [ 4.6.3]	
MHL SRC CT : [ 4.6.1]	
Licensed reactures	
Licensed, 02 (HDMI SOURCE COMPLIANCE TEST)	
Licensed: 03 [EDID COMPLIANCE TEST]	
Licensed: 04 [ENCRYPTED LINK ANALYZER]	
Licensed: 06 [HDMI SINK COMPLIANCE TEST]	
Licensed: 07 [MHL SINK/DONGLE COMPLIANCE TEST]	
Licensed: 08 [MHL SOURCE COMPLIANCE TEST]	
Licensed: 09 [CBUS SOURCE COMPLIANCE TEST]	
Licensed: 10 [CBUS SINK/DONGLE COMPLIANCE TEST]	
Licensed: 11 [HDMI ACA]	
	Ψ.
OK	

x

### 1.4 980 User Interface

The 980 provides a graphical user interface for operation. This GUI can run both on the 980 itself through the built-in color touch screen display or as a standalone application running on a PC. The look and feel and functions are similar but not identical.



	Quantum Data 980
	C teastineists
MHL Source (DUT)	Image:
	MHL Cable

### 1.4.1 External 980 GUI Manager

The external 980 GUI Manager provides easy access to the captured data on your PC for sharing with others. Also the external 980 GUI Manager enables you to operate the 980 through a larger interface which allows you to use multiple panels at the same time.

### 1.4.2 Embedded 980 GUI Manager

You can operate the 980 fully through the built-in color touch screen display. There are two key features that are available only with the embedded 980 GUI Manager: 1) viewing the video in real time, 2) viewing the MHL video/audio metadata and DDC (MHL C-Bus) transactions in real time using the **Real Time** mode. These features apply to the 980 HDMI Protocol Analyzer module and not to the MHL CBUS Compliance module.

You can transfer data captures and compliance test results taken from the built-in touch display to your PC where they can be viewed through the external 980 GUI Manager and also disseminated to others for analysis.

### 2 Getting Started

This chapter explains what is involved in getting your 980 CBUS Compliance Test Module up and running in the 980/980B Advanced Test Platform.

### 2.1 What is in the 980 shipping box?

When the Quantum Data 980 is shipped it will contain a variety of items. The items it will contain will depend on the module configurations and whether it is a 980 ATP or a 980B ATP. The following list shows all the items in the 980 shipping box with the standard configuration of the 980, which includes the 980 HDMI Protocol Analyzer, and also those items specific to the MHL CBUS Compliance Test module.

#### Standard configuration items with 980/980B:

- Quantum Data 980 test instrument (comes standard with 980; optional for 980B).
- 980 HDMI Protocol Analyzer module (pre-installed).
- Ethernet cable (P/N 30-00151) used for connecting a host PC to the 980 over the LAN interface.
- Detachable power cable used for supplying power to the 980.
- HDMI cable (P/N 30-00146) Category 2 HDMI cable, 6 feet (comes standard with 980; optional for 980B).
- ESD warning sheet (P/N 68-00204) information useful for protecting the HDMI interface against static discharge.

#### MHL CBUS Compliance module items:

MHL CBUS Compliance Test module

Note: The MHL CBUS Compliance test module will be pre-installed in the 980 chassis.

- HDMI cable (P/N 30-00202) Short (30 centimeter) HDMI cable CBUS compliance test. (Used for MHL CBUS sink compliance test option).
- MHL cable (P/N 30-00197) Short (30 centimeter) MHL cable for running compliance test. (Used for MHL CBUS source compliance test option).

### 2.2 Operational workflow for CBUS Compliance Testing

The following are the high level steps you will need to follow MHL CBUS compliance testing.

### 2.2.1 Procedures covered in 980 Advanced Test Platform Quick Start Guide:

- 1. Remove the 980 from the shipping box.
- 2. Assemble the source device under test into your lab area and power it up. When using the optional passthrough feature to monitor between an HDMI or MHL source and an HDMI or MHL sink, assemble the display device as well.
- 3. Connect the 980 Protocol Analyzer power cable (provided) to a suitable outlet (110-240V 50/60Hz) and apply power to the 980.
- 4. (Optional not required if using the built-in display) Select a suitable PC to host the 980 GUI Manager application. A minimum of 512MB of RAM is recommended. (Note that you do not need a PC because you can use the built-in Front Panel display; however the external 980 GUI Manager provides you with a larger viewing area).

- 5. (Optional not required if using the built-in display) Determine how you are going to connect to the 980 Protocol Analyzer from the external 980 GUI Manager in order to operate the instrument:
  - o Put the 980 on your corporate network and enable DHCP using an available Ethernet patch cable, or...
  - o Connect directly with a host PC or laptop using the Ethernet crossover cable provided.
- 6. (Optional not required if using the built-in display) Assign an IP address to the 980/980B either directly or by enabling DHCP.
- 7. (Optional not required if using the built-in display) Download the latest 980 GUI Manager application from the Quantum Data website:

www.quantumdata.com/downloads/index.asp.

- 8. (Optional not required if using the built-in display) Install the 980 Manager application on your host PC.
- 9. (Optional not required if using the built-in display) Establish a connection to the 980 from the 980 Manager resident on your host PC.
- 10. (Optional not required if using the built-in display) Through the 980 Manager "Add" the 980/980B as an Instrument.

### 2.2.2 Procedures covered in this User Guide:

- 1. Connect the MHL device under test to the CBUS Compliance Test module.
- 2. Launch the 980 GUI Manager application, either the external 980 GUI Manager or the embedded 980 GUI Manager.
- 3. Launch the CBUS Compliance application in the 980 GUI Manager application.
- 4. Complete a (or load an existing) Capabilities Declaration Form (CDF) for the device under test using the **CDF Entry** panel.
- 5. Select the tests that you wish to run from the Test Selection panel.
- 6. Initiate the tests through the **Test Options / Review** panel.
- 7. View the detailed data for test failures if failures occur.
- 8. View the results in the **Test Results** panel under the **Navigator** panel.

### 2.3 Connector Description

This User Guide covers three configurations of the 980 rear panels with the MHL CBUS Compliance test module installed. Each illustration shows the CBUS Compliance test module installed in the 980/980B. Use the following table to identify the connector function and descriptions on your 980/980B system configuration.

980 Configurations	Information / Function	
CBUS Compliance Module - 980	The following is a description of each connector:	
	980 MHL CBUS module:	
	<ul> <li>A – MHL OUT connector for running tests on MHL CBUS compliance tests on dongle devices.</li> </ul>	
	<ul> <li>B – MHL IN connector for running tests on MHL CBUS compliance tests on source devices.</li> </ul>	
	<ul> <li>C – MHL IN connector and HDMI cable connection to run MHL CBUS compliance tests on sink devices.</li> </ul>	

980 Configurations	Information / Function
	QD Bus Board (99-000631):
	<ul> <li>D – Ethernet Tx connector use for HEAC function. Not used for CBUS compliance testing.</li> </ul>
	<ul> <li>E – BNC Trig OUT connector. Not used for CBUS compliance testing.</li> </ul>
	<ul> <li>F – BNC Trig IN connector. Not used for CBUS compliance testing.</li> </ul>
	<ul> <li>G – RCA OUT connector for SPDIF function. Not used for CBUS compliance testing.</li> </ul>
	<ul> <li>H – RCA IN connector for SPDIF function. Not used for CBUS compliance testing.</li> </ul>
	Lower Panel:
	<ul> <li>K – Ethernet port for connection to PC host for 980 GUI Manager application, telnet for command line control and FTP for transferring files.</li> </ul>
	<ul> <li>L – Various USB ports for transferring files and restoring system.</li> </ul>

Use the following table to identify the connector function and descriptions on your 980/980B system configuration.

980B Configurations	Information / Function
CBUS Compliance Module – 980B	The following is a description of each connector:
	980 MHL CBUS module:
	<ul> <li>A – MHL OUT connector for running tests on MHL CBUS compliance tests on dongle devices.</li> </ul>
	<ul> <li>B – MHL IN connector for running tests on MHL CBUS compliance tests on source devices.</li> </ul>
	<ul> <li>C – MHL IN connector and HDMI cable connection to run MHL CBUS compliance tests on sink devices.</li> </ul>
	QD Bus Board (99-000631):
	<ul> <li>D – Ethernet Tx connector use for HEAC function.</li> <li>Not used for CBUS compliance testing.</li> </ul>
	<ul> <li>E – BNC Trig OUT connector. Not used for CBUS compliance testing.</li> </ul>
	<ul> <li>F – BNC Trig IN connector. Not used for CBUS compliance testing.</li> </ul>
	<ul> <li>G – RCA OUT connector for SPDIF function. Not used for CBUS compliance testing.</li> </ul>
	<ul> <li>H – RCA IN connector for SPDIF function. Not used for CBUS compliance testing.</li> </ul>

980B Configurations	Information / Function
	Lower Panel:
	<ul> <li>I – Ethernet port for connection to PC host for 980 GUI Manager application, telnet for command line control and FTP for transferring files.</li> </ul>
	<ul> <li>J – Various USB ports for transferring files and restoring system.</li> </ul>

### **3 MHL CBUS Source Compliance Tests**

This chapter describes how to run the MHL CBUS source compliance tests. Please note you will have to purchase the optional 980 MHL CBUS Compliance Test module in order to run these tests. These procedures assume that you have the 980 Advanced Test Platform powered up and the 980 GUI Manager up and running.

The 980 MHL CBUS Compliance test module supports the following test sections in the MHL 1.2 and MHL 2.0 Compliance Test specifications:

#### 3.1 Electrical Tests

• 3.1.13 Rx Sense Impedance

#### 3.2 System Tests

- 3.2.6 EDID and Device Capability Register Tests
  - o 3.2.6.1 EDID Reading Test
  - 3.2.6.2 Device Capability Registers Test
- 3.2.7 RCP Sub-Command Tests
- 3.2.9 3D Tests
  - 3.2.9.1 3D Video Mode Support (MHL CTS 2.0 only)
- 3.2.10 UCP Sub-Command Tests (MHL CTS 2.0 only)

#### 3.3 CBUS Tests

- 3.3.1 CBUS Source DUT Common Test Equipment Setups
- 3.3.2 CBUS Source DUT Common Methodologies
- 3.3.3 Link Layer Electrical Source: Absolute Maximum Voltages
- 3.3.4 Link Layer Timing Source DUT Output: Pre-Discovery
- 3.3.5 Link Layer Electrical Source DUT Output: Discovery
- 3.3.6 Link Layer Timing Source DUT Output: Discovery
- 3.3.7 Link Layer Electrical Source DUT Output: Arbitration/Sync/Data Signaling
- 3.3.8 Link Layer Timing Source DUT Output: Arbitration/Sync/Data in Nanoseconds
- 3.3.9 Link Layer Timing Source DUT Output: Arbitration/Sync/Data in Bit Times
- 3.3.10 Link Layer Timing Source DUT Output: Link-Level NACK
- 3.3.11 Link Layer Timing Source DUT Output: ACK
- 3.3.12 Link Layer Timing Source DUT Output: Bus Re-Arbitration
- 3.3.13 Link Layer Behavior Source DUT Output: Ill-formed packets
- 3.3.14 Link Layer Timing Source DUT Input: Discovery
- 3.3.15 Link Layer Electrical Source DUT Input: Arbitration/Sync/Data signaling
- 3.3.16 Link Layer Timing Source DUT Input: Arbitration
- 3.3.17 Link Layer Timing Source DUT Input: Data
- 3.3.18 Link Layer Timing Source DUT Input: NACK
- 3.3.19 Link Layer Timing Source DUT Input: ACK
- 3.3.20 Link Layer Timing Source DUT Input: Bus Re-Arbitration

- 3.3.21 Link Layer Behavior Source DUT Input: Ill-formed packets
- 3.3.22 Link Layer Timing Source DUT Input: Disconnect
- 3.3.23 Link Layer Electrical Source DUT VBUS Control

#### 6.3 CBUS Common Tests

- 6.3.1 MSC Source and Sink DUT Input: Device Register Space Contents; Reads
- 6.3.2 MSC Source and Sink DUT Output: NACK Packet Response to MSC\_MSG
- 6.3.3 MSC Source and Sink DUT Output: Never Initiates Bad Commands
- 6.3.4 MSC Source and Sink DUT Output: NACK Packet Response to MSC\_MSG
- 6.3.5 MSC Source and Sink DUT Output: Never Initiates Bad Commands
- 6.3.6 MSC Source and Sink DUT Output: Errors and Exceptions
- 6.3.7 MSC Source and Sink DUT Output: Disconnect
- 6.3.8 MSC Source and Sink DUT Input: Device Register Space Contents; Writes
- 6.3.9 MSC Source and Sink DUT Input: Vendor Specific and Reserved Header Values
- 6.3.10 MSC Source and Sink DUT Input: Normal Commands
- 6.3.11 MSC Source and Sink DUT Input: Errors and Exceptions
- 6.3.12 MSC Source and Sink DUT Input: Argument Timeouts
- 6.3.13 MSC Source DUT Output: Never Initiates Bad Commands
- 6.3.14 MSC Source DUT Input: Normal Commands
- 6.3.17 DDC Source DUT Output; DUT Never Sends Illegal DDC Command
- 6.3.18 DDC Source DUT Output; Normal Operation
- 6.3.19 DDC Source DUT Output; Illegal Responses

### 3.1 Workflow for running the MHL CBUS Source Compliance Tests

The list below is the high level workflow for running the MHL CBUS Source Compliance Tests. Note that the installation of the external 980 GUI Manager and the Ethernet session are optional; you can run the compliance tests through the embedded GUI Manager.

- 1. Power up the 980. Refer to the procedures in 980 Advanced Test Platform Quick Start Guide available from the quantum data website on the downloads page.
- 2. (Optional; only necessary if using the external 980 GUI Manager) Establish an Ethernet/IP connection between the external 980 GUI Manager and the 980.
- Connect the MHL source device under test to the CBUS Rx ports on the 980 MHL CBUS Compliance Test module.
- 4. Complete a (or load an existing) Capabilities Declaration Form (CDF) for the device under test using the **CDF Entry** panel.
- 5. Select the tests that you wish to run from the **Test Selection** panel.
- 6. Initiate the tests through the **Test Options / Review** panel.
- 7. View the detailed data for test failures if failures occur.
- 8. View the results in the **Test Results** panel under the **Navigator** panel.

### 3.2 Making the physical MHL connections

This subsection describes the physical MHL connections required to run the MHL CBUS source compliance tests.



Connections for MHL CBUS source compliance test - 980

#### To make the physical MHL connections:

This procedure assumes that you have assembled the 980 with the MHL CBUS Compliance Test module and the MHL source device under test and applied power to all these devices. Refer to the procedures below and the diagram above.

1. Connect your MHL source device under test to the MHL IN connector on the 980 MHL CBUS Compliance Test module. Use the short (30 centimeter) MHL cable provided by Quantum Data.

### **3.3** Completing the CDF

Use the following procedures to complete the CDF for the MHL CBUS source compliance tests.

**Note**: The example workflows and screens use MHL 2.0 except where noted. Workflow and screens are similar for testing MHL 1.2 devices.

#### To complete the CDF:

1. From the **View** menu, enable viewing of the **MHL CBUS Src CT** panel.

File Edid Instrument Options	Compliance View	Help	
💷 Generator 🔃 ACA	HDMI 🕨	1	
Capture 😤 Navigat	MHL 🕨	🔯 So	ource Test
Captures St Compliant 1		🔯 Si	nk Test
	Segment	🔯 D	ongle Test
🖻 🖾 🗶 🕲 😫		🔯 Cl	BUS Source Test
Name Date / Time		🔯 C	BUS Sink Test
▲ Capture		🔯 C	BUS Dongle Test

2. Select the **CDF Entry** panel as shown below.

🗄 Event Plot 🔯 HDMI Src CT 1.4b 🔯 CBUS Src CT 2.0 🕱 🛛 🗖 🗖					
CDF Entry Selection Freview					
CDF File: < not saved>					
🔒 General 💿 Registers 💿	RCP Rcv   RCP Send  RCP LD Map  UCP Rcv (2.0)  UCP Send (2.0)  SD Video (2.0)				
Manufacturer or Model field ca	in not be blank.				
CDF_CTS_VERSION	CTS Version to test against. 1.2  2.0				
CDF_MFR_NAME	What is the product manufacturer's name?				
	What is the model name/number of the product?				
CDF_SRC_POWERED	Can the Source drive the VBUS? ① Yes ③ No				
CDF_SRC_CBUS_THRESHOLD_V	Voltage at which CBUS Timing Measurements should be taken. This voltage should be halfway between the HIGH and LOW CBUS voltages for data driven by this device. This will be related to the device's VOH.         0.90       V (0.75 to 1.05)				
CDF_PROC_SET_ACTIVE	Set Device into Active Mode for Discovery Tests. Edit Procedure				
CDF_PROC_SET_STANDBY	Set Device into Standby-Discover Mode. Edit Procedure				

3. To create a new CDF, click on the **New** activation button.

You will be prompted with a confirmation that you want to start a new CDF and reset the values. Click **OK** to proceed.



4. To open an existing CDF, click on the **Open** activation button.

You will be prompted with a dialog box that enables you to open a CDF. Select a CDF and then **OK** to proceed.

**Note**: You can save these CDFs to your PC for use on other PCs and by other colleagues.

С	CDF Editor				
	🕸 Open CDF File				
Select a CDF to open in the CDF editor.					
	C Acme_XYW_CDF				
	Cancel Ok				

5. Complete the items in the **General** tab of the CDF Entry panel shown below. Note that you will have to complete the essential fields in order to proceed. A read status message will appear indicating if you have not completed all the essential fields. This is shown in the example below.

You can enter helpful information using the "Edit Procedure" dialog box. The information entered into this dialog box will appear during the test and can be helpful to instruct users on running a particular test.

🔠 Event Plot 🔯 HDMI Src CT 1.4	4b 🔯 CBUS Src CT 2.0 🕱			
🖄 CDF Entry 🖌 Test Selection 🕨 Test Options / Preview				
Copen New 🔛 Save	e CDF File: <not saved=""></not>			
😔 General 💿 Registers 💿	RCP Rcv          • RCP Send          • RCP LD Map          • UCP Rcv (2.0)          • UCP Send (2.0)          • 3D Video (2.0)			
Manufacturer or Model field ca	an not be blank.			
CDF_CTS_VERSION	CTS Version to test against.			
CDF_MFR_NAME	What is the product manufacturer's name?			
CDF_MODEL_NUMBER	What is the model name/number of the product?			
CDF_SRC_POWERED	Can the Source drive the VBUS? ◎ Yes ◎ No			
CDF_SRC_CBUS_THRESHOLD_V	Voltage at which CBUS Timing Measurements should be taken. This voltage should be halfway between the HIGH and LOW CBUS voltages for data driven by this device. This will be related to the device's VOH.         0.90       V (0.75 to 1.05)	the		
CDF_PROC_SET_ACTIVE	Set Device into Active Mode for Discovery Tests.           Edit Procedure			
CDF_PROC_SET_STANDBY	Set Device into Standby-Discover Mode. Edit Procedure			

When you have entered in all the required fields the error indication will go away as shown in the example below.

Event Plot 🔯 HDMI Src CT 1.4b 🔯 CBUS Src CT 2.0 😣	
Second CDF Entry of Test Selection Freview	
CDF File: < not saved>	
General     Registers     RCP Rcv     RCP Send     RCP LD Map     UCP Rcv (2.0)     UCP Send (2.0)     3D Video (2.0)	
CDE CTS VERSION	
CDF_MFR_NAME What is the product manufacturer's name?	
Acme	-
CDF_MODEL_NUMBER What is the model name/number of the product? XYZ	
CDF SRC POWERED Can the Source drive the VBUS?	
● Yes ◎ No	_
Voltage at which CBUS Timing Measurements should be taken. This voltage should be halfway between the	•
0.90 V (0.75 to 1.05)	
Set Device into Active Mode for Discovery Tests.	
CDF_PROC_SET_ACTIVE Edit Procedure	
Set Device into Standby-Discover Mode.	
CDF_PROC_SET_STANDBY Edit Procedure	

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#### 6. Complete the items in the **Registers** tab.

뒢 Event Plot 🔯 HDMI Src CT :	1.46 🔯 CBUS Src CT 2.0 🛛	-	- 0
🕲 CDF Entry 🗹 Test Select	tion 🕨 Test Options / Preview	v	
Copen New 🔛 Sa	CDF File: <not saved=""></not>		
General     Registers	RCP Rcv RCP Send	RCP LD Map O UCP Rcv (2.0) UCP Send (2.0) 3D Video (2.0)	
	Declare the expected value of	of each of the DUT's Capability Registers.	*
	Register: MHL_VERSION	Field: MHL_VER_MAJOR	
CDF_CR_MHL_VER_MAJOR	1	]	
	Register: MHL_VERSION	Field: MHL_VER_MINOR	-
CDF_CK_WHL_VEK_WINOK	0	]	Ξ
	Register: DEV_CAT Field: DEV	/_TYPE	
CDF_CR_DEV_TYPE	🔘 (1) Sink 💿 (2) Source 🔘	(3) Dongle	
CDE CR ADOPTER ID H	Register: ADOPTER_ID_H	Field: ADOPTER_ID_H	
	0	00 - FF	
CDE CR ADOPTER ID I	Register: ADOPTER_ID_L	Field: ADOPTER_ID_L	
	0	00 - FF	_
CDF CR DEVICE ID H	Register: DEVICE_ID_H	Field: DEVICE_ID_H	
	0	00 - FF	-
CDF CR DEVICE ID L	Register: DEVICE_ID_L	Field: DEVICE_ID_L	
	0	00 - FF	-
CDF_CR_BANDWIDTH	Register: BANDWIDTH	Field: BANDWIDTH	
	15	27	-
CDF_CR_INT_SIZE	Register: INT_STAT_SIZE	Field: INT_SIZE	
413		413	-
CDF_CR_STAT_SIZE	Register: INT_STAT_SIZE	Field: STAT_SIZE	
4 4.13		-	
CDF_CR_SP_SIZE	Register: SCRATCHPAD_SIZE	Field: SP_SIZE	
	U	0.01.10/04	-

7. Complete the items in the **RCP Rcv** tab.

You can enter helpful information using the "**Edit Procedure**" dialog box. The information entered into this dialog box will appear during the test. You can enter in the expected behavior for each supported command so that the test engineer can verify that the source DUT behaves properly when receiving the various RCP commands.

🗄 Event Plot 🔯 HDMI Src CT 1.4b 🔯 CBUS Src CT 2.0 🕱 🗧 🗖	3)
🔯 CDF Entry 🖌 Test Selection 🕨 Test Options / Preview	
CDF File: < not saved>	
General      Regir      RCP Rcv      RCP Send      RCP LD Map      UCP Rcv (2.0)      UCP Send (2.0)      SD Video (2.0)	
CDF_RCP_RECEIVE       Does the DUT receive RCP?         If yes, provide expected behavior for each supported RCP command below.         Image: CDF_RCP_RECEIVE         Image: CDF_RCP_RCF_RCF_RCF_RCF_RCF_RCF_RCF_RCF_RCF_RCF	
Select the RCP commands the DUT can receive. Specify the expected behavior for each supported command so that the Test Engineer can verify the correct behavior when each RCP command is received by the DUT.	
CDF_RCP_RCV_BEHAVIOR_00     0x00: Select () Required By: GUI       Image: CDF_RCP_RCV_BEHAVIOR_00     Edit Behavior	
CDF_RCP_RCV_BEHAVIOR_01       0x01: Up ()         Required By: GUI         Image: Supported?         Edit Behavior	
CDF_RCP_RCV_BEHAVIOR_02     0x02: Down ① Required By: GUI       V     Supported?   Edit Behavior	
CDF_RCP_RCV_BEHAVIOR_03       0x03: Left ①         Required By: GUI         Image: Supported?	

8. Complete the items in the **RCP Send** tab.

You can enter helpful information using the "**Edit Procedure**" dialog box. The information entered into this dialog box will appear during the test and can be helpful to instruct a test engineer on how to set up a device in order to run a particular test. In the example below you would enter in procedural information which a test engineer could use to cause the source to issue the various RCP commands.

🗄 Event Plot 🔯 HDMI Src CT 1.4b 🔯 CBUS Src CT 2.0 🛛 🖓 🖓
😂 CDF Entry 🧹 Test Selection 🕨 Test Options / Preview
CDF File: < not saved>
General     Registers     RCP Rcv     RCP Send     PRCP LD Map     UCP Rcv (2.0)     UCP Send (2.0)     SD Video (2.0)
CDF_RCP_SEND Does the DUT send RCP: If yes, provide procedures each supported RCP command below.
Select the RCP commands the DUT can send. Specify the procedure for each supported command so that the Test Engineer can force the DUT to output each RCP command,using these detailed steps and the DUT's user interface.
CDF_RCP_SEND_PROCEDURE_00     Ox00: Select ()       Image: CDF_RCP_SEND_PROCEDURE_00     Image: CDF_RCP_SEND_PROCEDURE_00
CDF_RCP_SEND_PROCEDURE_01       0x01: Up ()         Image: CDF_RCP_SEND_PROCEDURE_01       Image: CDF_RCP_SEND_PROCEDURE_01
CDF_RCP_SEND_PROCEDURE_02       0x02: Down ()         Image: CDF_RCP_SEND_PROCEDURE_02       Image: CDF_RCP_SEND_PROCEDURE_02
CDF_RCP_SEND_PROCEDURE_03 Ox03: Left  Supported? Edit Procedure

9. Complete the items in the **RCP LD Map** tab.

You can enter helpful information using the "Edit Procedure" dialog box. The information entered into this dialog box will appear during the test to assist the test engineer. In the example below you would enter in procedural information which a test engineer could use to force the source into the proper mode for further testing of each logical device.

🖶 Event Plot 🔯 HDMI Src CT 1.4b 🔯 CBUS Src CT 2.0 🛛 🖓				
🔯 CDF Entry 🗹 Test Selection 🕨 Test Options / Preview				
CDF File: < not saved>				
General     Registers     RCP Rcv     RCP Send     RCP LD Map     UCP Rcv (2.0)     UCP Send (2.0)     SD Video (2.0)				
CDF_LOG_DEV_MAP_CHANGE © Yes © No				
Add as many settings as the DUT supports using the "Add" button below. For each, define a procedure so that the Test Engineer can force the DUT into each of these modes for further testing of each Logical Device.				
Add Kemove All				
CDF_PROC_LOG_DEV_MAP_1 X VIDEO AUDIO MEDIA TUNER RECORD SPEAKER GUI				

10. Complete the items in the **UCP Rcv** tab.

You can enter helpful information using the "Edit Procedure" dialog box. The information entered into this dialog box will appear during the test to assist a test engineer. You can enter in the expected behavior for each supported command so that the test engineer can verify that the source DUT behaves properly when receiving the various UCP commands.

🗄 Event Plot 🔯 HDMI Src CT 1.4b 🔯 CBUS Src CT 2.0 🛛	, 🗆
CDF Entry V Test Selection F Test Options / Preview	
CDF File: < not saved>	
General     Registers     RCP Rcv     RCP Send     RCP LD Map     UCP Rcv (2.0)     UCP Send (2.0)     SD Video (2.0)	
CDF_UCP_RECV_SUPPORT Does the DUT support receiving UCP sub-commands?  Yes No	
CDF_UCP_RECV_APPLICATION     Edit Procedure	
UCP Commands	
Add (# of Entries: 1)	
Command #01	
Hex Byte Data:	

11. Complete the items in the UCP Send tab.

🗄 Event Plot 🔯 HDMI Src CT 1.4b 🔯 CBUS Src CT 2.0 🕱	- 0
😂 CDF Entry 🧹 Test Selection 🕨 Test Options / Preview	
CDF File: < not saved>	
General     Registers     RCP Rcv     RCP Send     RCP LD Map     UCP Rcv (2.0)     UCP Send (2.0)     O     3D Video (2.0)	
CDF_UCP_SEND_SUPPORT Does the DUT support sending UCP sub-commands? Yes ONo	
CDF_UCP_SEND_APPLICATION     Edit Procedure	
UCP Commands	
Add (# of Entries: 1)	
<b>X</b> Command #01	
Hex Byte Data:	

12. Complete the items in the **3D Video** tab.

🔠 Event Plot 🔯 HDMI Src CT 1.4b 🔯 CBUS S	irc CT 2.0 🛛	_				- 8
🕲 CDF Entry 🧹 Test Selection 🕨 Test O	ptions / Preview					
CDF File: < not saved>						
General     Registers     RCP Rcv	RCP Send 🛛	RCP LD Map	● UCP Rcv (2.0) ● UCP Set	nd (2.0)	3D Video (2.0)	
CDF_VIDEO_3D	Does the DUT s ◎ Yes ◎ No	support 3D v	rideo?			
	Supported No	rmal Mode	3D Video Formats			
CDF_VIDEO_1280x720P_60_3D_Top_Bottom	🖲 Yes 🔘 No	(4)	1280x720p 59.94/60Hz,	3D, 1	Top-Bottom	
CDF_VIDEO_1280x720P_50_3D_Top_Bottom	🖲 Yes 🔘 No	(19)	1280x720p 50Hz,	3D, 1	Top-Bottom	
CDF_VIDEO_1920x1080p_24_Top_Bottom	🖲 Yes 🔘 No	(32)	1920x1080p 23.97/24Hz,	3D, 3	Top-Bottom	
CDF_VIDEO_1920x1080i_60_3D_Left_Right	🖲 Yes 🔘 No	(5)	1920x1080i 59.94/60Hz,	3D, 1	Left-Right	
CDF_VIDEO_1920x1080i_50_3D_Left_Right	🖲 Yes 🔘 No	(20)	1920x1080i 50Hz,	3D, 1	Left-Right	
CDF_VIDEO_1280x720P_60_3D_Frame	🖲 Yes 🔘 No	(4)	1280x720p 59.94/60Hz,	3D, 1	Frame-Sequentia	1
CDF_VIDEO_1280x720P_50_3D_Frame	🖲 Yes 🔘 No	(19)	1280x720p 50Hz,	3D, 1	Frame-Sequentia	1
CDF_VIDEO_1920x1080p_24_Frame	Yes ONO	(32)	1920x1080p 23.97/24Hz,	3D, 1	Frame-Sequentia	1
Supported PixelPacked Mode 3D Video Formats						
CDF_VIDEO_1280x720P_60_3D_Top_Bottom	🔘 Yes 🔘 No	(4)	1280x720p 59.94/60Hz,	3D, 1	Top-Bottom	
CDF_VIDEO_1280x720P_50_3D_Top_Bottom	🔘 Yes 🔘 No	(19)	1280x720p 50Hz,	3D, 3	Top-Bottom	

13. Save the CDF. A confirmation box with a default name will appear as shown below. Edit the name if necessary and click OK.

Save CDF	
😂 CDF Name	
Enter a name for the CDF	
Acme_XYZ_Source_CDF	
<sup>™</sup> My980_Source_CDF <sup>™</sup> MyCDF_Src1 <sup>™</sup> SG_Phone_CDF	
Cancel 📀 Ok	

The name of the CDF will appear next to the Save button as shown below:

🗄 Event Plot 🔯 HDMI Src CT 1.4b 🔯 CBUS Src CT 2.0 🛛	
<sup>™</sup> CDF Entry ✓ Test Selection ► Test Options / Preview	
CDF File: Acme_XYZ_Source_CDF	
General     General     Registers     RCP Rcv     RCP Send     RCP LD Map     UCP Rcv (2.0)     UCP Send (2.0)     SD Video (2.0)	

You can then view the CDF or load other CDFs from the Navigator/Compliance view as shown below:



You can open for use these CDF files using the right click **Open** menu item as shown below. You can also delete a CDF or rename it. If you wish to view a text file of the CDF you can do so by selecting **View as Text**. In some cases you might want to share these files with other colleagues. Since these files are stored locally on your PC you can simply email them. Conversely if you wish to import a CDF file from another user for use on your application you can do that using the **Import** function on the right click menu also show below.



### 3.4 Selecting which tests to run

Use the following procedures to select the tests to run. There are multiple tabs which correspond to each section in the CTS.

**Note**: The example workflows and screens use MHL 2.0 except where noted. Workflow and screens are similar for testing MHL 1.2 devices.

#### To select the tests to run:

- 1. Select the **Test Selection** panel as shown below.
- 2. If you have an existing Test Selection option file saved you can recall that for use in your testing. Simply click on the **Open** activation button.

🗄 Event Plot 🔯 MHL Src CT 2.0 🔯 CBUS Src CT 2.0 🛛	
CDF Entry V Test Selection ptions / Preview	
Carlo Open Save Select All Tests Deselect All Tests	
▶ Source (3/41)         ▶ Common (0/67)         ▶ EDID/Registers (0/2)         ▶ RCP (0/2)         ▶ 3D (0/1)         ▶ UCP (0/2)	

A dialog box will appear as follows. Simply select the file and click on the **OK** activation button.

**Note**: You can save the Test Selection files to your host PC and transfer them to other PCs and for others to use.

MHL Src Compliance Test	
Øpen Test Selection File	
Select an Test Selection file to open.	
MHL_test_sels.xml	
Cancel Ok	

3. Complete the items in the Source tab of the Test Selection panel shown below.

For convenience you can Select All or Deselect All tests using the activation buttons provided.

Check box indicators inform how many tests in each section and how many are selected. Each tab (Source, Common or RCP) inform you of how many tests in that section have been selected.

Each test section list includes several tests. In the example shown below the 3.2.6 EDID and Device Capability Register Test section is selected and the specific tests in that section are then available to be selected.

Note: Some tests are run in background and cannot be deselected.

Source (3)	3/41) ▶ Common (0/67) ▶ EDID/Registers (0/2) ▶ RCP (0/2) ▶ 3D (0/1) ▶ UCP (0/2)		
3.1.1	TMDS Electrical Tests	0/1	
3.3.3	Link Layer Electrical: Absolute Maximum Voltages	2/2	
3.3.4	Link Layer Timing - DUT Output: Pre-Discovery	0/1	
3.3.5	Link Layer Electrical - DUT Output: Discovery	3/5	
> 3.3.6	Link Layer Timing - DUT Output: Discovery	0/4	
3.3.7	Link Layer Electrical - DUT Output: Arbitration/Sync/Data Signaling	0/5	
3.3.8	Link Layer Timing - DUT Output: Arbitration/Sync/Data in Nanoseconds	0/2	
3.3.9	Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times	1/2	1
3.3.10	Link Layer Timing - DUT Output: Link-Level NACK	0/1	
> 3.3.11	Link Layer Timing - DUT Output: ACK	0/2	
> 3.3.12	Link Layer Timing - DUT Output: Bus Re-Arbitration	1/3	
> 3.3.13	Link Layer Behavior - DUT Output: Ill-formed packets	2/2	
> 3.3.14	Link Layer Timing - DUT Input: Discovery	0/3	
> 3.3.15	Link Layer Electrical - DUT Input: Arbitration/Sync/Data signaling	0/1	
> 3.3.16	Link Layer Timing - DUT Input: Arbitration	0/2	
3.3.17	Link Layer Timing - DUT Input: Data	0/1	
> 3.3.18	Link Layer Timing - DUT Input: NACK	0/1	
> 3.3.19	Link Layer Timing - DUT Input: ACK	0/1	
> 3.3.20	Link Layer Timing - DUT Input: Bus Re-Arbitration	0/1	
> 3.3.21	Link Layer Behavior - DUT Input: III-formed packets	0/1	
> 3.3.22	Link Layer Timing - DUT Input: Disconnect	0/3	
3.3.23	Link Layer Electrical - DUT VBUS Control	0/3	-
✓ 3.3 Veri with	<b>.5.1: CBE-Source: Response to Initial Plug-in to MHL Device</b> fy correct Source DUT behavior when going from unplugged to Z[CBUS_SINK_DISCOVER] in the MHL range.		
3.3 Veri sub	<b>.5.2: CBE-Source: Response to Sink Priming Pulse to MHL device</b> fy correct Source DUT behavior when Sink HIGH-Z's the CBUS to invoke a new (second or sequent) CBUS Discovery, then attaches with ZICBUS_SINK_DISCOVERI within the MHL range.		

4. Complete the items in the **Common** tab of the **Test Selection** panel shown below.

For convenience you can Select All or Deselect All tests using the activation buttons provided.

CDE Entry			
2 CDI LIIUY	V Test Selection  Test Options / Preview		
🔁 Open 🗌	Save Select All Tests Deselect All Tests		
Source (3/	412 -> Common (67/67) -> EDID/Registers (0/2) -> RCP (0/2) -> 3D (0/1) -> UCP (0/2)		
6.3.1	- DUT Input: Device Register Space Contents; Reads	1/1	
► 6.3.2 <	MSC - DUT Output: Vendor-specific and Reserved Header Values	1/1	
6.3.3	MSC - DUT Output: Normal Commands	7/7	
▶ 6.3.4	MSC - DUT Output: NACK Packet Response to MSC_MSG	1/1	
6.3.5	MSC - DUT Output: Never Initiates Bad Commands	8/8	
▶ 6.3.6	MSC - DUT Output: Errors and Exceptions	5/5	
▶ 6.3.7	MSC - DUT Output: Disconnect	1/1	
▶ 6.3.8	MSC - DUT Input: Device Register Space Contents; Writes	2/2	
▶ 6.3.9	MSC - DUT Input: Vendor-specific and Reserved Header Values	1/1	
6.3.10	MSC - DUT Input: Normal Commands	8/8	
▶ 6.3.11	MSC - DUT Input: Errors and Exceptions	22/22	
▶ 6.3.12	MSC - DUT Input: Argument Timeouts	9/9	
▶ 6.3.13	MSC - DUT Output: Never Initiates Bad Commands	2/2	
▶ 6.3.14	MSC - DUT Input: Normal Commands	2/2	
▶ 6.3.17	DDC - DUT Output; DUT Never Sends Illegal DDC Command	2/2	
▶ 6.3.18	DDC - DUT Output; Normal Operation	4/4	
▶ 6.3.19	DDC - DUT Output; Illegal Responses	4/4	
			_
<ul> <li>6.3. Verify retur Capa</li> <li>6.3. Verify</li> </ul>	10.1: CBM: DUT receives (0x62) GET_STATE Command that if DUT responds appropriately when it receives a GET_STATE. It should the value defined in the MHL Spec as the value stored in the DEV_STATE bility Register, which is always 0.  10.2: CBM: DUT receives (0x63) GET_VENDOR_ID Command that if DUT responds appropriately when it receives a GET_VENDOR_ID.		

5. Complete the items in the EDID Registers tab of the Test Selection panel shown below.

🔠 Event Plot 🔯 MHL Src CT 2.0 🔯 CBUS Src CT 2.0 🕱	
CDF Entry 🗸 Test Selection 🕨 Test Options / Preview	
Copen Save Select All Tests Deselect All Tests	
▶ Source (3/41)         ▶ Common (67/67)         ▶ EDID/Registers (0/2)         ▶ 3D (0/1)         ▶ UCP (0/2)	
3.2.6.1: EDID Reading Test Verify that the DUT reads the EDID while the MHL link is being established and when the EDID is updated.	
✓ 3.2.6.2: Device Capability Registers Test Verify that the Device Capability Registers have accurate values.	

6. Complete the items in the **RCP** tab of the **Test Selection** panel shown below.

뒢 Event Plot 🔯 MHL Src CT 2.0 🔯 CBUS Src CT 2.0 🛛		
CDF Entry 🗸 Test Selection 🕨 Test Options / Preview		
Copen 🔚 Save Select All Tests Deselect All Tests		
► Source (3/41) ► Common (67/67) ► EDID/Registers (0/2) ► RCP (0/2) ► 3D (0/1) ► UCP (0/2)		
3.2.7.1: RCP Sub-Commands Receiving Test Verify that Source DUT responds to RCP sub-commands with the expected behavior based on the definitions in the MHL Specification, for each Logical Device claimed to be supported by the Source DUT.		
✓ 3.2.7.2: RCP Sub-Commands Transmitting Test Verify that the Source DUT outputs each RCP sub-command supported as identified in the CDF, demonstrating the proper opcode and sub-command.		

7. Complete the items in the **3D** tab of the **Test Selection** panel shown below.

🔁 Event Plot 🔯 MHL Src CT 2.0 🔯 CBUS Src CT 2.0 🛛	- 8
CDF Entry V Test Selection > Test Options / Preview	
Copen Save Select All Tests Deselect All Tests	
► Source (3/41) ► Common (67/67) ► EDID/Registers (0/2) ► RCP (0/2) ► 3D (0/1) ► UCP (0/2)	
3.2.9.1: 3D Video Mode Support (3D REQ) Verify that the Source DUT requests 3D video mode support data from the connected Sink.	
(CTS 2.0 Only)	

8. Complete the items in the UCP tab of the Test Selection panel shown below.

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#### - 8 🖶 Event Plot 隧 MHL Src CT 2.0 🔯 CBUS Src CT 2.0 🙁 CDF Entry Test Selection Test Options / Preview 🔀 Select All Tests 📃 Deselect All Tests 🚉 Open 🛛 🔡 Save Source (3/41) Common (67/67) EDID/Registers (0/2) RCP (0/2) 3D (0/1) UCP (0/2) 3.2.10.1: UCP Sub-Commands Receiving Test Verify that the DUT responds to valid UCP sub-commands by displaying the character or characters sent in the UCP command, or response to invalid UCP sub-commands by displaying an error message. (CTS 2.0 Only) 3.2.10.2: UCP Sub-Commands Transmitting Test Verify that the DUT sends valid UCP sub-commands by initiating the sending of UTF-8 characters in various formats through the user interface on the DUT. (CTS 2.0 Only)

9. You can save the Test Selection options using the **Save** activation button.

🗄 Event Plot 🔯 MHL Src CT 2.0 🔯 CBUS Src CT 2.0 🛛	- 8
CDF Entry 🗸 Test Selection 🕨 Test Options / Preview	
Copen Save elect All Tests Deselect All Tests	
► Source (3/41) ► Common (67/67) ► EDID/Registers (0/2) ► RCP (0/2) ► 3D (0/1) ► UCP (0/2)	

A dialog box will appear as follows. Simply assign a name and click on the OK activation button. Click Cancel to exit.

ſ	CBUS Src CT: Save Test Selections	
	Test Selection File	
	Enter a file name for the Test Selection.	
	My980_Source_Selection.xml	
	MHL_CBUS_DS.xml	
	Cancel Ok	

You can then view the Test Selection in the Navigator/Test Selections view as shown below. You can delete Test Selections and load Test Selections from this list as well.

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You can use the right click menu to open, delete or rename a Test Selection file as shown below.



### 3.5 Executing the MHL CBUS Source Compliance Tests

Use the following procedures to initiate the execution of an MHL CBUS Source Compliance test series.

**Note**: The example workflows and screens use MHL 2.0 except where noted. Workflow and screens are similar for testing MHL 1.2 devices.

#### To initiate a test series:

1. Select the **Test Options / Preview** panel as shown below.

🗄 Event Plot 🔯 MHL Src CT 2.0 🔯 CBUS Src CT 2.0 🕱	
🔯 CDF Entry 🗹 Test Selection 🕨 Test Options / Preview	
Test List	
📝 All 🗸 🕺 Instrument: My980 [192.168.254.163]	Execute Tests
Category / Test Name	× ^
3.2.6: EDID and Device Capability Register Test	
📳 3.2.6.1: EDID Reading Test	<b>V</b>
3.2.6.2: Device Capability Registers Test	V
▶ 3.2.9: 3D Test	=
3.2.9.1: 3D Video Mode Support (3D REQ)	V
3.2.10: UCP Sub-Command Tests	
3.2.10.1: UCP Sub-Commands Receiving Test	V
• Iter 01: Test all supported Commands.	V
3.2.10.2: UCP Sub-Commands Transmitting Test	V
• Iter 01: Test all supported Commands.	V
3.3.3: Link Layer Electrical: Absolute Maximum Voltages	
3.3.3.2: CBE-Source: VBUS Absolute Maximum Positive Voltage	V
📑 3.3.3.3: CBE-Source: CBUS Absolute Maximum Positive Voltage	<b>V</b>
3.3.5: Link Layer Electrical - DUT Output: Discovery	
3.3.5.1: CBE-Source: Response to Initial Plug-in to MHL Device	V
3.3.5.2: CBE-Source: Response to Sink Priming Pulse to MHL device	V
3.3.5.3: CBE-Source: Pre-Discovery Success Pull-up HIGH Voltage	V
3.3.9: Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times	5
3.3.9.2: CBT-Source: Continuous Monitor: Bit Timing Variation within a Packet	<b>V</b>
3.3.12: Link Layer Timing - DUT Output: Bus Re-Arbitration	
📑 3.3.12.3: CBT Source: Source Never Sends Too Many Back-to-Back Packets	<b>V</b>
3.3.13: Link Layer Behavior - DUT Output: Ill-formed packets	
3.3.13.1: CBT-Source: Source Never Sends Impulse Noise	V
3.3.13.2: CBT-Source: Source Never Sends Partial Packets	<b>V</b>
6.3.1: MSC - DUT Input: Device Register Space Contents; Reads	
6.3.1.1: CBM: Capability Regs; READ DEVCAP of Capability Register Contents	V
6.3.2: MSC - DUT Output: Vendor-specific and Reserved Header Values	
6.3.2.1: CBM: DUT Sends Vendor-Specific and Reserved Header Values	<b>V</b>
6.3.3: MSC - DUT Output: Normal Commands	
5.0.0 Control	V
5.0.3.3.2: CBM: DUT sends (0x63) GET VENDOR ID Command	V
5.3.3.3: CBM: DUT sends (0x6B) GET MSC ERRORCODE Command	

🗄 Event Plot 🔯 MHL Src CT 2.0 🔯 CBUS Src CT 2.0 😫		
🔯 CDF Entry 🗹 Test Selection 🕨 Test Options / Preview		
Test List		
Instrument:         My980 [192.168.254.163]	ecute Tes	sts
Category / Test Name	$\checkmark$	*
6.3.1: MSC - DUT Input: Device Register Space Contents; Reads 6.3.1.1: CBM: Capability Regs; READ DEVCAP of Capability Register Contents	<b>~</b>	-
6.3.2: MSC - DUT Output: Vendor-specific and Reserved Header Values		
2 0.3.2.1. Char. Dor Sends Vendor-Specific and Reserved header values	~	
6 3 3 1 CPM: DUT OUTPUT: NOTMAL COMMANDS		
6.3.3.1. CHA. DOI SERIES (0x62) GET STATE COMMAND	×	
6.3.3. CEM. DIT Sends (0x65) GT MSC ERRORCODE Command	1	-
6 3 3 4 CBM DIT Sends (0x6), SET INT/WRITE STAT Command	×	=
= 6.3.3.5: CBM: DUT sends (0x6C) WRITE BIRST Command	×	1
6.3.3.6: CBM: DUT sends (0x66) MSC MSG Command	×	
5.3.3.7: CBM: DUT sends (0x6A) GET DDC ERRORCODE Command	×	
► 6.3.4. MSC - DIF Output: NACK Packet Response to MSC MSC		
▶ 5.3.4.1: CBM: DUT Receives NACK to MSC MSG	<b>V</b>	-
6.3.5: MSC - DUT Output: Never Initiates Bad Commands		ſ
6.3.5.1: CBM: DUT Never Sends Reserved Commands	<b>V</b>	
🗏 6.3.5.2: CBM: DUT Never Sends Illegal Commands	<b>V</b>	
🗏 6.3.5.3: CBM: DUT Never Sends Data While No Command is Outstanding	$\checkmark$	
📙 6.3.5.4: CBM: DUT Never Sends (0x33) ACK packet While No Command is Outstanding	$\checkmark$	
📙 6.3.5.5: CBM: DUT Never Sends (0x34) NACK Packet While No Command is Outstandir	$\checkmark$	
🗏 🖪 6.3.5.6: CBM: DUT Never Sends (0x35) ABORT While No Command is Outstanding	$\checkmark$	
🛛 🗏 6.3.5.7: CBM: DUT Never Sends (0x32) EOF While No Command is Outstanding	$\checkmark$	
🗏 🖪 6.3.5.8: CBM: DUT never sends WRITE BURST Command without First Arbitrating	$\checkmark$	
6.3.6: MSC - DUT Output: Errors and Exceptions		
🗏 6.3.6.1: CBM: DUT Receives Bad Reply; Control instead of Data	$\checkmark$	
📑 6.3.6.2: CBM: DUT Receives Bad Reply; Data instead of Control	$\checkmark$	
📃 5.3.6.3: CBM: DUT Receives Bad Reply; Control, Control instead of Control, Data	×	
📑 6.3.6.4: CBM: DUT Receives Result Timeout	<b>V</b>	_
5.3.6.5: CBM: Verify No Next Command Until Hold-Off after ABORT Seen		
6.3.7: MSC - DUT Output: Disconnect		
5.3.7.1: CBM: DUT Receives Disconnect during Various Commands		-
6.3.8: MSC - DUT Input: Device Register Space Contents; Writes		-
THE AND A CONTRACT ALL AND THE AND	~	
2. (Optional) Review the list of tests for each category. If you wish to skip some of the tests. You can skip tests by clicking on the Check mark on the right side of the **Test Options / Preview** panel.

The screen shot below shows some of the tests that have been skipped (highlighted in yellow with a red X).

🗄 Event Plot 🔯 MHL Src CT 2.0 🔯 CBUS Src CT 2.0 🛛		
🔯 CDF Entry 🖌 Test Selection 🕨 Test Options / Preview		
Test List		
All V X Instrument: My980 [192.168.254.163]	Execute Tests	;
Category / Test Name	V .	^
A > 3.2.6: EDID and Device Capability Register Test		
B 3.2.6.1: EDID Reading Test	V	
> 🗏 3.2.6.2: Device Capability Registers Test	V	=
▲ ▶ 3.2.9: 3D Test		-
▶ 📑 3.2.9.1: 3D Video Mode Support (3D REQ)	V	
▲ ▶ 3.2.10: UCP Sub-Command Tests		
A 🔄 3.2.10.1: UCP Sub-Commands Receiving Test	×	-
X Iter 01: Test all supported Commands.	×	
A 🔄 3.2.10.2: UCP Sub-Commands Transmitting Test	V	
• Iter 01: Test all supported Commands.	$\checkmark$	
3.3.3: Link Laver Electrical: Absolute Maximum Voltages		
> 🗄 🚾 3.3.2: CBE-Source: VBUS Absolute Maximum Positive Voltage	$\checkmark$	
> 🔄 3.3.3: CBE-Source: CBUS Absolute Maximum Positive Voltage	$\checkmark$	
A > 3. 5: Link Laver Electrical - DUT Output: Discovery		
4 5.5.1: CBE-Source: Response to Initial Plug-in to MHL Device	×	
¥ Iter 01:	×	
> 3.3.5.2: CBE-Source: Response to Sink Priming Pulse to MHL device	V	
> 🔄 3.3.5.3: CBE-Source: Pre-Discovery Success Pull-up HIGH Voltage	$\checkmark$	
3.3.9: Link Laver Timing - DUT Output: Arbitration/Sync/Data in Bit Times	\$	
Bit Timing Variation within a Packet	$\checkmark$	
A > 3.3.12: Link Laver Timing - DUT Output: Bus Re-Arbitration		
Isotropy Back-to-Back Packets	$\checkmark$	
3.3.13: Link Laver Behavior - DUT Output: Ill-formed packets		
> 3.3.13.1: CBT-Source: Source Never Sends Impulse Noise	$\checkmark$	
> 🗄 3.3.13.2: CBT-Source: Source Never Sends Partial Packets	$\checkmark$	
6.3.1: MSC - DUT Input: Device Register Space Contents; Reads		
▶ 🗏 6.3.1.1: CBM: Capability Regs; READ DEVCAP of Capability Register Contents	$\checkmark$	
▲ ► 6.3.2: MSC - DUT Output: Vendor-specific and Reserved Header Values		
▶ 6.3.2.1: CBM: DUT Sends Vendor-specific and Reserved Header Values	V	
6.3.3: MSC - DUT Output: Normal Commands	1	
► = 6.3.3.1: CBM: DUT sends (0x62) GET STATE command		
▶ ■ 6.3.3.2: CBM: DUT sends (0x63) GET VENDOR ID Command	V	Ŧ
3.3.1.3.2: CBT-Source: Source Never Sends Partial Packets		

3. Click on the Execute Tests activation button to initiate the test suite. You will be prompted for a name for the tests. This dialog box is shown below.

CBUS Src CT Results
📃 Test Results Name
Execute CBUS Src Compliance Tests on Instrument: My980 @ 192.168.254.163
Enter a name for the Test Results.
Acme_XYZ_MHL_CBUS_Source
<ul> <li>05_02_2012_14_18_59</li> <li>Acme_MHL_Tests</li> <li>MHL_CBUS_04_30_2012_17_07_55</li> <li>MHL_CBUS_2_04_30_2012_17_07_55</li> <li>MHL_CBUS_3_04_30_2012_17_07_55</li> </ul>
Cancel Ok

A screen will appear instructing you on how to connect your MHL CBUS source device for testing. A sample screen is shown below:



During the test, the test results are shown. There is a progress arrow which points to the test that is currently being run. The lower panel **Test Log** shows the testing activity as it occurs. Refer to the screen examples below.

CBUS Src Compliance Test (1.2): "Acme\_MHL\_Tests" V All 🗶 All 🔄 Reset Status Category / Test Name Status × % Iter 01: # 3.3.5.2: CBE-Source: Response to Sink Priming Pulse to MHL device User Skipped ↓ Otter 0:
 ▲ 3.3.5.3: CBE-Source: Pre-Discovery Success Pull-up HIGH Voltage 1 Fail Incomplete 💥 Iter 01: User Skipped ▲ [] 3.3.5.4: CBE-Source: Discovery Pulse Drive HIGH Voltage \varTheta Iter 01: 1 Pass ▲ 🗏 3.3.5.5: CBE-Source: Discovery Pulse float LOW Voltage Das \varTheta Iter 01: Pass ▲ ► 3.3.9: Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times 3.3.12: Link Layer Timing - DUT Output: Bus Re-Arbitration Packets > 3.3.13: Link Laver Behavior - DUT Output: Ill-formed packets
 > 3.3.13.1: CBT-Source: Source Never Sends Impulse Noise
 > 3.3.13.2: CBT-Source: Source Never Sends Partial Packets 3.3.14: Link Layer Timing - DUT Input: Discovery • 3.3.14.1: CBT-Source: Discovery; Sink Responds Correctly; Time to Source Pull-up Change \_ \varTheta Iter 01: Fail Incomplete User Skipped In Progress ▲ 🗏 3.3.14.2: CBT-Source: Discovery; Sink Responds Late IGH  $\checkmark$ 🔶 Iter 01: In Progress Message Line • 0041 Test 3.3.5.5 Iter 01 0042 - Test 3.3.14.1-01 0043 Retrieving test results. Processing test results. Saving the test logs. • 0047 Test 3.3.14.1 Iter 01 -> Fail • 0048 0049 Cancel the Compliance Test Pause Test Execution

	Test List		
🖉 AII 🔀 AII 🔍	Reset Status		
Category / Te	st Name		Status
> 🔵 Iter 01	:	Image: A start of the start	Pass
4 3.3.22.2	2: CBT-Source: Remove MHL+/- Pull-up for More than Glitch Reject Time		Pass
þ 🔵 Iter 01	1	V	Pass
⊿ 📃 3.3.22.3	3: CBT-Source: Time from Disconnect until VOUT Falls		Fail
) 😝 Iter 01	:	<b>V</b>	Fail
▶ 6.3.2: MS	SC - DUT Output: Vendor-specific and Reserved Header Values		
▶ 🖪 6.3.2.1	: CBM: DUT Sends Vendor-Specific and Reserved Header Values		Pass
▶ 6.3.3: MS	SC - DUT Output: Normal Commands		
4 🖪 6.3.3.1:	: CBM: DUT sends (0x62) GET STATE command		In Progress
Iter 01	:	$\checkmark$	In Progress
6.3.3.2	: CBM: DUT sends (0x63) GET VENDOR ID Command		Not Tested
6.3.3.3	: CBM: DUT sends (0x6B) GET MSC ERRORCODE Command		Not Tested
6.3.3.4	: CBM: DUT sends (0x60) SET INT/WRITE STAT Command		Not Tested
▶ 📑 6.3.3.5	: CBM: DUT sends (0x6C) WRITE BURST Command		Not Tested
6.3.3.6	: CBM: DUT sends (0x68) MSC MSG Command		Not Tested
6.3.3.7	: CBM: DUT sends $(0x6A)$ GET DDC ERRORCODE Command		Not Tested
▶ 6.3.5: MS	SC - DUT Output: Never Initiates Bad Commands		
6.3.5.1	: CBM: DUT Never Sends Reserved Commands		Pass
▶ 🖪 6.3.5.2	: CBM: DUT Never Sends Illegal Commands		Pass
▶ 📑 6.3.5.3	: CBM: DUT Never Sends Data While No Command is Outstanding		Pass
▶ 📃 6.3.5.4	: CBM: DUT Never Sends (0x33) ACK packet While No Command is Outstanding		Pass
▶ 📑 6.3.5.5	: CBM: DUT Never Sends (0x34) NACK Packet While No Command is Outstanding		Pass
▶ 📑 6.3.5.6	: CBM: DUT Never Sends (0x35) ABORT While No Command is Outstanding		Pass
	Test Log		
ne	Message		
0065	Test 3.3.22.2 Iter 01 -> Pass		
0066	Test 3.3.22.3-01		
0067			
0068	Retrieving test results.		
0069	Processing test results.		
0070	Saving the test logs.		
0071	Test 3.3.22.3 Iter 01 -> Fail		
0072	Test 6.3.3.1-01		
0073			

CBUS Src Compliance Test (1.2): "Acme\_MHL\_Tests"

Test List			
Category / Test Name	×	Status	
▲ ■ 3.3.14.3: CBT-Source: Discovery; Sink Never Drives MHL+/- HIGH		Pass	
V Iter 01:	V		
• 3.3.22: Link Laver Timing - DUT Input: Disconnect		Daga	_
→ 15.3.22.1: CBT-Source: Remove MHL+/- Pull-ups for Less than Glitch Reject TI	me d	Pass	
→ Titer of:		Pass	
► S.S.ZZ.Z. CBI-SOURCE. REMOVE MALTY- Full-up for More than Gitten Reject Time		Page	
↓ 3 3 2 2 3. CBT-Source: Time from Disconnect until VOLT Falls	~	Fail	
The Discourse of the fight processing of the fight of the		Fail	
• DUT discovered in 3360 ms.		0.000	
simulated wide glitch: delay=499999 us; duration=3476034 us			
• 😔 01: DUT does enable VBUS as part of Discovery		Fail	
VBUS not driven by DUT			
$\triangleright \ominus 02$ : DUT does react to the long MHL glitch by floating CBUS		Pass	
● 03: DUT does stop driving VBUS within TSRC:CBUS TMDS DIS(max) from the	end of the M	Pass	
▲ ▶ 6.3.2: MSC - DUT Output: Vendor-specific and Reserved Header Values			
🛛 📙 6.3.2.1: CBM: DUT Sends Vendor-Specific and Reserved Header Values		Pass	
6.3.3: MSC - DUT Output: Normal Commands			
4 📙 6.3.3.1: CBM: DUT sends (0x62) GET STATE command		Pass	
↓	×	Pass	
▲ 📑 6.3.3.2: CBM: DUT sends (0x63) GET VENDOR ID Command		In Progress	
Piter 01:	×	In Progress	
▶ 📑 6.3.3.3: CBM: DUT sends (0x6B) GET MSC ERRORCODE Command		Not Tested	
Test Log			
Line Message			
• 0071 Test 3.3.22.3 Iter 01 -> Fail			
• 0072 Test 6.3.3.1-01			
• 0073 Executing the test.			
• 0074 Retrieving test results.			
• 0075 Processing test results.			
• 0075 Saving the test logs.			
• 0077 Test 6.3.3.1 Iter 01 -> Pass			
• 0078 Test 6.3.3.2-01			
Executing the test.			
Cancel the Compliance Test			
Ouantum Data 980 Manager - Version 4	1,5,29		

You can cancel the compliance test or pause at any time. If you pause the test you can resume later at any time even if you exit the 980 Manager application. Refer to the following screen example.

CBUS Src Compliance Test (1.2): "Acme\_MHL\_Tests"

Test List		
🖉 All 🐘 All 🔄 Reset Status		
Category / Test Name	<b>V</b>	Status
E 6.3.3.4: CBM: DUT sends (0x60) SET INT/WRITE STAT Command		Pass
▶ \varTheta Iter 01:	V	Pass
E 6.3.3.5: CBM: DUT sends (0x6C) WRITE BURST Command		Pass
▷ 😝 Iter 01:	$\checkmark$	Pass
5.3.3.6: CBM: DUT sends (0x68) MSC MSG Command		Pass
▶ 😝 Iter 01:	$\checkmark$	Pass
▲ 📑 6.3.3.7: CBM: DUT sends (0x6A) GET DDC ERRORCODE Command		In Progress
iter 01:		In Progress
6.3.5: MSC - DUT Output: Never Initiates Bad Commands		
E 6.3.5.1: CBM: DUT Never Sends Reserved Commands		Pass
E 6.3.5.2: CBM: DUT Never Sends Illegal Commands		Pass
E 6.3.5.3: CBM: DUT Never Sends Data While No Command is Outstanding		Pass
E 6.3.5.4: CBM: DUT Never Sends (0x33) ACK packet While No Command is Outstanding		Pass
$\triangleright = 6.3.5.5$ : CBM: DUT Never Sends (0x34) NACK Packet While No Command is Outstanding		Pass
▷ ■ 6.3.5.6: CBM: DUT Never Sends (0x35) ABORT While No Command is Outstanding		Pass
$\triangleright = 6.3.5.7$ : CBM: DUT Never Sends (0x32) EOF While No Command is Outstanding		Pass
6.3.8: MSC - DUT Input: Device Register Space Contents; Writes		
E 6.3.8.1: CBM: Interrupt Regs; SET INT (0x60); Valid Registers Respond		Not Tested
▶ 6.3.8.2: CBM: Status Regs; WRITE STAT (0x60); Valid Registers Respond		Not Tested
6.3.13: MSC - DUT Output: Never Initiates Bad Commands		<b>D</b> = = =
6.3.13.1: CBM-Source: Source DUT Never Sends (0x64) SET HPD Command		Pass
▶ 6.3.13.2: CEM-Source: Source DUT Never Sends (0x65) CLR HPD Command		Pass
6.3.17: DDC - DUT Output; DUT Never Sends Illegal DDC Command		
Test Log		
ne Message		
D101 Test 6.3.3.5 Iter 01 -> Pass		
0102 Test 6.3.3.6-01		
D103 Executing the test.		
20104 Retrieving test results.		
0105 Processing test results.		
0106 Saving the test logs.		
Test 6.3.3.6 Iter 01 $\rightarrow$ Pass		
0108 Test 6.3.3.7-01		
0109 Executing the test.		

You can view the details of failures when they occur by exposing the navigation arrows on the left. Examples are shown on the following two screens.



CBUS Src Compliance Test (1.2): "Acme\_MHL\_Tests"

Test List			
🖌 All 🙀 All 🔗 Reset Status			
Category / Test Name	×	Status	
$\blacktriangleright$ 6.3.2: MSC - DUT Output: Vendor-specific and Reserved Header Values			
> 5.3.2.1: CBM: DUT Sends Vendor-Specific and Reserved Header Values		Pass	
6.3.3: MSC - DUT Output: Normal Commands			
▲ ■ 6.3.3.1: CBM: DUT sends (0x62) GET STATE command		Pass	
▷ ↓ Iter 01:	×	Pass	
4 🗏 6.3.3.2: CBM: DUT sends (0x63) GET VENDOR ID Command		Pass	
▶ 😝 Iter 01:	V	Pass	
4 📙 6.3.3.3: CBM: DUT sends (0x6B) GET MSC ERRORCODE Command		Pass	
ه 😝 Iter 01:	V		
<ul> <li>Pass 1, watching for 0x56b; tester response fastest</li> </ul>			
DUT discovered in 3610 ms.			
<ul> <li>DUT did not send command being watched for within 10 seconds, PASS</li> </ul>			
<ul> <li>Pass 2, watching for 0x56b; tester response slowest</li> </ul>			
<ul> <li>DUT discovered in 3370 ms.</li> </ul>			
😑 01: No unexpected MSC commands or unexpected Data during the time it is waitin	g for	Pass	
	rned	Pass	
4 📑 6.3.3.4: CBM: DUT sends (0x60) SET INT/WRITE STAT Command		Pass	
> e Iter 01:		Pass	
A Solution of the sender (0x6C) WRITE BURST Command		Pass	
b Jiter 01:		Pass	
▲ 🗄 6.3.3.6: CBM: DUT sends (0x68) MSC MSG Command		Pass	
▷ V Iter 01:	×	Pass	
E: 6.3.3.7: CBM: DUT sends (0x6A) GET DDC ERRORCODE Command		Pass	
Test Log			
ine Message			
0118 Saving the test logs.			
0119 Test 6.3.8.1 Iter 01 -> Fail			
0120 Test 6.3.8.2-01			
0121 Executing the test.			
0122 Retrieving test results.			
0123 Processing test results.			
0124 Saving the test logs.			
0125 Test 6.3.8.2 Iter 01 -> Fail			
0126 Tests completed			
🔀 Close Window 🕨 Continue Testing			

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The log will indicate when the tests have completed.

Test List			
All XAII 🔅 Reset Status			
Category / Test Name	×	Status	
b 😝 Iter 01:	V		
▲ 📙 6.3.3.7: CBM: DUT sends (0x6A) GET DDC ERRORCODE Command		Pass	
▷	×	Pass	
6.3.5: MSC - DUT Output: Never Initiates Bad Commands			
> 🗏 6.3.5.1: CBM: DUT Never Sends Reserved Commands		Pass	
🛛 📙 6.3.5.2: CBM: DUT Never Sends Illegal Commands		Pass	
🛛 📃 6.3.5.3: CBM: DUT Never Sends Data While No Command is Outstanding		Pass	
[] 6.3.5.4: CBM: DUT Never Sends (0x33) ACK packet While No Command is Outstanding	ng	Pass	
E 6.3.5.5: CBM: DUT Never Sends (0x34) NACK Packet While No Command is Outstandi	ing	Pass	
E 6.3.5.6: CBM: DUT Never Sends (0x35) ABORT While No Command is Outstanding		Fail	
E 6.3.5.7: CBM: DUT Never Sends (0x32) EOF While No Command is Outstanding		Pass	
6.3.8: MSC - DUT Input: Device Register Space Contents; Writes			
5.3.8.1: CBM: Interrupt Regs; SET INT (0x60); Valid Registers Respond		Fail	
▶ 😝 Iter 01:	×	Fail	
6.3.8.2: CBM: Status Regs; WRITE STAT (0x60); Valid Registers Respond		Fail	
b	×	Fail	
6.3.13: MSC - DUT Output: Never Initiates Bad Commands			
E 6.3.13.1: CBM-Source: Source DUT Never Sends (0x64) SET HPD Command		Pass	
E 6.3.13.2: CBM-Source: Source DUT Never Sends (0x65) CLR HPD Command		Pass	
6.3.17: DDC - DUT Output; DUT Never Sends Illegal DDC Command			
6.3.17.2: CBM-Source: DUT Never Sends Illegal DDC Command		Fail	
↓ Jter 01: Continuous Background Test	×	Fail	
E 6.3.17.3: CBM-Source: DUT Never Sends Illegal DDC Command Sequence		Pass	
Test Log			
ne Message			_
Saving the test logs.			
Test 6.3.8.1 Iter 01 -> Fail			
D120 Test 6.3.8.2-01			
2121 Executing the test.			
122 Betrieving test results			
2123 Processing test results.			
Saving the test logs			
Test 6.3.8.2 Iter 01 -> Fail			
Test completed			

When the tests are completed the test window that shows the current activity will close. A new tab and panel will appear called the **CT Results** tab. You can view the test results in this panel. Refer to the following screen shot for an example of the **CT Results** panel.

🔠 Event Plot 🔤 Edid Editor 🔯 EDID CT 1.4a 🔯 CBUS Sink CT 1.2 🔯 CBUS Src CT 1.2 🔯 CBUS Dongle CT 1.2 🗐 CT R	lesults 🛛	- 8
CBUS Src Compliance Test Results		
Results Name: Acme_MHL_Tests ManufacManufacturer:		HTML Report
Date Tested: October 2, 2012 2:05 PM Model Name:		
Overall Status: CTS 1.2 - Incomplete Port Tes/Port Tested:		
Test Results		
Test Name / Details	Ö	Status
3.2.6.1: EDID Reading Test		Fail
3.2.6.2: Device Capability Registers Test		Pass
3.3.3.1: Common Test Environment		Pass
🗏 3.3.3.2: CBE-Source: VBUS Absolute Maximum Positive Voltage		Pass
🗏 3.3.3.3: CBE-Source: CBUS Absolute Maximum Positive Voltage		Pass
🗏 3.3.4.1: CBT-Source: Time from Source VBUS Application to Disc		Fail
3.3.5.1: CBE-Source: Response to Initial Plug-in to MHL Device		Incomplete
3.3.5.2: CBE-Source: Response to Sink Priming Pulse to MHL dev		Fail
🗏 3.3.5.3: CBE-Source: Pre-Discovery Success Pull-up HIGH Voltag		Incomplete
3.3.5.4: CBE-Source: Discovery Pulse Drive HIGH Voltage		Pass
3.3.5.5: CBE-Source: Discovery Pulse float LOW Voltage		Pass
3.3.9.2: CBT-Source: Continuous Monitor: Bit Timing Variation		Pass
3.3.12.3: CBT Source: Source Never Sends Too Many Back-to-Back		Pass
3.3.13.1: CBT-Source: Source Never Sends Impulse Noise		Pass
3.3.13.2: CBT-Source: Source Never Sends Partial Packets		Pass
3.3.14.1: CBT-Source: Discovery; Sink Responds Correctly; Time		Fail
3.3.14.2: CBT-Source: Discovery; Sink Responds Late		Incomplete
3.3.14.3: CBT-Source: Discovery; Sink Never Drives MHL+/- HIGH		Pass
3.3.22.1: CBT-Source: Remove MHL+/- Pull-ups for Less than Gli		Pass
3.3.22.2: CBT-Source: Remove MHL+/- Pull-up for More than Glit		Pass
3.3.22.3: CBT-Source: Time from Disconnect until VOUT Falls		Fail
6.3.2.1: CBM: DUT Sends Vendor-Specific and Reserved Header Va		Pass
6.3.3.1: CBM: DUT sends (0x62) GET STATE command		Pass
6.3.3.2: CBM: DUT sends (0x63) GET VENDOR ID Command		Pass
6.3.3.3: CBM: DUT sends (0x6B) GET MSC ERRORCODE Command		Pass
6.3.3.4: CBM: DUT sends (0x60) SET INT/WRITE STAT Command		Pass
6.3.3.5: CBM: DUT sends (0x6C) WRITE BURST Command		Pass
6.3.3.6: CBM: DUT sends (0x68) MSC MSG Command		Pass
E 6.3.3.7: CBM: DUT sends (0x6A) GET DDC ERRORCODE Command		Pass 🔻
Instrument: My980 [192.168.254.135]	•	Continue Test Execution

# **3.6** Viewing Details of Source Compliance Test Passes or Failures

When you have completed the test series you will have an opportunity to view the detailed data for a particular failure. Use the following procedures to view the details of a test.

### To view the details of each test:

1. Expose the detailed results of a failure and highlight a failure. Refer to the screen example below.

🔠 Event Plot 🚾 Edid Editor 🔯 EDID CT 1.4a 🔯 CBUS Sink CT 1.2 🔯 CBUS Src CT 1.2 🔯 CBUS Dongle CT 1.	2 📃 CT Results 🛛	
CBUS Src Compliance Test Results		
Results Name:     Acme_MHL_Tests     Manufacturer:     Acme       Date Tested:     October 2, 2012 2:05 PM     Model Name:     XYZ       Overall Status:     CTS 1.2 - Incomplete     Port Tested:     1		IL Report
Test Results		
Test Name / Details	😥 Status	*
B 3.3.3.2: CBE-Source: VBUS Absolute Maximum Positive Volta	age Pass	
B 3.3.3.3: CBE-Source: CBUS Absolute Maximum Positive Volta	age Pass	
> 🗏 3.3.4.1: CBT-Source: Time from Source VBUS Application to	Disc Fail	
> 🗏 3.3.5.1: CBE-Source: Response to Initial Plug-in to MHL D	Device Incomplet	e 🛛
> 🗏 3.3.5.2: CBE-Source: Response to Sink Priming Pulse to MH	HL dev Fail	
> 🗏 3.3.5.3: CBE-Source: Pre-Discovery Success Pull-up HIGH V	Joltag Incomplet	<mark>e</mark>
> 🗄 3.3.5.4: CBE-Source: Discovery Pulse Drive HIGH Voltage	Pass	
> 3.3.5.5: CBE-Source: Discovery Pulse float LOW Voltage	Pass	
3.3.9.2: CBT-Source: Continuous Monitor: Bit Timing Varia	ation Pass	
▷ 3.3.12.3: CBT Source: Source Never Sends Too Many Back-to	D-Back Pass	=
▶ 3.3.13.1: CBT-Source: Source Never Sends Impulse Noise	Pass	
▶ 3.3.13.2: CBT-Source: Source Never Sends Partial Packets	Pass	
3.3.14.1: CBT-Source: Discovery; Sink Responds Correctly;	; Time Fail	
⊿ ⊌ Iter 01:	Fail	
DUT discovered in 3370 ms.		
DUT in discovery mode: measured 1654/1659/1657.42 mv (min/max/avg)		
DUT in on mode: measured 1513/1517/1515.91 mv (min/max/avg)		
• voltage change: -8.54 *		_
unexpected voltage change. Expected about 5 percent increase.		
01: Source does complete Discovery	Pass	
U2: DUT does switch its pull-up from ZCBUS SRC DISCOV	/ER to Pass	
3.3.14.2: CBT-Source: Discovery; Sink Responds Late		,e
5.5.14.5: CBT-Source: Discovery; Sink Never Drives MHL+/-	- HIGH Pass	
► 3.3.22.1. CBI-Source: Remove MHL+/- Pull-up for More than		
N ■ 3 3 22 3: CBT-Source: Time from Disconnect until VOLT Fol		
6 3 2 1: CBM: DUT Sends Vendor-Specific and Reserved Head	ler Va	
6.3.3.1: CBM: DUT sends (0x62) GET STATE command	Pass	
6.3.3.2: CBM: DUT sends (0x63) GET VENDOR TO Command	Pass	-
3.2.6.1: EDID Reading Test		
Instrument: [My980 [192.168.254.135]	<ul> <li>Continue Test Ex</li> </ul>	ecution

980 User Guide – MHL CBUS Compliance Tests

CBUS Src Compliance Test Results		
Results Name: Acme_MHL_Tests     Manufacturer: Acme       Date Tested: October 2, 2012 2:05 PM     Model Name: XYZ       Overall Status:     CTS 1.2 - Incomplete     Port Tested: 1		HTML R
Test Results		
Test Name / Details	0	Status
3.3.3.2: CBE-Source: VBUS Absolute Maximum Positive Voltage		Pass
5 3.3.3.3: CBE-Source: CBUS Absolute Maximum Positive Voltage		Pass
5 3.3.4.1: CBT-Source: Time from Source VBUS Application to Disc		Fail
3.3.5.1: CBE-Source: Response to Initial Plug-in to MHL Device		Incomplete
5 3.3.5.2: CBE-Source: Response to Sink Priming Pulse to MHL dev		Fail
Description State	1	Incomplete
▲ 🗏 3.3.5.4: CBE-Source: Discovery Pulse Drive HIGH Voltage		Pass
⊿ 🝚 Iter 01:		Pass
Running pass 1, VBUS not driven by tester		
Discovery pulse high measurement: 1606 mv		
Discovery pulse high measurement: 1608 mv		
Discovery pulse high measurement: 1609 mv		
Running pass 2, VBUS driven by tester		
Discovery pulse high measurement: 1627 mv		
Discovery pulse high measurement: 1628 mv		
\varTheta 01: HIGH voltage is greater than VIH CBUS{min}		Pass
B 3.3.5.5: CBE-Source: Discovery Pulse float LOW Voltage		Pass
<pre>&gt; 3.3.9.2: CBT-Source: Continuous Monitor: Bit Timing Variation</pre>		Pass
B 3.3.12.3: CBT Source: Source Never Sends Too Many Back-to-Back		Pass
3.3.13.1: CBT-Source: Source Never Sends Impulse Noise		Pass
D 3.3.13.2: CBT-Source: Source Never Sends Partial Packets		Pass
3.3.14.1: CBT-Source: Discovery; Sink Responds Correctly; Time		Fail
3.3.14.2: CBT-Source: Discovery; Sink Responds Late		Incomplete
▶ 3.3.14.3: CBT-Source: Discovery; Sink Never Drives MHL+/- HIGH		Pass
▶ 3.3.22.1: CBT-Source: Remove MHL+/- Pull-ups for Less than Gli		Pass
3.3.22.2: CBT-Source: Remove MHL+/- Pull-up for More than Glit	:	Pass
3.3.22.3: CBT-Source: Time from Disconnect until VOUT Falls		Fail
6.3.2.1: CBM: DUT Sends Vendor-Specific and Reserved Header Va	L	Pass
E 6.3.3.1: CBM: DUT sends (0x62) GET STATE command		Pass

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## 3.7 Accessing the test results through the navigator panel

You can view the results of the tests at any time after you run them through the 980 GUI Manager's **Navigator** panel. Use the following procedures to view the details of a test.

### To access the test results:

1. Access the **Navigator** tab and select **Compliance**. Refer to the screen example below.



2. Double click on the Results file you wish to view. The results will appear in a CT Results window on the right. Refer to the screen example below.

Compliance       Compliance       Test Results         Compliance       ACA       Image: Compliance       Test Results         Compliance       Test Results       Image: Compliance       Test Results         Compliance       Test Results       Image: Compliance       Test Results         Name       Date / Time       Overall Status:       CIS 1.2 - Fail       Port Tested: 1	ort
Results Name:         0.02 <th0.02< th="">         0.02         0.02</th0.02<>	ort
> 🗁 HDMI EDID CT CT Test Results	
b be HDMISrc CT Test Name / Details Status	
BHDMISink CT     B 3.2.6.1: EDID Reading Test     Fail	
MHLSrC1	
B WHILE SINCE OUNGECT     Source : Time from Source VBUS Application to Discovery     Fail	
► COF	
Test Selections	
🛛 MHL_CBUS_DS.xml 2012/04/3017: 📃 3.3.9.1: CBT-Source: Arb, Sync, Data HIGH and LOW Times Pass	
🕞 Results 📃 🗄 3.3.14.1: CBT-Source: Discovery; Sink Responds Correctly; Time to S	
MHL_CBUS_3_04_30_20 2012/04/30 17:	
>         MHL_CBUS_2.04.30.20 2012/04/30 17:         Image: 6.3.3.1: CBM: DUT sends (0x62) GET STATE command         Fail	
Image: MHL_CBUS_04_30_2012 2012/04/30 17:         Image: Gamma and the second s	
▶ = 05_02_2012_14_18_59 2012/05/0214	
📑 6.3.8.1: CBM: Interrupt Regs; SET INT (0x60); Valid Registers Response of Fail	
📕 6.3.8.2: CBM: Status Regs; WRITE STAT (0x60); Valid Registers Respo	
6.3.11.3: CBM: DUT Receives Data While No Command Outstanding	
6.3.11.5: CBM: DUT Receives (0x34) a NACK Packet While No Command C	
■ 6.3.12.1: CBM: DUT Receives (0x61) READ DEVCAP - Offset Timeout	
■ 6.3.12.3: CBM: DUT Receives (0x60) SET INT - Data Timeout	
6.3.12.5: CBM: DUT Receives (0x6C) WRITE BURST - Offset Timeout	
6.3.18.1: CBM-Source: DUT Issues DDC Short Read and Current Read	
5.3.18.2: CBM-Source: DUT Issues Regular DDC Read	
6.3.18.3: CBM-Source: DUT Issues DDC Segment Read Fail	
Di Hars Action Dutton 6 219 20 CPM Sources DIT Jourse Results DDC Band	
Instrument: Dan_980_CBUS [192.168.254.155]	۶n

3. Double click on the Log file you wish to view. The results will appear in a new window. Refer to the screen example below.

, 	
	🖾 Log
	From: Acme_MHL_Tests
Line	Message
• 14:05:50:260	Compliance Test Started.
• 14:05:50:363	
• 14:05:50:397	Assembling the test list.
• 14:05:51:295	Transferring the CDF to the Test Instrument.
14:05:51:295	FTP Connect
• 14:05:51:557	
	From "C:\Users\nkendall\Desktop\980_CBUS_GUI\980mgr\cbussrcct\results\Acme_MHL_Tests\cdf.txt"
	To "adf.txt"
• 14:05:51:919	Test 3.2.6.1-01
• 14:06:51:640	Configuration Change: UNKNOWN -> SRC_ACTIVE
• 14:06:51:692	
• 14:06:51:693	exec rm -f /home/qd/cbus_results.log
• 14:06:51:710	exec rm -f /home/qd/cbus_results.log
• 14:06:51:900	<pre>#cbus-scope&gt;</pre>
• 14:06:51:901	IN10:cbus_test 3.2.6.1 -o "/home/qd/" -c "/home/qd/cdf.txt"
• 14:06:51:910	IN10:cbus_test 3.2.6.1 -o */home/qd/c -c */home/qd/cdf.txt*
• 14:07:35:805	<pre>#cbus-scope&gt;</pre>
• 14:07:36:031	Retrieving test results.
• 14:07:36:031	FTP Connect
14:07:36:289	FTP Get
	From "cbus_results.log"
	To "C:\Users\nkendall\Desktop\980_CBUS_GUI\980mgr\cbussrcct\results\Acme_MHL_Tests\lastResult.log"
• 14:07:36:533	Processing test results.
• 14:07:36:565	Saving the test logs.
• 14:07:36:568	exec test -e */home/qd/cbus_log.log* 66 echo exists
• 14:07:36:580	exec test -e */home/qd/cbus_log.log* 66 echo exists
14:07:36:770	exists
	\$cbus-scope>
• 14:07:36:771	FTP Connect
• 14:07:37:028	FTP Get
	From "cbus log.log"
•	To "C:\Users\nkendall\Desktop\980 CEUS GUI\980mar\cbussrcct\results\Acme MHL Tests\3 2 6 1 01\cbus log.log"
	"
	X Close

4. Double click on the Summary file. The Summary file will appear in a new window. Refer to the screen example below.

File Viewer	×
File: C:\Users\nkendall\Desktop\980 CBUS GUI\980mar\cbussrcct\results\Acme MHL Tests\summarv.txt	
[Created]	Â.
Created On: October 2, 2012 2:05:49 PM CDT	
[Status]	
Ok: All tests executed.	
[Test Summary]	
Test: 3.2.6.1 - Fail	
Test: 3.2.6.2 - Pass	=
Test: 3.3.3.1 - Pass	
Test: 3.3.3.2 - Pass	
Test: 3.3.3.3 - Pass	
Test: 3.3.5.1 - Incomplete	
Test: 3.3.5.2 - Fail	
Test: 3.3.5.3 - Incomplete	
Test: 3.3.5.4 - Pass	
Test: 3.3.5.5 - Pass	
Test: 3.3.9.2 - Pass	
Test: 3.3.12.3 - Pass	
Test: 3.3.13.1 - Pass	
Test: $3.3.13.2 - Fass$	
Test: 3.3.14.2 - Incomplete	
Test: 3.3.14.3 - Pass	
Test: 3.3.22.1 - Pass	
Test: 3.3.22.2 - Pass	
Test: 3.3.22.3 - Fail	
Test: 6.3.2.1 - Pass	
Test: 6.3.3.1 - Pass	
Test: 6.3.3.2 - Pass	
Test: 6.3.3.4 - Pass	
Test: 6.3.3.5 - Pass	
Test: 6.3.3.6 - Pass	
Test: 6.3.3.7 - Pass	
Test: 6.3.5.1 - Pass	
Test: 6.3.5.2 - Pass	
Test: 6.3.5.3 - Pass	
Test: 6.3.5.4 - Pass	
4 III	•
	_
OK	

# 3.8 Viewing the MHL Source Compliance HTML test report

After you have completed the tests, an HTML Report activation button will appear in the upper right of the screen which enables you to access the html report of the test results. Use the following procedures to view the html test report.

### To view the html test report:

- 1. Select the **CT Results** panel as shown below.
- 2. Click on the HTML Report activation button.

A dialog box will appear asking if you want a summary of the test results or a version that includes the CDF. This dialog box is shown in the screen shot below.

🗄 Event Plot 🔤 Edid Editor 🔯 EDID CT 1.4a 🔯 CBUS Sink CT 1.2 🔯 CBUS Src CT 1.2 🔯 CBUS Dongle CT 1.2 📳 CT Results 🛛 📃 🗆			
CBUS Src Complia	nce Test Results		
Results Name: Acme_MHL_Tests Manufacturer: Acme Manufacturer: Acme			
Date Tested: October 2, 2012 2:05 PM Model Name: XYZ			
Overall Status: CTS 1.2 - Incomplete	Port Tested: 1		
Test R	esults		
Test Name / Details		Ø	Status 🔺
3.2.6.1: EDID Reading Test			Fail
3.2.6.2: Device Capability Registers Test			Pass
🗏 3.3.3.1: Common Test Environment			Pass
3.3.3 Or ODD Grouper Mould abor late Meridian	Tositive Voltage		Pass
3.3. Generate Report	ositive Voltage		Pass
3.3.4	pplication to Disc		Fail
B 3.3.1 HTML Report	J-in to MHL Device		Incomplete
3.3.1 Acme_MHL_Tests	J Pulse to MHL dev		Fail
3.3 Select the desired report options.	ill-up HIGH Voltag		Incomplete
3.3.1 Stiet in desite report options	IGH Voltage		Pass
3.3.1 Show Test Summary Only.	DW Voltage		Pass
3.3.1	Timing Variation		Pass
■ 3.3.:	Many Back-to-Back		Pass
3.3.1	ilse Noise		Pass
3.3.1 X Cancel	tial Packets		Pass
3.3.1 Calcer	is Correctly; Time		Fail
3.3.1	ds Late		Incomplete
3.3.14.3: CBT-Source: Discovery; Sink Neve	r Drives MHL+/- HIGH		Pass
3.3.22.1: CBT-Source: Remove MHL+/- Pull-u	ps for Less than Gli		Pass
3.3.22.2: CBT-Source: Remove MHL+/- Pull-u	p for More than Glit		Pass
3.3.22.3: CBT-Source: Time from Disconnect	until VOUT Falls		Fail
6.3.2.1: CBM: DUT Sends Vendor-Specific an	d Reserved Header Va		Pass
6.3.3.1: CBM: DUT sends (0x62) GET STATE c	ommand		Pass
6.3.3.2: CBM: DUT sends (0x63) GET VENDOR	ID Command		Pass
6.3.3.3: CBM: DUT sends (0x6B) GET MSC ERR	ORCODE Command		Pass
6.3.3.4: CBM: DUT sends (0x60) SET INT/WRI	TE STAT Command		Pass
6.3.3.5: CBM: DUT sends (0x6C) WRITE BURST	Command		Pass
5.3.3.6: CBM: DUT sends (0x68) MSC MSG Com	mand		Pass
	ORCODE Command		Pass 🔻
Instrument: My980 [192.168.254.135]		-	Continue Test Execution

Specify if you want to see a summary report and if you want to see the CDF. If you leave Show Test Summary Only unchecked the application will produce a full detailed report. The following screens provide samples of the report.

Note: This example shows an MHL 1.2 test result; MHL 2.0 test results are similar in content and structure.

Viewer				
C:\Users\nkend	all\Desktop\980_CBUS_GUI\980mgr\cbussrcct\results\Acme_MHL_Test	s\Report_Summary_Cdf.htm		
port generated on: October 2, 2012 2:41 PM	<u>Quantum Data</u> BUS Src Compliance Test F CTS 1.2	www.quantumdata.com		
Results Name: Date Tested: Overall Status:	Acme_MHL_Tests October 2, 2012 2:05 PM Incomplete	Manufacturer: Acme Model Name: XYZ Port Tested: -		
	Capabilities Declaration Form (CDF	)		
CDF MFR NAME	General	Acme		
CDF_MODEL_NUMBER XYZ				
CDF_SRC_POWERED YES				
CDF_SRC_CBUS_THRESHOLD_V 0.90				
CDF_PROC_SET_ACTIVE Not Specified				
CDF_PROC_SET_STANDBY Not Specified				
CDF_RCP_RECEIVE		YES		
CDF_RCP_SEND		NO		
CDF_LOG_DEV_MAP_CHANGE	NO			
	Capability Registers			
CDF_CR_MHL_VER_MAJOR	1			
CDF_CR_MHL_VER_MINOR 0				
CDF_CR_DEV_TYPE 2				
CDF_CR_POW 0				
CDF_CR_ADOPTER_ID_H 0				
CONCEPADOPTED ID I		💠 Back 🌩 Forward 📙 Save As  K Clos		

The CDF is shown below:

HTML Viewer				
	C:\Users\nkendall\Desktop\980_CBUS_GUI\980mgr\cbussrcct\results\Acme_MHL_Tests\Report_Sum	mary_Cdf.htm		
	Capability Registers		<u>^</u>	
	CDF_CR_MHL_VER_MAJOR	1		
	CDF_CR_MHL_VER_MINOR	0		
[	CDF_CR_DEV_TYPE	2		
[	CDF_CR_POW	0		
	CDF_CR_ADOPTER_ID_H	0		
[	CDF_CR_ADOPTER_ID_L	0	E	
	CDF_CR_SUPP_RGB444	1		
	CDF_CR_SUPP_YCBCR444	1		
	CDF_CR_SUPP_YCBCR422	0		
	CDF_CR_SUPP_PPIXEL	0		
	CDF_CR_SUPP_ISLANDS	0		
	CDF_CR_SUPP_VGA	0		
[	CDF_CR_AUD_2CH	1		
	CDF_CR_AUD_8CH	0		
	CDF_CR_VT_GRAPHICS	0		
	CDF_CR_VT_PHOTO	0		
	CDF_CR_VT_CINEMA	0		
	CDF_CR_VT_GAME	0		
[	CDF_CR_SUPP_VT	0		
	CDF_CR_LD_DISPLAY	0		
	CDF_CR_LD_VIDEO	1		
	CDF_CR_LD_AUDIO	1		
	CDF_CR_LD_MEDIA	1		
	CDF_CR_LD_TUNER	0		
	CDF_CR_LD_RECORD	0		
	CDF_CR_LD_SPEAKER	0		
	CDF_CR_LD_GUI	1		
	CDF_CR_BANDWIDTH	15	-	
	4	Back 🜩 Forward 🛛 🗟 Save As 🛛 💥 🤇	Close	

The detailed results for a failure are shown below:

L Viewer		
C:\Users\nkendall\Desktop\980_CBUS_GUI\980mgr\cbussrcct\results\Acme_MHL_T	ests\Report_Summary_Cdf.htm	
Test 3.2.6.1 EDID Reading Test	Fail	
Test 3.2.6.2 Device Capability Registers Test	Pass	
Test 3.3.3.1 Common Test Environment	Pass	
Test 3.3.3.2 CBE-Source: VBUS Absolute Maximum Positive Voltage	Pass	
Test 3.3.3 CBE-Source: CBUS Absolute Maximum Positive Voltage	Pass	
Test 3.3.4.1 CBT-Source: Time from Source VBUS Application to Discovery Pulses	Fail	
Test 3.3.5.1 CBE-Source: Response to Initial Plug-in to MHL Device	Incomplete	
Test 3.3.5.2 CBE-Source: Response to Sink Priming Pulse to MHL device	Fail	
Test 3.3.5.3 CBE-Source: Pre-Discovery Success Pull-up HIGH Voltage	Incomplete	
Test 3.3.5.4 CBE-Source: Discovery Pulse Drive HIGH Voltage	Pass	
Test 3.3.5.5 CBE-Source: Discovery Pulse float LOW Voltage	Pass	
Test 3.3.9.2 CBT-Source: Continuous Monitor: Bit Timing Variation within a Packet	Pass	
Test 3.3.12.3 CBT Source: Source Never Sends Too Many Back-to-Back Packets	Pass	
Test 3.3.13.1 CBT-Source: Source Never Sends Impulse Noise	Pass	
Test 3.3.13.2 CBT-Source: Source Never Sends Partial Packets	Pass	
Test 3.3.14.1 CBT-Source: Discovery; Sink Responds Correctly; Time to Source Pull-up Change	Fail	
Test 3.3.14.2 CBT-Source: Discovery; Sink Responds Late	Incomplete	
Test 3.3.14.3	Berr	

ITML Viewer	
C:\Users\nkendall\Desktop\980_CBUS_GUI\980mgr\cbussrcct\results\05_02_2012_14_18_59\Report_Cdf.htm	
Test 3.2.6.2 Device Capability Registers Test	Fail
• Iter 01:	Fail
<ul> <li>DUT discovered in 2492 ms.</li> <li>Continuous test results to follow</li> <li>3.3: Tester began driving VBUS at 00050362.40; VBUS expected to be stable by 00065362.40.</li> <li>3.3: CBUS and VBUS within Absolute Maximum voltages during entire test</li> </ul>	
<ul> <li>3.3.12.3: max incoming back to back packets: 0 (good)</li> <li>3.3.13.1: no narrow pulses detected</li> <li>3.3.13.2: no bad packets from DUT detected</li> </ul>	
• 01: MHL_VERSION register matches CDF_CR_MHL_VER_MAJOR and CDF_CR_MHL_VER_MINOR Fail	
<ul> <li>DUT has wrong major version; wanted 1 but got 0</li> <li>DUT minor version matches</li> </ul>	
• 02: DEV_TYPE in the DEV_CAT(0ffset:0x02) register is 0b0010:Source Fail	
<ul> <li>DUT DEV_TYPE doesn't match CDF; wanted 2 but got 0</li> </ul>	
• 03: POW in the DEV_CAT(offset:0x02) register matches the CDF_CR_POW field in CDF Pass	
DUT POW is correct	
• 04: ADOPTER_ID_H(0ffset:0x03) and ADOPTER_ID_L(offset:0x04) register matches the corresponding CDF_CR_ADOPTER_ID_H and CDF_CR_ADOPTER_ID_L fields in the CDF	
DUT ADOPTER_ID_H is correct     DUT ADOPTER_ID_L is correct	
• 05: SUPP_RGB444, SUPP_YCBCR444, SUPP_YCBCR422, SUPP_PPIXEL, SUPP_ISLANDS and SUPP_VGA bits in the VID_LINK_MODE/offset/0x03) register match the corresponding CDF_CR_SUPP_RGB444, CDF_CR_SUPP_YCBCR444, CDF_CR_SUPP_YCBCR422, CDF_CR_SUPP_PPIXEL, CDF_CR_SUPP_ISLANDS and CDF_CR_SUPP_VGA field in the CDF	-
<ul> <li>DUT SUPP_RGB444 is correct</li> <li>DUT SUPP_VCBCR444 is correct</li> <li>DUT SUPP_VCBCR422 is correct</li> </ul>	
<ul> <li>DUT SUPP_PPIXELis correct</li> <li>DUT SUPP_ISLANDS is correct</li> </ul>	
	ave As 🛛 💥 Close

The final page of the report shows the test equipment configuration as shown below.

	Instrument
	Instrument
Jame:	Dan 980 CBUS
P Ad	Juness: 192.168.254.155
let M	ask: 255.255.255.0
Jatew	ay IP: 192.168.254.1
Tersi	n:
	QD980 Advanced Test platform Version: 4.3.0
	MHL CBUS Protocol Analyzer in slot 1:
	Gateware: [Version: 0 Build Number: 1 (05:02:2012 100000) pcb: 23232323]
	Firmware: [Version: 1.0.0 beta Build Number: 242 (dsmith 05:02:2012 13:21:41 CDT)]
	System Information:
	SN : [N/A::N/A]
	Main Board : [ "DG41RQ"]
	DDD - [ 2.081 'Intel(k) Celeron(k) CPU 440 @ 2.00GHZ"]
	HD · [ WD1600EFVT_11
	OS : [ Linux xpscope-97 2.6.26-2-686 #1 SMP Wed Aug 19 06:06:52 UTC 2009 i686 GNU/Linux]
	GUI manager : [ Version 3.1.0 26501 201107071448]
	1 : [ lo inet 127.0.0.1/8 scope host lo]
	2 : [ eth0 inet 192.168.254.155/24 brd 192.168.254.255 scope global eth0]
	HDMI SRC CTS: [ 2.4.4]
	MHL SRC CTS : [ NOT Installed]
	HDMI SNK CTS: [ NOT Installed]
	TT 4
	nost
IT No.	The Overstype Date 080 Manager . Morrier 2 1 14
IT Ho	me. plantom baca sob manager - version still me. plantom (hase/plugins/com guantumdata 1980 app
Tava	Vendor: Null
ava	Runtime: 1.6.0 15-603
Tava	Home: C:\Users\nkendall\Desktop\MHL CBUS Release 4 26\980mgr\jre
S: w	in32
S Ar	ch: x86
local	e: en US

# 3.9 CBUS Log Plot

The **CBUS Log Plot** panel (shown below) is panel used for viewing the bit and byte timing events of the CBUS controls and commands that occurred during a specific test. A **CBUS Log Plot** is provided for each source CBUS compliance test. The panel has both a graphical depiction of CBUS timing events and a sequential table list out of each event. The vertical axis shows the various CBUS event types. The **CBUS Log Plot** panel provides a set of CBUS event types labeled on the left that indicate the type of event. The horizontal axis is time.

The CBUS Log Plot is useful diagnosing CBUS compliance test failures.

The example below shows a series of events captured during a source test.

For more detailed information about the CBUS Log Plot, please refer to CBUS Log Plot.

🖶 Event Plo	ot 🖶 CBUS Plot 🛛 🚺	CT Results				- 8
Data: MHL_CBUS_2.0_121105\3_3_10_1_01						
Rows	Segment					
	Zoom %:	0.252	🔾 🔍 📃 Marker 1		Marker 2 🗲 💿 Đ	
0:0:1.501.489	).486					
[						
PASS			Pa	ss 1		
PACKET						
CBUS L/V						
PULSE						
CBUS DRV					DUT	DUT
VBUS DRV			Te	ster		
VBUSTVI						
CRUIC TRM	1000		<u> </u>	100		
CBUS TRM	1000 onims p	uliuown		100 K-0	ims pulidown	
TMDS TRM	high	Z		70 o	hm pullup	
RXS+						
RXS-						
0:0:1.500	.598.325 0:0	0:1.501.365.345	0:0:1.50 Time (H:M:	2.136.797 S.ms.us.ns)	0:0:1.502.908.250	0:0:1.503.679.703
TimeStamp		Туре	Description			
0:0:1.50	01.750.210	CBUS LVL	HIGH (0:0:0.000.499.540)			
0:0:1.50	01.750.290	CBUS TRM	100 k-ohms pulldown			68
0:0:1.50	01.750.340	TMDS TRM	70 ohm pullup			
0:0:1.50	02.249.450	CBUS DRV	Tester is driving CBUS			
0:0:1.502.249.750 CBUS LVL		LOW (0:0:0.000.001.050)				
0:0:1.502.249.750 PULSE		Sink arbitrates (case 3)				
0:0:1.502.249.750 PACKET		Sink -> Source <msc clr_hpd=""></msc>				
0:0:1.502.250.800 CBUS LVL		HIGH (0:0:0.000.003.980)				
0:0:1.502.250.850 CBUS DRV		DUT is driving	J CBUS			
0:0:1.50	02.254.480	CBUS DRV	Tester is driv	ring CBUS		0
Events	🔯 Find					

# 4 MHL CBUS Sink Compliance Tests

This chapter describes how to run the MHL CBUS sink compliance tests. Please note you will have to purchase the optional 980 MHL CBUS Compliance Test module in order to run these tests.

The 980 MHL CBUS Compliance test module supports the test sections listed below in the MHL 1.2 and MHL 2.0 Compliance Test specifications. *Please note that some non-CBUS compliance tests are also covered by the 980 MHL CBUS Compliance Test module*.

## 4.1 System Test – Section 4.2

- 4.2.5 EDID and Device Capability Register Tests
  - o 4.2.5.1 EDID Reading Test
  - 4.2.5.2 Device Capability Registers Test
- 4.2.6 RCP Sub-Command Tests
- 4.2.8 3D Tests
  - 4.2.8.1 3D Video Most Support (MHL CTS 2.0 only)
- 4.2.9 UCP Sub-Command Tests (MHL CTS 2.0 only)

## 4.2 CBUS Tests – Section 4.3

- 4.3.1 CBUS Sink DUT Common Test Equipment Setups
- 4.3.2 CBUS Sink DUT Common Required Methodologies
- 4.3.3 Link Layer Electrical Sink: Absolute Maximum Voltages
- 4.3.4 Link Layer Electrical Sink DUT Output: Standby Discovery Impedance
- 4.3.5 Link Layer Timing Sink DUT Output: Pre-Discovery
- 4.3.6 Link Layer Electrical Sink DUT Output: Arbitration/Sync/Data Signaling
- 4.3.7 Link Layer Timing Sink DUT Output: Arbitration/Sync/Data in Nanoseconds
- 4.3.8 Link Layer Timing Sink DUT Output: Arbitration/Sync/Data in Bit Times
- 4.3.9 Link Layer Timing Sink DUT Output: Link Level NACK
- 4.3.10 Link Layer Timing Sink DUT Output: Link Level ACK
- 4.3.11 Link Layer Timing Sink DUT Output: Bus Re-Arbitration
- 4.3.12 Link Layer Timing Sink DUT Output: Ill-formed packets
- 4.3.13 Link Layer Electrical Sink DUT Input: Discovery
- 4.3.14 Link Layer Timing Sink DUT Input: Discovery OK
- 4.3.15 Link Layer Timing Sink DUT Input: Discovery Reject
- 4.3.16 Link Layer Electrical Sink DUT Input: Arbitration/Sync/Data Signaling
- 4.3.17 Link Layer Timing Sink DUT Input: Arbitration
- 4.3.18 Link Layer Timing Sink DUT Input: Data
- 4.3.19 Link Layer Timing Sink DUT Input: NACK
- 4.3.20 Link Layer Timing Sink DUT Input: ACK

- 4.3.21 Link Layer Timing Sink DUT Input: Bus Re-Arbitration
- 4.3.22 Link Layer Timing Sink DUT Input: Ill-formed Packets
- 4.3.23 Link Layer Timing Sink DUT Input: Disconnect
- 4.3.24 Link Layer Electrical Sink DUT VBUS Output
- 4.3.25 Link Layer Timing Sink DUT VBUS Turn On Transition

# 4.3 CBUS Common Tests – Section 6.3

- 6.3.1 MSC Source and Sink DUT Input: Device Register Space Contents; Reads
- 6.3.2 MSC Source and Sink DUT Output: NACK Packet Response to MSC\_MSG
- 6.3.3 MSC Source and Sink DUT Output: Never Initiates Bad Commands
- 6.3.5 MSC Source and Sink DUT Output: Errors and Exceptions
- 6.3.6 MSC Source and Sink DUT Input: Device Register Space Contents; Writes
- 6.3.7 MSC Source and Sink DUT Input: Vendor Specific and Reserved Header Values
- 6.3.8 MSC Source and Sink DUT Input: Device Register Space Contents; Writes
- 6.3.9 MSC Source and Sink DUT Input: Vendor-specific and Reserved Header Values
- 6.3.10 MSC Source and Sink DUT Input: Normal Commands
- 6.3.11 MSC Source and Sink DUT Input: Errors and Exceptions
- 6.3.12 MSC Source and Sink DUT Input: Argument Timeouts
- 6.3.15 MSC Sink DUT Output: Normal Commands
- 6.3.16 MSC Sink DUT Input: Errors and Exceptions
- 6.3.20 DDC Sink DUT Input; Continuous Monitors and Normal Operation
- 6.3.21 DDC Sink DUT Input; Normal Operation
- 6.3.22 DDC Sink DUT Input; Illegal Responses

# 4.4 Workflow for running the MHL CBUS Sink Compliance Tests

The list below is the high level workflow for running the MHL CBUS Sink Compliance Tests. Note that the installation of the external 980 GUI Manager and the Ethernet session are optional; you can run the compliance tests through the embedded GUI Manager.

1. Power up the 980. Refer to the procedures in Getting Started.

**Note**: The power switch in the front is used when you are turning off the 980 for a short period of time. For extended periods of off time, it is best to power the 980 down by first using the power button on the front and then the rocker switch on the back.

- 2. (Optional; only necessary if using the external 980 GUI Manager) Establish an Ethernet/IP connection between the external 980 GUI Manager and the 980.
- 3. Connect the MHL sink device under test to the CBUS Out port on the 980 MHL CBUS Compliance module using an HDMI cable.
- 4. Complete a (or load an existing) Capabilities Declaration Form (CDF) for the device under test using the **CDF Entry** panel.
- 5. Select the tests that you wish to run from the **Test Selection** panel.

- 6. Initiate the tests through the Test Options / Review panel.
- 7. View the detailed data for test failures if failures occur.
- 8. View the results in the **Test Results** panel under the **Navigator** panel.

# 4.5 Making the physical MHL connections

This subsection describes the physical MHL connections required to run the MHL CBUS sink compliance tests.



Connections for MHL CBUS sink compliance test - 980

### To make the physical MHL connections:

This procedure assumes that you have assembled the 980 with the MHL CBUS Compliance Test module and the MHL source device under test and applied power to all these devices. Refer to the procedures below and the diagram above.

1. Connect your MHL sink device under test to the lower OUT connector (HDMI) on the 980 MHL CBUS Compliance Test module as shown in the figure above.

**Important Note**: Quantum Data provides a short 30cm HDMI cable for running the MHL CBUS sink compliance tests. Although we recommend that you use this cable for all MHL CBUS sink compliance tests, the cable is optional except for the following tests where the supplied 30cm cable is mandatory:

- 4.3.6.2
- 4.3.7.2
- 4.3.15.1
- 4.3.15.2
- 4.3.24.1

# 4.6 Completing the CDF

Use the following procedures to complete the CDF for the MHL CBUS sink compliance tests.

**Note**: The example workflows and screens use MHL 2.0 except where noted. Workflow and screens are similar for testing MHL 1.2 devices.

### To complete the CDF:

1. From the View menu, enable viewing of the MHL CBUS Sink CT panel.



2. Select the **CDF Entry** panel as shown below.

🖶 Event Plot 🔯 MHL :	Sink CT 2.0 🕱 📃 🗖 🗖
CDF Entry	election 🕨 Test Options / Preview
🔄 Open 😼 New	DF File: < not saved>
🔒 General 💿 Video	o 🔍 Audio 🔍 3D Video (2.0) 🔍 Other
One or more essentia	l fields are blank.
CDE CTS VERSION	CTS Version to test against.
	○ 1.2
CDF_MFR_NAME	What is the product manufacturer's name?
CDF_MODEL_NUMBER	What is the model name/number of the product?
CDF_HDCP_SUPPORT	Is HDCP supported on this DUT?  Ves  No
CDF_AVI_SUPPORT	Is AVI InfoFrame supported on this DUT?  Ves  No
CDF_AUDIO_SUPPORT	Is audio supported on this DUT? Yes   No
CDF_RAP_SUPPORT	Does the DUT support RAP Sub-Commands? (2.0 Only)
	◎ Yes ◎ No

3. To create a new CDF, click on the **New** activation button.

You will be prompted with a confirmation that you want to start a new CDF and reset the values. Click **OK** to proceed.



4. To open an existing CDF, click on the **Open** activation button.

You will be prompted with a dialog box that enables you to open a CDF. Select a CDF and then **OK** to proceed.

Note: You can save these CDFs to your PC for use on other PCs and by other colleagues.

0	CDF Editor	
	🔯 Open CDF File	
	Select a CDF to open in the CDF editor.	
	CMAcme_XYZ_MHL_CBUS_Sink_CDF	
	WHL_Display_cdf	
	Wy980_CDF	
	WyCDF_1	
	WyCDF_Sink	
	Cancel	

After you open an existing CDF or save it the name will appear beside the **Save** activation button as shown below:

🔠 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Sink CT 2.0 🛛	- 8
😂 CDF Entry 🧹 Test Selection 🕨 Test Options / Preview	
CDF File: Acme_XYZ_MHL_CBUS_Sink_CDF	

5. Complete the items in the **General** tab of the CDF Entry panel shown below. Note that you will have to complete the essential fields in order to proceed.

**Note**: A read status message will appear indicating if you have not completed all the essential fields. This is shown in the example below.

When you have entered in all the required fields the error indication will go away as shown in the example below.

🔠 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS	3 Sink CT 2.0 🛛 🦳 🗖	
🖄 CDF Entry 🧹 Test Selection 🕨 Tes	t Options / Preview	
CDF File: Acme_XYZ_MHL_CBUS_Sink_CDF		
General     Video     Audio     F	tegisters   RCP Rcv  RCP Send  RCP Send  RCP LD Map  UCP Rcv  (2.0)  UCP Send  (2.0)  3D Video  (2.0)	
CDF_CTS_VERSION	CTS Version to test against.	
CDF_MFR_NAME	What is the product manufacturer's name? Acme	
CDF_MODEL_NUMBER	What is the model name/number of the product? XYZ	
CDF_SINK_CBUS_THRESHOLD_V	Voltage at which CBUS Timing Measurements should be taken. This voltage should be halfway between the HIGH and LOW CBUS voltages for data driven by this device. This will be related to the device's VOH.         0.90       V (0.75 to 1.05)	
CDF_SINK_CABLE_DETECT_TO_R_DISCOVER	Time from Cable Detect until Sink presents valid Z_CBUS_SINK_DISCOVER.         60       sec. (0.0 to 300)	
CDF_HDCP_SUPPORT	Is HDCP supported on this DUT? Yes   No	
CDF_DDC_SEGMENT_READ_SUPPORT	Can this device support DDC Segment Read?	
CDF_SINK_WAKE_FROM_STANDBY	The DUT can recognize wake pulses from an attached Source while in standby mode, and wake up? (2.0 Only)	
CDF_PROC_SET_ACTIVE	Set Device into Active Mode for Discovery Tests. Edit Procedure	
CDF_PROC_SET_STANDBY	Set Device into Standby Mode for Discovery Tests.  Standby Mode Supported? Edit Procedure	

You can enter information using the "Edit Procedure" dialog box to help test engineers understand how to put the device in the proper mode. The information entered into this dialog box will appear during the test.

## 6. Complete the items in the **Video** tab.

🖶 Event Plot 🔯 MHL Sink	CT 2.0 🔯 CBUS Si	Sink CT 2.0 🛛					
🔯 CDF Entry 🧹 Test Se	lection 🕨 Test C	Options / Preview					
🔄 Open 🛛 🕞 New	Save CDF File: A	Acme_XYZ_MHL_CBU	S_Sink_CDF				
Consul     Video	Audia Da	nintern @ DCD Dave	B DCD Sand	e PCD I D Man	a UCD Pre (2.0)	0 UCD Same (2.0) 0 2D1	Video (20)
General Video (	• Audio   • Reg	gisters V RCP RCV	KCP Send	<ul> <li>KCP LD IViap</li> </ul>	0 UCP KCV (2.0)	• UCP Send (2.0) • 3D	video (2.0)
CDF_VIDEO_RGB	Does the DUT su	ipport RGB encoding	<u> </u> ?				
	• Yes INO		P2				
CDF_VIDEO_YCBCR_444	Over No	іррогт тевек 4:4:4 е	ncoding:				
		unport VCBCR 4-2-2 e	ncodina?				
CDF_VIDEO_YCBCR_422	Yes   No	ipport rebert 4.2.2 e	incounty.				
Does the DUT supr		upport PackedPixel e	ncodina?				
CDF_VIDEO_PACKEDPIXEL	🔘 Yes 🔘 No		·····				
		Suppo	rted Normal Mo	de Video Formats			
CDF_VIDEO_VGA	🔘 Yes 🔘 No	(1) 640x48	0p(VGA) 59.9	94/60Hz			
CDF_VIDEO_480p_60	🖲 Yes 🔘 No	(2,3) 720x48	Op 59.94/60F	łz			
CDF_VIDEO_720p_60	🖲 Yes 🔘 No	(4) 1280x7	20p 59.94/60	)Hz			
CDF_VIDEO_1080i_60	🔘 Yes 🔘 No	(5) 1920x1	080i 59.94/6	50Hz			
CDF_VIDEO_480i_60_2X	🔘 Yes 🔘 No	(6,7) 1440x4	80i 59.94/60	)Hz			
CDF_VIDEO_480i_60_4X	🔘 Yes 💿 No	(10,11) 2880x4	80i 59.94/60	OHz			
CDF_VIDEO_480p_60_2X	🔘 Yes 💿 No	(14,15) 1440x4	80p 59.94/60	OHz			
CDF_VIDEO_576p_50	🖲 Yes 🔘 No	(17,18) 720x57	6p 50Hz				
CDF_VIDEO_720p_50	🔘 Yes 💿 No	(19) 1280x7	20p 50Hz				
CDF_VIDEO_1080i_50	🖲 Yes 🔘 No	(20) 1920x1	080i 50Hz				
CDF_VIDEO_576i_50_2X	🔘 Yes 🔘 No	(21,22) 1440x5	76i 50Hz				
CDF_VIDEO_576i_50_4X	🔘 Yes 🔘 No	(25,26) 2880x5	76i 50Hz				
CDF_VIDEO_576p_50_2X	🔘 Yes 🔘 No	(29,30) 1440x5	76p 50Hz				
CDF_VIDEO_1080p_24	🔘 Yes 🔘 No	(32) 1920 <b>x</b> 1	080p 23.97/2	24Hz			
CDF_VIDEO_1080p_25	🔘 Yes 🔘 No	(33) 1920 <b>x</b> 1	080p 25Hz				
CDF_VIDEO_1080p_30	🔘 Yes 🔘 No	(34) 1920x1	080p 29.97/3	30Hz			
CDF_VIDEO_1080p_60	🔘 Yes 🔘 No	(16) 1920x1	080p 59.94/6	50Hz			
CDF_VIDEO_1080p_50	🔘 Yes 🔘 No	(31) 1920x1	080p 50Hz				

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## 7. Complete the items in the Audio tab.

🖶 Event Plot 🔯 MHL Sink CT 2	2.0 😢 CBUS Sink CT 2.0 🛛 🖓 🖓 🖓			
🔯 CDF Entry 🧹 Test Selecti	ion 🕨 Test Options / Preview			
CDF File: Acme_XYZ_MHL_CBUS_Sink_CDF				
General     Video     Audio     Registers     RCP Rcv     RCP Send     RCP LD Map     UCP Rcv (2.0)     UCP Send (2.0)     SD Video (2.0)				
	Linear PCM Audio Support			
CDF_AUDIO_2CH_3	◎ Yes ◎ No PCM 2Ch 32kHz Audio?			
CDF_AUDIO_2CH_44.1kHz	◎ Yes ◎ No PCM 2Ch 44.1kHz Audio?			
CDF_AUDIO_2CH_48kHz	◎ Yes ◎ No PCM 2Ch 48kHz Audio?			
CDF_AUDIO_2CH_88.2kHz	O Yes O No PCM 2Ch 88.2kHz Audio?			
CDF_AUDIO_2CH_96kHz	O Yes O No PCM 2Ch 96kHz Audio?			
CDF_AUDIO_2CH_176.4kHz	© Yes ⊚ No PCM 2Ch 176.4kHz Audio?			
CDF_AUDIO_2CH_192kHz	O Yes O No PCM 2Ch 192kHz Audio?			
	Max supported Channel Count.			
CDF_AUDIO_PCM_Channels	0 0 2 3 4 5 6 7 8			
	Maximum Freq for multi-channel audio (kHz)			
CDF_AUDIO_Max_Fs_Multi_Ch	© 32kHz ◎ 44.1kHz ◎ 48kHz ◎ 88.2kHz ◎ 96kHz ◎ 176.4kHz ◎ 192kHz			
Non-PCM Audio Support				
CDF_AUDIO_AC3	💿 Yes 💿 No 2: AC-3 (Dolby Digital)			
CDF_AUDIO_MPEG1	○ Yes			
CDF_AUDIO_MP3	© Yes ⊚ No 4: MP3: MPEG1 Layer 3			
CDF_AUDIO_MPEG2	© Yes ⊚ No 5: MPEG2 (multichannel)			
CDF_AUDIO_AAC	© Yes ⊚ No 6: AAC			

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## 8. Complete the items in the **Registers** tab.

🛃 Event Plot 🔯 MHL Sink CT	1 2.0 🔯 CBUS Sink CT 2.0 🛛 🖓 🖓 🖓				
🖄 CDF Entry 🧹 Test Selec	tion Fast Options / Preview				
CDF File: Acme_XYZ_MHL_CBUS_Sink_CDF					
◎ General ◎ Video ◎	Audio Registers RCP Rcv RCP Send RCP LD Map UCP Rcv (2.0) UCP Send (2.0) 3D Video (2.0)				
	Declare the expected value of each of the DUT's Capability Registers.				
CDF_CR_MHL_VER_MAJOR	Register: MHL_VERSION     Field: MHL_VER_MAJOR       1     1				
CDF_CR_MHL_VER_MINOR	Register: MHL_VERSION Field: MHL_VER_MINOR				
CDF_CR_DEV_TYPE	Register: DEV_CAT       Field: DEV_TYPE <ul> <li>(1) Sink</li> <li>(2) Source</li> <li>(3) Dongle</li> </ul>				
CDF_CR_ADOPTER_ID_H	Register: ADOPTER_ID_H     Field: ADOPTER_ID_H       0     00 - FF				
CDF_CR_ADOPTER_ID_L	Register: ADOPTER_ID_L     Field: ADOPTER_ID_L       0     00 - FF				
CDF_CR_DEVICE_ID_H	Register: DEVICE_ID_H     Field: DEVICE_ID_H       0     00 - FF				
CDF_CR_DEVICE_ID_L	Register: DEVICE_ID_L     Field: DEVICE_ID_L       0     00 - FF				
CDF_CR_BANDWIDTH	Register: BANDWIDTH     Field: BANDWIDTH       15     515				
CDF_CR_INT_SIZE	Register: INT_STAT_SIZE     Field: INT_SIZE       4     415				
CDF_CR_STAT_SIZE	Register: INT_STAT_SIZE     Field: STAT_SIZE       4     415				

9. Complete the items in the **RCP Rcv** tab.

You can enter helpful information using the "**Edit Procedure**" dialog box. The information entered into this dialog box will help a test engineer determine if the device behaves properly when the various RCP commands are received.

🗄 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Sink CT 2.0 🛛 🗖 🗖				
1 CDF Entry  √ Test Selection  ► Test Options / Preview				
CDF File: Acme_XYZ_MHL_CBUS_Sink_CDF				
General     Video     Audio     Registers     RCP Rcv     RCP Send     RCP LD Map     UCP Rcv (2.0)     UCP Send (2.0)     O     JD Video (2.0)				
CDF_RCP_RECEIVE If yes, provide expected behavior for this supported RCP command below.				
Select the RCP commands the DUT can receive. Specify the expected behavior for each supported command so that the Test Engineer can verify the correct behavior when each RCP command is received by the DUT.				
CDF_RCP_RCV_BEHAVIOR_00  Ox00: Select  Required By: GUI  Supported? Edit Behavior				
CDF_RCP_RCV_BEHAVIOR_01  Ox01: Up  Required By: GUI Supported? Edit Behavior				
Ox02: Down ()         Required By: GUI         V Supported?				
CDF_RCP_RCV_BEHAVIOR_03  Ox03: Left  Required By: GUI Supported? Edit Behavior				

#### 10. Complete the items in the **RCP Send** tab.

You can enter helpful information using the "**Edit Procedure**" dialog box. The information entered into this dialog box will appear during the test and can be helpful to instruct a test engineer on how to set up a device in order to run a particular test. In the example below you would enter in procedural information which a test engineer could use to cause the sink to issue the various RCP commands.

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掛 Event Plot 🔯 MHL Sink CT 2.0	🔯 CBUS Sink CT 2.0 🛛 🖓 🖓	3
🖄 CDF Entry 🧹 Test Selection	n 🕨 Test Options / Preview	
Copen New Save	CDF File: Acme_XYZ_MHL_CBUS_Sink_CDF	
General Video Au	dio • Registers • RCP Rcv • RCP Send • RCP LD Map • UCP Rcv (2.0) • UCP Send (2.0) • 3D Video (2.0)	
CDF_RCP_SEND	Does the DUT send RCP?       ▲         If yes, provide procedures for each supported RCP command below.       ■         ● Yes       ● No	
	Select the RCP commands the DUT can send. Specify the procedure for each supported command so that the Test Engineer can force the DUT to output each RCP command, using these detailed steps and the DUT's user interface.	
CDF_RCP_SEND_PROCEDURE_00	0x00: Select (1) Supported? Edit Procedure	
CDF_RCP_SEND_PROCEDURE_01	0x01: Up I Supported? Edit Procedure	
CDF_RCP_SEND_PROCEDURE_02	0x02: Down (1) V Supported? Edit Procedure	
CDF_RCP_SEND_PROCEDURE_03	0x03: Left  U Supported? Edit Procedure	
11. Complete the items in the **RCP LD Map** tab.

You can enter helpful information using the "Edit Procedure" dialog box. The information entered into this dialog box will appear during the test to assist the test engineer. In the example below you would enter in procedural information which a test engineer could use to force the sink into the proper mode for further testing of each logical device.

Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Sink CT 2.0 😫					
CDF Entry V Test Selection > Test Options / Preview					
CDF File: Acme_XYZ_MHL_CBUS_Sink_CDF					
General     Video     Audio     Registers     RCP Rcv     RCP Send     RCP LD Map     UCP Rcv (2.0)     UCP Send (2.0)     Send (2.0)					
CDF_LOG_DEV_MAP_CHANGE       Does the DUT support more than one setting in its LOG_DEV_MAP register?         If yes, provide procedures to change to each setting below.         Image: Set the se					
Add as many settings as the DUT supports using the "Add" button below. For each, define a procedure so that the Test Engineer can force the DUT into each of these modes for further testing of each Logical Device.					
Add 🔀 Remove All					
CDF_PROC_LOG_DEV_MAP_1	_				

12. Complete the items in the **UCP Rcv** tab.

You can enter helpful information using the "**Edit Procedure**" dialog box. The information entered into this dialog box will appear during the test to assist a test engineer. You can enter in the expected behavior for each supported command so that the test engineer can verify that the sink DUT behaves properly when receiving the various UCP commands.

🗄 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Sink CT 2.0 🗵	- 8			
😢 CDF Entry 🗹 Test Selection 🕨 Test Options / Preview				
CDF File: Acme_XYZ_MHL_CBUS_Sink_CDF				
General     Video     Audio     Registers     RCP Rcv     RCP Send     RCP LD Map     UCP Rcv     C2.0)     UCP Send     C2.0     O     UCP     Send     C2.0     O     UCP     Send     C2.0     O     UCP     Send     C2.0     O     UCP     Send     C2.0     O     UCP     Send     C2.0     UCP     Send     C2.0     UCP     Send     C2.0     O     UCP     Send     C2.0     UCP     Send     C2.0     O     UCP     Send     C2.0     UCP     Send     Send	2.0)			
CDF_UCP_RECV_SUPPORT Does the DUT support receiving UCP sub-commands?  Ves Ves No				
CDF_UCP_RECV_APPLICATION     Edit Procedure				
UCP Commands				
- Add (# of Entries: 1)				
<b>X</b> Command #01				
Hex Byte Data:				

13. Complete the items in the **UCP Send** tab.

You can enter helpful information using the "**Edit Procedure**" dialog box. The information entered into this dialog box will appear during the test and can be helpful to instruct a test engineer on how to set up a device in

order to run a particular test. In the example below you would enter in procedural information which a test engineer could use to cause the sink to issue the various UCP commands.

🗄 Event Plot 🥸 MHL Sink CT 2.0 🔯 CBUS Sink CT 2.0 🕱 🗧 🗖				
Signature CDF Entry V Test Selection 🕨 Test Options / Preview				
CDF File: Acme_XYZ_MHL_CBUS_Sink_CDF				
General     Video     Audio     Registers     RCP Rcv     RCP Send     RCP LD Map     UCP Rcv (2.0)     UCP Send (2.0)     O     SD Video (2.0)				
CDF_UCP_SEND_SUPPORT Does the DUT support sending UCP sub-commands?				
CDF_UCP_SEND_APPLICATION Edit Procedure				
UCP Commands				
- Add (# of Entries: 1)				
<b>X</b> Command #01				
Hex Byte Data:				

#### 14. Complete the items in the **3D Video** tab.

🗄 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Si	nk CT 2.0 🔀						
🕲 CDF Entry 🧹 Test Selection 🕨 Test O	😢 CDF Entry 🗹 Test Selection 🕨 Test Options / Preview						
CDF File: Ad	cme_XYZ_MHL_C	BUS_Sink_C	DF				
● General ● Video ● Audio ● Reg	isters	cv 🔍 RC	CP Send   RCP LD Map  UC	CP Rcv	(2.0) • UCP Send (2.0) • 3D Video (2.0)		
CDF_VIDEO_3D	Does the DUT so Yes No	upport 3D	video?				
	Suppo	orted Norm	nal Mode 3D Video Formats				
CDF_VIDEO_1280x720P_60_3D_Top_Bottom	🖲 Yes 🔘 No	(4)	1280x720p 59.94/60Hz,	3D,	Top-Bottom		
CDF_VIDEO_1280x720P_50_3D_Top_Bottom	🖲 Yes 🔘 No	(19)	1280x720p 50Hz,	3D,	Top-Bottom		
CDF_VIDEO_1920x1080p_24_Top_Bottom	🖲 Yes 🔘 No	(32)	1920x1080p 23.97/24Hz,	3D,	Top-Bottom		
CDF_VIDEO_1920x1080i_60_3D_Left_Right	🔘 Yes 🔘 No	(5)	1920x1080i 59.94/60Hz,	3D,	Left-Right		
CDF_VIDEO_1920x1080i_50_3D_Left_Right	🔘 Yes 🔘 No	(20)	1920x1080i 50Hz,	3D,	Left-Right		
CDF_VIDEO_1280x720P_60_3D_Frame	🖲 Yes 🔘 No	(4)	1280x720p 59.94/60Hz,	3D,	Frame-Sequential		
CDF_VIDEO_1280x720P_50_3D_Frame	🖲 Yes 🔘 No	(19)	1280x720p 50Hz,	3D,	Frame-Sequential		
CDF_VIDEO_1920x1080p_24_Frame	🖲 Yes 🔘 No	(32)	1920x1080p 23.97/24Hz,	зD,	Frame-Sequential		
Supported PixelPacked Mode 3D Video Formats							
CDF_VIDEO_1280x720P_60_3D_Top_Bottom	🔘 Yes 🔘 No	(4)	1280x720p 59.94/60Hz,	3D,	Top-Bottom		
CDF_VIDEO_1280x720P_50_3D_Top_Bottom	🔘 Yes 🔘 No	(19)	1280x720p 50Hz,	3D,	Top-Bottom		
CDF_VIDEO_1920x1080p_24_Top_Bottom	🔘 Yes 🔘 No	(32)	1920x1080p 23.97/24Hz,	3D,	Top-Bottom		
CDF_VIDEO_1920x1080i_60_3D_Left_Right	🔘 Yes 💿 No	(5)	1920x1080i 59.94/60Hz,	3D,	Left-Right		
CDF_VIDEO_1920x1080i_50_3D_Left_Right	🔘 Yes 🔘 No	(20)	1920x1080i 50Hz,	3D,	Left-Right		
CDF_VIDEO_1280x720P_60_3D_Frame	🔘 Yes 🔘 No	(4)	1280x720p 59.94/60Hz,	3D,	Frame-Sequential		
CDF_VIDEO_1280x720P_50_3D_Frame	🔘 Yes 💿 No	(19)	1280x720p 50Hz,	зD,	Frame-Sequential		
CDF_VIDEO_1920x1080p_24_Frame	🔘 Yes 💿 No	(32)	1920x1080p 23.97/24Hz,	зD,	Frame-Sequential		

15. Save the CDF. If you have not already saved the CDF, you can do so with the **Save** activation button. Alternatively you can save the CDF under a different name.

Save CDF	
🖾 CDF Name	
Enter a name for the CDF	
Acme_XYZ_MHL_CBUS_Sink_CDF_2	-
Acme_XYZ_MHL_CBUS_Sink_CDF         MHL_Display_cdf         My980_CDF         MyCDF_1         MyCDF_Sink	
Cancel Ok	

## 4.7 Selecting which tests to run

Use the following procedures to select the tests to run. There are multiple tabs which correspond to each section in the CTS.

**Note**: The example workflows and screens use MHL 2.0 except where noted. Workflow and screens are similar for testing MHL 1.2 devices.

#### To select the tests to run:

- 1. Select the **Test Selection** panel as shown below.
- 2. If you have an existing Test Selection option file saved you can recall that for use in your testing. Simply click on the **Open** activation button.

🗄 Event Plot 🔤 Edid Editor 🔯 EDID CT 1.4a 🔯 CBUS Sink CT 1.2 🙁 🔯 CBUS Src CT 1.2	- 8
CDF Entry V Test Selection > Test Options / Preview	
C Open Select All Tests Deselect All Tests	
▶ Sink (0/33) ▶ Common (0/68) ▶ EDID/Registers (0/2) ▶ RCP (0/2)	

A dialog box will appear as follows. Simply select the file and click on the **OK** activation button.

**Note**: You can save the Test Selection files to your host PC and transfer them to other PCs and for others to use.

CBUS Sink Compliance Test	
Open Test Selection File	
Select an Test Selection file to open.	
MySelect1.xml	
MySelect_Sink.xml	
Cancel 🛛 🖉 Ok	

3. Complete the items in the **Sink** tab of the **Test Selection** panel shown below.

For convenience you can Select All or Deselect All tests using the activation buttons provided.

Check box indicators inform how many tests in each section and how many are selected. Each tab (Sink, Common or RCP) inform you of how many tests in that section have been selected.

Each test section list includes several tests. In the example shown below, the 4.3.6 Link Layer Timing – DUT Output: Bus Arbitration/Sync/Data Signaling Test section is selected and the specific tests in that section are then available to be selected.

**Note**: Some tests are run in background and cannot be deselected such as the 4.3.3 but there are other background tests within other 4.3.x sections are that are also background. The background tests are highlighted in a light blue as shown in the example below.

Sink (9/34)		
	Common (0/58) EDID/Registers (0/3) RCP (0/2) 3D (0/1) B LICP (0/2)	
▶ 411	TMDS Electrical Tests	0/1
▶ 4.3.3	Link Laver Electrical: Absolute Maximum Voltages	3/3
▶ 4.3.4	Link Layer Electrical - DUT Output: Standby Discovery Impedance	0/1
▶ 4.3.5	Link Laver Timing - DUT Output: Pre-Discovery	0/1
▶ 4.3.6	Link Laver Electrical - DUT Output: Arbitration/Svnc/Data Signaling	4/4
▶ 4.3.7	Link Laver Timing - DUT Output: Arbitration/Sync/Data in Nanoseconds	0/2
▶ 4.3.8	Link Laver Timing - DUT Output: Arbitration/Sync/Data in Bit Times	1/2
▶ 4.3.9	Link Layer Timing - DUT Output: Link Level NACK	0/1
▶ 4.3.10	Link Layer Timing - DUT Output: Link Level ACK	0/2
▶ 4.3.11	Link Layer Timing - DUT Ouput: Bus Re-Arbitration	1/4
▶ 4.3.12	Link Layer Timing - DUT Output: Ill-formed packets	2/2
▶ 4.3.13	Link Layer Electrical - DUT Input: Discovery	0/1
▶ 4.3.14	Link Layer Timing - DUT Input: Discovery OK	3/3 🗹
▶ 4.3.15	Link Layer Timing - DUT Input: Discovery Reject	0/2
▶ 4.3.16	Link Layer Electrical - DUT Input: Arbitration/Sync/Data Signaling	0/1
▶ 4.3.17	Link Layer Timing - DUT Input: Arbitration	2/2
▶ 4.3.18	Link Layer Timing - DUT Input: Data	0/1
▶ 4.3.19	Link Layer Timing - DUT Input: NACK	0/1
▶ 4.3.20	Link Layer Timing - DUT Input: ACK	0/1
▶ 4.3.21	Link Layer Timing - DUT Input: Bus Re-Arbitration	0/1
▶ 4.3.22	Link Layer Timing – DUT Input: Ill-formed Packets	0/1
▶ 4.3.23	Link Layer Timing - DUT Input: Disconnect	0/2
▶ 4.3.24	Link Layer Electrical - DUT VBUS Output	0/1
▶ 4.3.25	Link Layer Timing - DUT VBUS Turn On Transition	0/1

4. Complete the items in the **Common** tab of the **Test Selection** panel shown below.

For convenience you can Select All or Deselect All tests using the activation buttons provided.

CDF Entry Test Selection Test Options / Preview   COPE Save Select All Tests Deselect All Tests   Sink (9/34) Common (0/68) EDD/Registers (0/3) RCP (0/2) 3D (0/1)   4.1.1 TMDS Electrical Tests 0/1   4.3.3 Link Layer Electrical - Absolute Maximum Voltages 3/3   4.3.4 Link Layer Electrical - DUT Output: Standby Discovery Impedance 0/1   4.3.5 Link Layer Timing - DUT Output: Arbitration/Sync/Data Signaling 4/4   4.3.7 Link Layer Timing - DUT Output: Arbitration/Sync/Data in Nanoseconds 0/2   4.3.8 Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times 1/2   4.3.9 Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times 1/2   4.3.9 Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times 1/2   4.3.1 Link Layer Timing - DUT Output: Link Level NACK 0/1   4.3.2 Link Layer Timing - DUT Output: Bit K-Arbitration 1/4   4.3.3 Link Layer Timing - DUT Output: Bit K-Arbitration 1/4   4.3.1 Link Layer Timing - DUT Output: Bit K-Arbitration 1/4   4.3.2 Link Layer Timing - DUT Output: Bit K-Arbitration 1/4   4.3.3 Link Layer Timing - DUT Output: Bit K-Arbitration 1/4   4.3.1 Link Layer Timing - DUT Input: Discovery 0/1   4.3.2 Link Layer Timing - DUT Input: Discovery Reject 0/2   4.3.3 Link Layer Timing - DUT Input: Arbitration 2/2   4.3.4 Link	Event Plot	MHL Sink CT 2.0 🔯 CBUS Sink CT 2.0 🙁		
Image: Solution of the second seco	🖄 CDF Entry	/ 🗸 Test Selection 🕨 Test Options / Preview		
Sink (9/34)         © Common (0/68)         E EDID/Registers (0/3)         P CP (0/2)         P 3D (0/1)         UCP (0/2)           4.1.1         TMDS Electrical Tests         0/1         0/1           4.3.3         Link Layer Electrical Absolute Maximum Voltages         3/3         0/1           4.3.4         Link Layer Electrical - DUT Output: Standby Discovery Impedance         0/1         0/1           4.3.5         Link Layer Timing - DUT Output: Arbitration/Sync/Data Signaling         4/4         0/1           4.3.6         Link Layer Timing - DUT Output: Arbitration/Sync/Data Signaling         4/4         0/2           4.3.6         Link Layer Timing - DUT Output: Arbitration/Sync/Data Signaling         0/2         0/1           4.3.8         Link Layer Timing - DUT Output: Arbitration/Sync/Data Signaling         0/2         0/2           4.3.9         Link Layer Timing - DUT Output: Bus Re-Arbitration         1/2         0/2           4.3.10         Link Layer Timing - DUT Output: Bus Re-Arbitration         1/4         0/2         0/2           4.3.11         Link Layer Timing - DUT Output: Bus Re-Arbitration         1/4         0/2         0/1         0/1         0/1         0/1         0/1         0/1         0/1         0/2         0/1         0/2         0/1         0/1         0/2	🔁 Open	🔜 Save Select All Tests 🔲 Deselect All Tests		
+ 4.1.1       TMDS Electrical Tests       0/1         + 4.3.3       Link Layer Electrical: Absolute Maximum Voltages       3/3       2         + 4.3.4       Link Layer Electrical - DUT Output: Standby Discovery Impedance       0/1       0/1         + 4.3.4       Link Layer Electrical - DUT Output: Standby Discovery Impedance       0/1       0/1         + 4.3.5       Link Layer Electrical - DUT Output: Arbitration/Sync/Data Signaling       4/4       2         + 4.3.7       Link Layer Timing - DUT Output: Arbitration/Sync/Data in Nanoseconds       0/2       0/1         + 4.3.8       Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times       1/2       2         + 4.3.9       Link Layer Timing - DUT Output: Link Level NACK       0/1       0/2         + 4.3.1       Link Layer Timing - DUT Output: Link Level ACK       0/2       0/2         + 4.3.1       Link Layer Timing - DUT Output: Bus Re-Arbitration       1/4       2         + 4.3.1       Link Layer Timing - DUT Output: Bus Re-Arbitration       1/4       2         + 4.3.1       Link Layer Timing - DUT Input: Discovery       0/1       0/1         + 4.3.1       Link Layer Timing - DUT Input: Discovery Reject       0/2       0/2         + 4.3.15       Link Layer Timing - DUT Input: Arbitration/Sync/Data Signaling       0/1 <td< td=""><td>🕨 Sink (9/3</td><td>4) ▶ Common (0/68) ▶ EDID/Registers (0/3) ▶ RCP (0/2) ▶ 3D (0/1) ▶ UCP (0/2)</td><td></td><td></td></td<>	🕨 Sink (9/3	4) ▶ Common (0/68) ▶ EDID/Registers (0/3) ▶ RCP (0/2) ▶ 3D (0/1) ▶ UCP (0/2)		
<ul> <li>4.3.3</li> <li>Link Layer Electrical: Absolute Maximum Voltages</li> <li>3/3</li> <li>4.3.4</li> <li>Link Layer Electrical - DUT Output: Standby Discovery Impedance</li> <li>0/1</li> </ul> <ul> <li>4.3.5</li> <li>Link Layer Electrical - DUT Output: Standby Discovery Impedance</li> <li>0/1</li> </ul> <ul> <li>4.3.5</li> <li>Link Layer Timing - DUT Output: Pre-Discovery</li> <li>0/1</li> </ul> <ul> <li>4.3.5</li> <li>Link Layer Timing - DUT Output: Arbitration/Sync/Data Signaling</li> <li>4/4</li> <li>4.3.7</li> <li>Link Layer Timing - DUT Output: Arbitration/Sync/Data in Nanoseconds</li> <li>0/2</li> </ul> 4.3.9         Link Layer Timing - DUT Output: Link Level NACK         0/1           4.3.9         Link Layer Timing - DUT Output: Link Level ACK         0/2           4.3.10         Link Layer Timing - DUT Output: Link Level ACK         0/2           4.3.11         Link Layer Timing - DUT Output: Link Level ACK         0/1           4.3.12         Link Layer Timing - DUT Output: Link Level ACK         0/1           4.3.13         Link Layer Timing - DUT Input: Discovery         0/1         0/1           4.3.13         Link Layer Timing - DUT Input: Discovery         0/1         0/1         0/1	▶ 4.1.1	TMDS Electrical Tests	0/1	
4.3.4       Link Layer Electrical - DUT Output: Standby Discovery Impedance       0/1         4.3.5       Link Layer Timing - DUT Output: Pre-Discovery       0/1         4.3.6       Link Layer Electrical - DUT Output: Arbitration/Sync/Data Signaling       4/4         4.3.7       Link Layer Timing - DUT Output: Arbitration/Sync/Data in Nanoseconds       0/2         4.3.8       Link Layer Timing - DUT Output: Arbitration/Sync/Data in Nanoseconds       0/2         4.3.8       Link Layer Timing - DUT Output: Link Level NACK       0/1         4.3.9       Link Layer Timing - DUT Output: Link Level NACK       0/2         4.3.10       Link Layer Timing - DUT Output: Link Level ACK       0/2         4.3.11       Link Layer Timing - DUT Output: Bus Re-Arbitration       1/4       1/4         4.3.12       Link Layer Timing - DUT Output: Bus Re-Arbitration       1/4       1/4         4.3.13       Link Layer Timing - DUT Input: Discovery       0/1       1/4         4.3.14       Link Layer Timing - DUT Input: Discovery OK       3/3       2/2         4.3.15       Link Layer Timing - DUT Input: Arbitration/Sync/Data Signaling       0/1       1/4         4.3.16       Link Layer Timing - DUT Input: Arbitration/Sync/Data Signaling       0/1       1/4         4.3.16       Link Layer Timing - DUT Input: Arbitration/Sync/Data Signaling </td <td>▶ 4.3.3</td> <td>Link Layer Electrical: Absolute Maximum Voltages</td> <td>3/3</td> <td></td>	▶ 4.3.3	Link Layer Electrical: Absolute Maximum Voltages	3/3	
<ul> <li>43.5</li> <li>Link Layer Timing - DUT Output: Arbitration/Sync/Data Signaling</li> <li>43.7</li> <li>Link Layer Timing - DUT Output: Arbitration/Sync/Data in Nanoseconds</li> <li>0/2</li> </ul> 43.7         Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times <li>1/2</li> <li>43.9</li> <li>Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times</li> <li>1/2</li> <li>43.9</li> <li>Link Layer Timing - DUT Output: Link Level NACK</li> <li>0/1</li> <li>43.10</li> <li>Link Layer Timing - DUT Output: Bus Re-Arbitration</li> <li>1/4</li> <li>43.11</li> <li>Link Layer Timing - DUT Output: Bus Re-Arbitration</li> <li>1/4</li> <li>43.12</li> <li>Link Layer Timing - DUT Input: Discovery</li> <li>0/1</li> <li>43.13</li> <li>Link Layer Timing - DUT Input: Discovery NK</li> <li>43.14</li> <li>Link Layer Timing - DUT Input: Discovery Reject</li> <li>0/2</li> <li>43.15</li> <li>Link Layer Timing - DUT Input: Arbitration/Sync/Data Signaling</li> <li>0/1</li> <li>43.16</li> <li>Link Layer Timing - DUT Input: Arbitration</li> <li>43.17</li> <li>Link Layer Timing - DUT Input: Arbitration</li> <li>43.20</li> <li>Link Layer Timing - DUT Input: Arbitration</li> <li>43.21</li> <li>Link Layer Timing - DUT Input: Bus Re-Arbitration</li> <li>1/4</li> <li>43.21</li> <li>Link Layer Timing - DUT Input: Bus Re-Arbitration</li> <li>1/1</li> <li>43.21</li> <li>Link Layer Timing - DUT Input: Bus Re-Arbitration</li> <li>1/1</li> <li>43.22</li> <li>Link Layer Timing - DUT Input: Bus Re-Arbitration</li> <li>1/1</li>	▶ 4.3.4	Link Layer Electrical - DUT Output: Standby Discovery Impedance	0/1	
<ul> <li>4.3.6</li> <li>Link Layer Electrical - DUT Output: Arbitration/Sync/Data in Nanoseconds</li> <li>4.3.7</li> <li>Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times</li> <li>4.3.8</li> <li>Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times</li> <li>4.3.9</li> <li>Link Layer Timing - DUT Output: Link Level NACK</li> <li>4.3.10</li> <li>Link Layer Timing - DUT Output: Link Level NACK</li> <li>4.3.11</li> <li>Link Layer Timing - DUT Output: Link Level ACK</li> <li>4.3.12</li> <li>Link Layer Timing - DUT Output: Bis Re-Arbitration</li> <li>4.3.14</li> <li>Link Layer Timing - DUT Output: Discovery</li> <li>4.3.14</li> <li>Link Layer Timing - DUT Input: Discovery OK</li> <li>4.3.14</li> <li>Link Layer Timing - DUT Input: Discovery OK</li> <li>4.3.15</li> <li>Link Layer Timing - DUT Input: Arbitration/Sync/Data Signaling</li> <li>4.3.16</li> <li>Link Layer Timing - DUT Input: Arbitration</li> <li>4.3.17</li> <li>Link Layer Timing - DUT Input: Arbitration</li> <li>4.3.18</li> <li>Link Layer Timing - DUT Input: Arbitration</li> <li>4.3.19</li> <li>Link Layer Timing - DUT Input: Arbitration</li> <li>4.3.20</li> <li>Link Layer Timing - DUT Input: Base</li> <li>A.3.21</li> <li>Link Layer Timing - DUT Input: Arbitration</li> <li>4.3.22</li> <li>Link Layer Timing - DUT Input: Arbitration</li> <li>4.3.20</li> <li>Link Layer Timing - DUT Input: Arbitration</li> <li>4.3.21</li> <li>Link Layer Timing - DUT Input: Arbitration</li> <li>4.3.22</li> <li>Link La</li></ul>	▶ 4.3.5	Link Layer Timing - DUT Output: Pre-Discovery	0/1	
<ul> <li>4.3.7</li> <li>Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times</li> <li>1/2</li> <li>4.3.9</li> <li>Link Layer Timing - DUT Output: Link Level NACK</li> <li>0/2</li> </ul> 0/1                4.3.9         Link Layer Timing - DUT Output: Link Level ACK <li>0/2</li> 0/1                4.3.10         Link Layer Timing - DUT Output: Link Level ACK <li>0/2</li> 0/2                4.3.11         Link Layer Timing - DUT Output: Bus Re-Arbitration             1/4                4.3.11         Link Layer Timing - DUT Output: Ill-formed packets <ld>2/2                4.3.13         Link Layer Timing - DUT Input: Discovery OK                4.3.15             Link Layer Timing - DUT Input: Discovery Reject             0/2               4.3.16             Link Layer Timing - DUT Input: Arbitration/Sync/Data Signaling             <ld>0/1               4.3.17             Link Layer Timing - DUT Input: Arbitration             2/2               4.3.18             Link Layer Timing - DUT Input: Arbitration <li>4.3.19</li>             Link Layer Timing - DUT Input: Arbitration <li>4.3.19</li>             Link Layer Timing - DUT Input: MACK  <ul>             4.3.19             Link Layer Timing - DUT Input: NACK             4.3.20             Link La</ul></ld></ld>	▶ 4.3.6	Link Layer Electrical - DUT Output: Arbitration/Sync/Data Signaling	4/4	
<ul> <li>4.3.8</li> <li>Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times</li> <li>1/2</li> <li>4.3.9</li> <li>Link Layer Timing - DUT Output: Link Level NACK</li> <li>0/1</li> </ul> <ul> <li>4.3.10</li> <li>Link Layer Timing - DUT Output: Link Level ACK</li> <li>0/2</li> </ul> <ul> <li>4.3.11</li> <li>Link Layer Timing - DUT Output: Bis Re-Arbitration</li> <li>1/4</li> <li>4.3.12</li> <li>Link Layer Timing - DUT Output: Bis Covery OK</li> <li>4.3.13</li> <li>Link Layer Timing - DUT Input: Discovery OK</li> <li>4.3.14</li> <li>Link Layer Timing - DUT Input: Discovery Reject</li> <li>0/2</li> </ul> <ul> <li>4.3.15</li> <li>Link Layer Timing - DUT Input: Arbitration/Sync/Data Signaling</li> <li>0/1</li> <li>4.3.18</li> <li>Link Layer Timing - DUT Input: Arbitration</li> <li>4.3.19</li> <li>Link Layer Timing - DUT Input: Arbitration</li> <li>4.3.19</li> <li>Link Layer Timing - DUT Input: Arbitration</li> <li>4.3.19</li> <li>Link Layer Timing - DUT Input: Arbitration</li> <li>4.3.20</li> <li>Link Layer Timing - DUT Input: Arbitration</li> <li>4.3.21</li> <li>Link Layer Timing - DUT Input: Arbitration</li> <li>4.3.22</li> <li>Link Layer Timing - DUT Input: Arbitration</li> <li>4.3.24</li> <li>Link Layer Timing - DUT Input: Arbitration</li> <li>4.3.25</li> <li>Link Layer Timing - DUT Input: Arbitration</li> <li>4.3.24</li> <li>Link Layer Timing - DUT Input: Ar</li></ul>	▶ 4.3.7	Link Layer Timing - DUT Output: Arbitration/Sync/Data in Nanoseconds	0/2	
• 43.9       Link Layer Timing - DUT Output: Link Level NACK       0/1         • 4.3.10       Link Layer Timing - DUT Output: Link Level ACK       0/2         • 4.3.11       Link Layer Timing - DUT Output: Bus Re-Arbitration       1/4       1/4         • 4.3.12       Link Layer Timing - DUT Output: Bus Re-Arbitration       1/4       1/4         • 4.3.12       Link Layer Timing - DUT Output: III-formed packets       2/2       1         • 4.3.13       Link Layer Timing - DUT Input: Discovery       0/1       1         • 4.3.14       Link Layer Timing - DUT Input: Discovery OK       3/3       1         • 4.3.15       Link Layer Timing - DUT Input: Discovery Reject       0/1       1         • 4.3.16       Link Layer Timing - DUT Input: Arbitration/Sync/Data Signaling       0/1       1         • 4.3.18       Link Layer Timing - DUT Input: Data       0/1       1         • 4.3.18       Link Layer Timing - DUT Input: Data       0/1       1         • 4.3.20       Link Layer Timing - DUT Input: NACK       0/1       1         • 4.3.21       Link Layer Timing - DUT Input: MACK       0/1       1         • 4.3.22       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1       1         • 4.3.23       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1<	▶ 4.3.8	Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times	1/2	M
• 4.3.0       Link Layer Timing - DUT Output: Link Level ACK       0/2         • 4.3.11       Link Layer Timing - DUT Output: Bus Re-Arbitration       1/4       2/2         • 4.3.12       Link Layer Timing - DUT Output: Ill-formed packets       2/2       2         • 4.3.13       Link Layer Timing - DUT Input: Discovery       0/1       1/4       2         • 4.3.14       Link Layer Timing - DUT Input: Discovery OK       3/3       2         • 4.3.15       Link Layer Timing - DUT Input: Discovery Reject       0/2       1         • 4.3.16       Link Layer Timing - DUT Input: Arbitration/Sync/Data Signaling       0/1       1         • 4.3.14       Link Layer Timing - DUT Input: Arbitration       2/2       2         • 4.3.15       Link Layer Timing - DUT Input: Arbitration       0/1       1         • 4.3.16       Link Layer Timing - DUT Input: Arbitration       0/1       1         • 4.3.17       Link Layer Timing - DUT Input: Arbitration       0/1       1         • 4.3.19       Link Layer Timing - DUT Input: NACK       0/1       1         • 4.3.20       Link Layer Timing - DUT Input: ACK       0/1       1         • 4.3.21       Link Layer Timing - DUT Input: Disconnect       0/2       1         • 4.3.22       Link Layer Timing - DUT VBUS Output	▶ 4.3.9	Link Layer Timing - DUT Output: Link Level NACK	0/1	
• 4.3.11       Link Layer Timing - DUT Ouput: Bus Re-Arbitration       1/4       ✓         • 4.3.12       Link Layer Timing - DUT Output: Ill-formed packets       2/2       ✓         • 4.3.13       Link Layer Timing - DUT Input: Discovery       0/1       ✓         • 4.3.14       Link Layer Timing - DUT Input: Discovery OK       3/3       ✓         • 4.3.15       Link Layer Timing - DUT Input: Discovery Reject       0/2       ✓         • 4.3.16       Link Layer Timing - DUT Input: Arbitration/Sync/Data Signaling       0/1       ✓         • 4.3.17       Link Layer Timing - DUT Input: Arbitration       2/2       ✓         • 4.3.18       Link Layer Timing - DUT Input: Arbitration       0/1       ✓         • 4.3.19       Link Layer Timing - DUT Input: NACK       0/1       ✓         • 4.3.20       Link Layer Timing - DUT Input: ACK       0/1       ✓         • 4.3.21       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1       ✓         • 4.3.22       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1       ✓         • 4.3.23       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1       ✓         • 4.3.24       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1       ✓         • 4.3.25       Link Layer Timing - D	▶ 4.3.10	Link Layer Timing - DUT Output: Link Level ACK	0/2	
▶ 4.3.12       Link Layer Timing - DUT Output: Ill-formed packets       2/2       ✓         ▶ 4.3.13       Link Layer Timing - DUT Input: Discovery       0/1       ✓         ▶ 4.3.14       Link Layer Timing - DUT Input: Discovery OK       3/3       ✓         ▶ 4.3.15       Link Layer Timing - DUT Input: Discovery Reject       0/2       ✓         ▶ 4.3.16       Link Layer Electrical - DUT Input: Arbitration/Sync/Data Signaling       0/1       ✓         ▶ 4.3.17       Link Layer Timing - DUT Input: Arbitration       2/2       ✓         ▶ 4.3.18       Link Layer Timing - DUT Input: Arbitration       0/1       ✓         ▶ 4.3.19       Link Layer Timing - DUT Input: Arbitration       0/1       ✓         ▶ 4.3.20       Link Layer Timing - DUT Input: ACK       0/1       ✓         ▶ 4.3.21       Link Layer Timing - DUT Input: ACK       0/1       ✓         ▶ 4.3.21       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1       ✓         ▶ 4.3.21       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1       ✓         ▶ 4.3.22       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1       ✓         ▶ 4.3.23       Link Layer Timing - DUT Input: Bus Connect       0/2       ✓         ▶ 4.3.24       Link Layer Electrical - DUT VBU	▶ 4.3.11	Link Layer Timing - DUT Ouput: Bus Re-Arbitration	1/4	
▶ 4.3.13       Link Layer Electrical - DUT Input: Discovery       0/1         ▶ 4.3.14       Link Layer Timing - DUT Input: Discovery OK       3/3       ✓         ▶ 4.3.15       Link Layer Timing - DUT Input: Discovery Reject       0/2       ✓         ▶ 4.3.16       Link Layer Electrical - DUT Input: Arbitration/Sync/Data Signaling       0/1       ✓         ▶ 4.3.17       Link Layer Timing - DUT Input: Arbitration       2/2       ✓         ▶ 4.3.18       Link Layer Timing - DUT Input: Arbitration       2/2       ✓         ▶ 4.3.19       Link Layer Timing - DUT Input: Arbitration       0/1       ✓         ▶ 4.3.20       Link Layer Timing - DUT Input: NACK       0/1       ✓         ▶ 4.3.21       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1       ✓         ▶ 4.3.22       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1       ✓         ▶ 4.3.21       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1       ✓         ▶ 4.3.22       Link Layer Timing - DUT Input: Disconnect       0/2       ✓         ▶ 4.3.23       Link Layer Timing - DUT VBUS Output       0/1       ✓         ▶ 4.3.24       Link Layer Timing - DUT VBUS Turn On Transition       0/1       ✓         ▶ 4.3.25       Link Layer Timing - DUT VBUS Turn On Transitio	▶ 4.3.12	Link Layer Timing - DUT Output: III-formed packets	2/2	
▶ 4.3.14       Link Layer Timing - DUT Input: Discovery OK       3/3       ✓         ▶ 4.3.15       Link Layer Timing - DUT Input: Discovery Reject       0/2       ✓         ▶ 4.3.16       Link Layer Electrical - DUT Input: Arbitration/Sync/Data Signaling       0/1       ✓         ▶ 4.3.17       Link Layer Timing - DUT Input: Arbitration       2/2       ✓         ▶ 4.3.17       Link Layer Timing - DUT Input: Arbitration       2/2       ✓         ▶ 4.3.18       Link Layer Timing - DUT Input: Arbitration       0/1       ✓         ▶ 4.3.19       Link Layer Timing - DUT Input: NACK       0/1       ✓         ▶ 4.3.20       Link Layer Timing - DUT Input: ACK       0/1       ✓         ▶ 4.3.21       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1       ✓         ▶ 4.3.22       Link Layer Timing - DUT Input: Ill-formed Packets       0/1       ✓         ▶ 4.3.23       Link Layer Timing - DUT Input: Disconnect       0/2       ✓         ▶ 4.3.24       Link Layer Timing - DUT VBUS Output       0/1       ✓         ▶ 4.3.25       Link Layer Timing - DUT VBUS Turn On Transition       0/1       ✓         ▶ 4.3.25       Link Layer Timing - DUT VBUS Turn On Transition       0/1       ✓         ▶ 4.3.25       Link Layer Timing - DUT VBUS Turn On Tran	▶ 4.3.13	Link Layer Electrical - DUT Input: Discovery	0/1	
▶ 4.3.15       Link Layer Timing - DUT Input: Discovery Reject       0/2         ▶ 4.3.16       Link Layer Electrical - DUT Input: Arbitration/Sync/Data Signaling       0/1         ▶ 4.3.17       Link Layer Timing - DUT Input: Arbitration       2/2         ▶ 4.3.18       Link Layer Timing - DUT Input: Arbitration       2/2         ▶ 4.3.18       Link Layer Timing - DUT Input: Arbitration       0/1         ▶ 4.3.19       Link Layer Timing - DUT Input: NACK       0/1         ▶ 4.3.20       Link Layer Timing - DUT Input: ACK       0/1         ▶ 4.3.21       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1         ▶ 4.3.22       Link Layer Timing - DUT Input: Use Re-Arbitration       0/1         ▶ 4.3.23       Link Layer Timing - DUT Input: Use Re-Arbitration       0/1         ▶ 4.3.22       Link Layer Timing - DUT Input: Use Re-Arbitration       0/1         ▶ 4.3.23       Link Layer Timing - DUT Input: Disconnect       0/2         ▶ 4.3.24       Link Layer Electrical - DUT VBUS Output       0/1         ▶ 4.3.25       Link Layer Timing - DUT VBUS Turn On Transition       0/1         ▶ 4.3.25       Link Layer Timing - DUT VBUS Turn On Transition       0/1	▶ 4.3.14	Link Layer Timing - DUT Input: Discovery OK	3/3	
▶ 4.3.16       Link Layer Electrical - DUT Input: Arbitration/Sync/Data Signaling       0/1         ▶ 4.3.17       Link Layer Timing - DUT Input: Arbitration       2/2       ☑         ▶ 4.3.18       Link Layer Timing - DUT Input: Arbitration       0/1       ☑         ▶ 4.3.18       Link Layer Timing - DUT Input: Data       0/1       ☑         ▶ 4.3.19       Link Layer Timing - DUT Input: NACK       0/1       ☑         ▶ 4.3.20       Link Layer Timing - DUT Input: ACK       0/1       ☑         ▶ 4.3.21       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1       ☑         ▶ 4.3.22       Link Layer Timing - DUT Input: Ill-formed Packets       0/1       ☑         ▶ 4.3.23       Link Layer Timing - DUT Input: Disconnect       0/2       ☑         ▶ 4.3.24       Link Layer Timing - DUT VBUS Output       0/1       ☑         ▶ 4.3.25       Link Layer Timing - DUT VBUS Turn On Transition       0/1       ☑         ▶ 4.3.25       Link Layer Timing - DUT VBUS Turn On Transition       0/1       ☑	▶ 4.3.15	Link Layer Timing - DUT Input: Discovery Reject	0/2	
▶ 4.3.17       Link Layer Timing - DUT Input: Arbitration       2/2       ☑         ▶ 4.3.18       Link Layer Timing - DUT Input: Data       0/1       ☑         ▶ 4.3.19       Link Layer Timing - DUT Input: NACK       0/1       ☑         ▶ 4.3.20       Link Layer Timing - DUT Input: ACK       0/1       ☑         ▶ 4.3.21       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1       ☑         ▶ 4.3.22       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1       ☑         ▶ 4.3.23       Link Layer Timing - DUT Input: Ill-formed Packets       0/1       ☑         ▶ 4.3.24       Link Layer Timing - DUT Input: Disconnect       0/2       ☑         ▶ 4.3.25       Link Layer Timing - DUT VBUS Output       0/1       ☑         ▶ 4.3.25       Link Layer Timing - DUT VBUS Turn On Transition       0/1       ☑         ▶ 4.3.25       Link Layer Timing - DUT VBUS Turn On Transition       0/1       ☑         ▶ 4.3.25       Link Layer Timing - DUT VBUS Turn On Transition       0/1       ☑	▶ 4.3.16	Link Layer Electrical - DUT Input: Arbitration/Sync/Data Signaling	0/1	
▶ 4.3.18       Link Layer Timing - DUT Input: Data       0/1         ▶ 4.3.19       Link Layer Timing - DUT Input: NACK       0/1         ▶ 4.3.20       Link Layer Timing - DUT Input: ACK       0/1         ▶ 4.3.21       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1         ▶ 4.3.22       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1         ▶ 4.3.23       Link Layer Timing - DUT Input: Ill-formed Packets       0/1         ▶ 4.3.23       Link Layer Timing - DUT Input: Disconnect       0/2         ▶ 4.3.24       Link Layer Timing - DUT VBUS Output       0/1         ▶ 4.3.25       Link Layer Timing - DUT VBUS Turn On Transition       0/1	▶ 4.3.17	Link Layer Timing - DUT Input: Arbitration	2/2	
▶ 4.3.19       Link Layer Timing - DUT Input: NACK       0/1         ▶ 4.3.20       Link Layer Timing - DUT Input: ACK       0/1         ▶ 4.3.21       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1         ▶ 4.3.22       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1         ▶ 4.3.23       Link Layer Timing - DUT Input: Ill-formed Packets       0/1         ▶ 4.3.23       Link Layer Timing - DUT Input: Disconnect       0/2         ▶ 4.3.24       Link Layer Electrical - DUT VBUS Output       0/1         ▶ 4.3.25       Link Layer Timing - DUT VBUS Turn On Transition       0/1         ▶ 4.3.25       Link Layer Timing - DUT VBUS Turn On Transition       0/1	▶ 4.3.18	Link Layer Timing - DUT Input: Data	0/1	
▶ 4.3.20       Link Layer Timing - DUT Input: ACK       0/1         ▶ 4.3.21       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1         ▶ 4.3.22       Link Layer Timing - DUT Input: Ill-formed Packets       0/1         ▶ 4.3.23       Link Layer Timing - DUT Input: Disconnect       0/2         ▶ 4.3.24       Link Layer Electrical - DUT VBUS Output       0/1         ▶ 4.3.25       Link Layer Timing - DUT VBUS Turn On Transition       0/1	▶ 4.3.19	Link Layer Timing - DUT Input: NACK	0/1	
▶ 4.3.21       Link Layer Timing - DUT Input: Bus Re-Arbitration       0/1         ▶ 4.3.22       Link Layer Timing - DUT Input: Ill-formed Packets       0/1         ▶ 4.3.23       Link Layer Timing - DUT Input: Disconnect       0/2         ▶ 4.3.24       Link Layer Electrical - DUT VBUS Output       0/1         ▶ 4.3.25       Link Layer Timing - DUT VBUS Turn On Transition       0/1	▶ 4.3.20	Link Layer Timing - DUT Input: ACK	0/1	
▶ 4.3.22       Link Layer Timing – DUT Input: Ill-formed Packets       0/1         ▶ 4.3.23       Link Layer Timing - DUT Input: Disconnect       0/2         ▶ 4.3.24       Link Layer Electrical - DUT VBUS Output       0/1         ▶ 4.3.25       Link Layer Timing - DUT VBUS Turn On Transition       0/1         ♥ <b>4.3.6.1: CBE-Sink: Post-Discovery Passive Pull-down Z[CBUS_SINK_ON] Resistance</b> ♥ erify that the Sink DUT Z[CBUS SINK ON] has correct value.	▶ 4.3.21	Link Layer Timing - DUT Input: Bus Re-Arbitration	0/1	
<ul> <li>             4.3.23 Link Layer Timing - DUT Input: Disconnect             0/2             4.3.24 Link Layer Electrical - DUT VBUS Output             0/1             4.3.25 Link Layer Timing - DUT VBUS Turn On Transition             0/1             4.3.25             Vink Layer Timing - DUT VBUS Turn On Transition             0/1             4.3.25 Verify that the Sink DUT ZICBUS SINK ONI has correct value.         </li> </ul>	▶ 4.3.22	Link Layer Timing – DUT Input: Ill-formed Packets	0/1	
▶ 4.3.24       Link Layer Electrical - DUT VBUS Output       0/1       ■         ▶ 4.3.25       Link Layer Timing - DUT VBUS Turn On Transition       0/1       ■         ✓ <b>4.3.6.1: CBE-Sink: Post-Discovery Passive Pull-down Z[CBUS_SINK_ON] Resistance</b> ✓         ✓ erify that the Sink DUT Z[CBUS SINK ON] has correct value.       ✓	▶ 4.3.23	Link Layer Timing - DUT Input: Disconnect	0/2	
<ul> <li>▶ 4.3.25 Link Layer Timing - DUT VBUS Turn On Transition</li> <li>Ø/1 ■</li> <li>Ø/2 4.3.6.1: CBE-Sink: Post-Discovery Passive Pull-down Z[CBUS_SINK_ON] Resistance</li> <li>Verify that the Sink DUT Z[CBUS_SINK_ON] has correct value.</li> </ul>	▶ 4.3.24	Link Layer Electrical - DUT VBUS Output	0/1	
✓ 4.3.6.1: CBE-Sink: Post-Discovery Passive Pull-down Z[CBUS_SINK_ON] Resistance Verify that the Sink DUT ZICBUS SINK ONI has correct value.	▶ 4.3.25	Link Layer Timing - DUT VBUS Turn On Transition	0/1	
	<ul> <li>4.3.25</li> <li>4.3</li> <li>Veri</li> </ul>	Link Layer Timing - DUT VBUS Turn On Transition  .6.1: CBE-Sink: Post-Discovery Passive Pull-down Z[CBUS_SINK_ON] Resistance fy that the Sink DUT Z[CBUS_SINK_ON] has correct value.	0/1	•
	<b>4.3</b> Veri	. <b>6.3: CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage</b> fy that Sink DUT drives Arbitration, Sync, and Data Pulses with the correct DRIVE LOW voltage.		

5. Complete the items in the **Common** tab of the **Test Selection** panel shown below.

뒢 Event Plot 🐧	MHL Sink CT 2.0 🔯 CBUS Sink CT 2.0 🖾		- 8
CDF Entry	V Test Selection > Test Options / Preview		
C Open	Save Select All Tests Deselect All Tests		
🕨 Sink (9/34)	► Common (7/68) gisters (0/3) ► RCP (0/2) ► 3D (0/1) ► UCP (0/2)		
▶ 6.3.1	MSC - DUT Input: Device Register Space Contents; Reads	0/1	
▶ 6.3.2	MSC - DUT Output: Vendor-specific and Reserved Header Values	1/1	
6.3.3	MSC - DUT Output: Normal Commands	7/7	
▶ 6.3.5	MSC - DUT Output: Never Initiates Bad Commands	8/8	
▶ 6.3.6	MSC - DUT Output: Errors and Exceptions	0/5	
▶ 6.3.7	MSC - DUT Output: Disconnect	0/1	
▶ 6.3.8	MSC - DUT Input: Device Register Space Contents; Writes	0/2	
▶ 6.3.9	MSC - DUT Input: Vendor-specific and Reserved Header Values	0/1	
▶ 6.3.10	MSC - DUT Input: Normal Commands	0/8	
▶ 6.3.11	MSC - DUT Input: Errors and Exceptions	0/22	
▶ 6.3.12	MSC - DUT Input: Argument Timeouts	0/9	
▶ 6.3.15	MSC - DUT Output: Normal Commands	0/2	
▶ 6.3.16	MSC - DUT Input: Errors and Exceptions	0/2	
▶ 6.3.20	DDC - DUT Input; Continuous Monitors and Normal Operation	2/2	
▶ 6.3.21	DDC - DUT Input; Normal Operation	0/5	
▶ 6.3.22	DDC - DUT Input; Illegal Responses	0/3	
G.3.3 Obser and o for a r	8.1: CBM: DUT sends (0x62) GET_STATE command ve that the DUT sends valid MHL Sideband Channel Commands. Respond with legal results, bserve the DUT responses. Observe that the DUT sends valid GET_STATE commands, and waits esponse before sending another MSC command.		^
6.3.3 Obser and o waits	3.2: CBM: DUT sends (0x63) GET_VENDOR_ID Command ve that the DUT sends valid MHL Sideband Channel Commands. Respond with legal results, bserve the DUT responses. Observe that the DUT sends valid GET_VENDOR_ID commands, and for a response before sending another MSC command.		E
6.3.3 Obser and o and w	3.3: CBM: DUT sends (0x6B) GET_MSC_ERRORCODE Command ve that the DUT sends valid MHL Sideband Channel Commands. Respond with legal results, bserve the DUT responses. Observe that the DUT sends valid GET_MSC_ERRORCODE commands, raits for a response before sending another MSC command.		
G.3.3 Obser and o	8.4: CBM: DUT sends (0x60) SET_INT/WRITE_STAT Command ve that the DUT sends valid MHL Sideband Channel Commands. Respond with legal results, bserve the DUT responses. Observe that the DUT sends valid SET_INT or WRITE_STAT commands,		Ŧ

6. Complete the items in the EDID tab of the Test Selection panel shown below.

🗄 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Sink CT 2.0 🕱	- 8
CDF Entry V Test Selection > Test Options / Preview	
Copen Save Select All Tests Deselect All Tests	
► Sink (9/34) ► Common (7/68) ► EDID/Registers (0/3) ► RCP (0/2) ► 3D (0/1) ► UCP (0/2)	
✓ 4.2.5.1: EDID Test Verify that the DUT EDID is accessible and accurate.	
✓ 4.2.5.2: Device Capability Register Test Verify that the Device Capability Registers have accurate values.	
✓ 4.2.5.3: Device Status Registers Test Verify that the Device Status Registers have proper values.	
(CTS 2.0 Only)	

7. Complete the items in the **RCP** tab of the **Test Selection** panel shown below.

🗄 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Sink CT 2.0 🛛	- 0)			
🔯 CDF Entry 🗸 Test Selection 🕨 Test Options / Preview				
Open       Save         Select All Tests       Deselect All Tests				
▶ Sink (9/34)         ▶ Common (7/68)         ▶ EDID/Registers (0/3)         ▶ RCP (0/2)         ▶ 3D (0/1)         ▶ UCP (0/2)				
✓ 4.2.6.1: RCP Sub-Commands Receiving Test Verify that Sink DUT responds to RCP sub-commands with the expected behavior based on the definitions in the MHL Specification, for each Logical Device claimed to be supported by the Sink DUT.				
4.2.6.2: RCP Sub-Commands Transmitting Test Verify that the Sink DUT outputs each RCP sub-command supported as identified in the CDF, demonstrating the proper opcode and sub-command.				

8. Complete the items in the **3D** tab of the **Test Selection** panel shown below.

🗄 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Sink CT 2.0 🛛	- D)
😢 CDF Entry 🗸 Test Selection 🕨 Test Options / Preview	
Open       Save         Select All Tests       Deselect All Tests	
► Sink (9/34) ► Common (7/68) ► EDID/Registers (0/3) ► RCP (0/2) ► 3D (0/1) ► UCP (0/2)	
4.2.8.1: 3D Video Mode Support Data Verify that the Sink DUT responds to 3D_REQ and sends the list of 3D video modes supported by the DUT.	
(CTS 2.0 Only)	

9. Complete the items in the UCP tab of the Test Selection panel shown below.

🗄 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Sink CT 2.0 🗵	
CDF Entry 🗸 Test Selection 🕨 Test Options / Preview	
Copen Save Select All Tests Deselect All Tests	
▶ Sink (9/34) ▶ Common (7/68) ▶ EDID/Registers (0/3) ▶ RCP (0/2) ▶ 3D (0/1) ▶ UCP (0/2)	
<ul> <li>4.2.9.1: UCP Sub-Commands Receiving Test         Verify that the DUT responds to valid UCP sub-commands by displaying the character         or characters sent in the UCP command, or response to invalid UCP sub-commands by         displaying an error message.         (CTS 2.0 Only)</li> </ul>	
<ul> <li>4.2.9.2: UCP Sub-Commands Transmitting Test         Verify that the DUT sends valid UCP sub-commands by initiating the sending of UTF-8             characters in various formats through the user interface on the DUT.         (CTS 2.0 Only)         </li> </ul>	

10. You can save the Test Selection options using the **Save** activation button.

🗄 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Sink CT 2.0 🖂	
CDF Entry V Test Selection > Test Options / Preview	
Copen Save Lect All Tests Deselect All Tests	
▶ Sink (9/34) ▶ Common (7/68) ▶ EDID/Registers (0/3) ▶ RCP (0/2) ▶ 3D (0/1) ▶ UCP (0/2)	

11. A dialog box will appear as follows. Simply assign a name and click on the **OK** activation button. Click **Cancel** to exit.

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# 4.8 Executing the MHL CBUS Sink Compliance Tests

Use the following procedures to initiate the execution of an MHL CBUS Sink Compliance test series.

**Note**: The example workflows and screens use MHL 2.0 except where noted. Workflow and screens are similar for testing MHL 1.2 devices.

#### To initiate a test series:

1. Select the **Test Options / Preview** panel as shown below.

**Note**: The background tests are highlighted in light blue. These are tests that are run in the background during the remaining test suite. Refer to the two screen shots below.

COF Entry       Test Selection       Test Options/ Preview         Test Ust       Test Ust         All       Instrument:       My980 [192:168:254:163]       Execute         Category / Test Name       Image: Category / Test Name       Image: Category / Test Name       Image: Category / Test Name         Category / Test Name       Image: Category / Test Name       Image: Category / Test Name       Image: Category / Test Name         Category / Test Name       Image: Category / Test Name         Category / Test Name       Image: Category / Test Name         Category / Test Name       Image: Category / Test Name         Category / Test Name       Image: Category / Test Name         Category / Test Name       Image: Category / Test Name         Category / Sub / Commands Transmitting Test       Image: Category / Test Name       Image: Category / Test Name       Image: Category / Test Name       Image: Category / T	- 8
Testist         Instrument       My980 [192168.254163]         Category / Test Name       Image: Category / Test Name         Label 2.5.1: EDID Test       Image: Category / Test Name         Label 2.5.1: EDID Test       Image: Category / Test Name         Label 2.5.1: EDID Test       Image: Category / Test Name         Label 2.5.1: EDID Test       Image: Category / Test Name         Label 2.5.1: EDID Test       Image: Category / Test Name         Label 2.5.1: EDID Test       Image: Category / Test Name         Label 2.5.2: Device Capability Register Test       Image: Category / Test Name         Label 2.5.2: Device Status Registers Test       Image: Category / Test Name         Label 2.5.2: Device Status Registers Test       Image: Category / Test Name         Label 2.5.2: Device Status Registers Test       Image: Category / Test Name         Label 2.5.2: DUCP Sub-Commands Receiving Test       Image: Category / Test Name         Label 2.5.2: UCP Sub-Commands Transmitting Test       Image: Category / Test Name         Label 2.5.2: UCP Sub-Commands Transmitting Test       Image: Category / Test Name         Label 3.3: Category Net Commands       Image: Category / Test Name         Label 4.3.3: Category Net Commands       Image: Category Net Cotegory         Label 4.3: A.3: Category Net Cotegory Passive Pull-down Z[CBUS SINK ON] Resistance       Image: Category NetC	
All Instrument: My800 [192168.254.163]   Category / Test Name Image: Category / Test Name   A.2.5: EDID Test and Device Capability / Device Status Register Test   A.2.5: EDVice Capability Register Test   A.2.5.: Device Status Register Test   A.2.5: 2.5:   A.2.5: Device Status Register Test   A.2.5: Device Status Register Test   A.2.5: Device Status Register Test   A.2.6: 3.0 Video Test   A.2.8: 3.0 Video Mode Support Data   A.2.9: UCP Sub-Command Tests   A.2.9: UCP Sub-Commands Receiving Test   Iter 01: Test all supported Commands.   A.3.2: UCP Sub-Commands Transmitting Test   Iter 01: Test all supported Commands.   A.3.3: Link Laver Electrical: Absolute Maximum Voltages   A.3.3: CBE-Sink: CBUS Absolute Maximum Positive Voltage   A.3.6: Link Laver Electrical - DUT Output: Arbitration/Sync/Data Signaling   A.3.6.1: CBE-Sink: CBUS Capacitance   A.3.6.1: CBE-Sink: CBUS Capacitance   A.3.6.2: CBE-Sink: Arbitrate/Sync/Data Drive HICH Voltage   A.3.6.1: CBE-Sink: Arbitrate/Sync/Data Drive HICH Voltage   A.3.6.2: CBE-Sink: Arbitrate/Sync/Data Drive HICH Voltage   A.3.6.2: CBE-Sink: Arbitrate/Sync/Data Drive HICH Voltage   A.3.6.2: CBE-Sink: Bit Timing Variation within a Packet   A.3.6.1: Laver Timing - DUT Output: Arbitration/Sync/Data in Bit Times   A.3.6.2: CBE-Sink: Bit T	
<ul> <li>Category / Test Name</li> <li>A.2.5: EDID Test and Device Capability / Device Status Register Test</li> <li>4.2.5.1: EDID Test</li> <li>4.2.5.1: EDID Test</li> <li>4.2.5.2: Device Capability Register Test</li> <li>4.2.5.3: Device Status Registers Test</li> <li>4.2.8: 3D Video Test</li> <li>4.2.8: 3D Video Mode Support Data</li> <li>4.2.9: UCP Sub-Command Tests</li> <li>4.2.9: UCP Sub-Commands Receiving Test</li> <li>1.4.2.9: UCP Sub-Commands Receiving Test</li> <li>1.4.3.3: Link Layer Electrical: Absolute Maximum Voltages</li> <li>4.3.3: CBE-Sink: CBUS Absolute Maximum Positive Voltage</li> <li>4.3.6: Link Layer Electrical - DUT Output: Arbitration/Sync/Data Signaling</li> <li>4.3.6: CBE-Sink: CBUS-Discovery Pasive Pull-down Z[CBUS SINK ON] Resistance</li> <li>4.3.6: CBE-Sink: Arbitrate/Sync/Data Drive HOW Voltage</li> <li>4.3.6: CBE-Sink: Arbitrate/Sync/Data Drive HOW Voltage</li> <li>4.3.6: CBE-Sink: Bit Timing Variation within a Packet</li> <li>4.3.11: Link Layer Timing - DUT Output: Bus Re-Arbitration</li> <li>4.3.11: Link Layer Timing - DUT Output: Ill-formed packets</li> <li>4.3.12: CBT-Sink: Sink Never Sends Too Many Back-to-Back Packets</li> </ul>	ests
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<ul> <li>4.2.5.1: EDID Test</li> <li>4.2.5.2: Device Capability Register Test</li> <li>4.2.5.3: Device Status Registers Test</li> <li>4.2.5.3: Device Status Registers Test</li> <li>4.2.8: 3D Video Test</li> <li>4.2.8: 3D Video Test</li> <li>4.2.9: UCP Sub-Command Tests</li> <li>4.2.9.1: UCP Sub-Commands Receiving Test</li> <li>1ter 01: Test all supported Commands.</li> <li>4.3.3: Link Laver Electrical: Absolute Maximum Voltages</li> <li>4.3.6.1: CBE-Sink: CBUS Absolute Maximum Positive Voltage</li> <li>4.3.6.2: CBE-Sink: CBUS Capacitance</li> <li>4.3.6.3: CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage</li> <li>4.3.6.4: CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage</li> <li>4.3.6.1: CBE-Sink: Bit Timing Variation within a Packet</li> <li>4.3.11: Link Laver Timing - DUT Output: Rus Re-Arbitration</li> <li>4.3.11: Link Laver Timing - DUT Output: Ill-formed packets</li> <li>4.3.12: Link Laver Timing - DUT Output: Ill-formed packets</li> <li>4.3.12: Link Laver Timing - DUT Output: Ill-formed packets</li> <li>4.3.12: Link Laver Timing - DUT Output: Ill-formed packets</li> <li>4.3.12: Link Laver Timing - DUT Output: Ill-formed packets</li> </ul>	
<ul> <li>4.2.5.2: Device Capability Register Test</li> <li>4.2.5.3: Device Status Registers Test</li> <li>4.2.5.3: Device Status Registers Test</li> <li>4.2.8.1: 3D Video Test</li> <li>4.2.8.1: 3D Video Mode Support Data</li> <li>4.2.9: UCP Sub-Command Tests</li> <li>4.2.9.1: UCP Sub-Commands Receiving Test</li> <li>Iter 01: Test all supported Commands.</li> <li>4.2.9.2: UCP Sub-Commands Transmitting Test</li> <li>Iter 01: Test all supported Commands.</li> <li>4.3.3: Link Layer Electrical: Absolute Maximum Voltages</li> <li>4.3.3: CBE-Sink: VBUS Absolute Maximum Positive Voltage</li> <li>4.3.6: Link Layer Electrical - DUT Output: Arbitration/Sync/Data Signaling</li> <li>4.3.6.1: CBE-Sink: CBUS Capacitance</li> <li>4.3.6.1: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage</li> <li>4.3.6.1: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage</li> <li>4.3.6.1: CBE-Sink: Bit Timing - DUT Output: Arbitration/Sync/Data in Bit Times</li> <li>4.3.8.12: CBT-Sink: Sink Never Sends Tool any Back-to-Back Packets</li> <li>4.3.12: Link Layer Timing - DUT Output: Ill-formed packets</li> <li>4.3.12: Link Layer Timing - DUT Output: Ill-formed packets</li> </ul>	
<ul> <li>4.2.5.3: Device Status Registers Test</li> <li>4.2.8: 3D Video Test</li> <li>4.2.8.1: 3D Video Mode Support Data</li> <li>4.2.8.1: 3D Video Mode Support Data</li> <li>4.2.9.1: UCP Sub-Command Tests</li> <li>4.2.9.1: UCP Sub-Commands Receiving Test</li> <li>6.1 Ter 01: Test all supported Commands.</li> <li>4.2.9.2: UCP Sub-Commands Transmitting Test</li> <li>4.3.3: Link Layer Electrical: Absolute Maximum Voltages</li> <li>4.3.3.2: CBE-Sink: VBUS Absolute Maximum Positive Voltage</li> <li>4.3.6.1: CBE-Sink: CBUS Capacitance</li> <li>4.3.6.2: CBE-Sink: CBUS Capacitance</li> <li>4.3.6.3: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage</li> <li>4.3.6.4: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage</li> <li>4.3.8.2: CBT-Sink: Bit Timing Variation within a Packet</li> <li>4.3.11: Link Layer Timing - DUT Output: HUGH Voltage</li> <li>4.3.11.4: CBT-Sink: Sink Never Sends Top May Back-to-Back Packets</li> <li>4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise</li> </ul>	
<pre>4 \$ 4.2.8: 3D Video Test     4.2.8: 3D Video Test     4.2.8: 3D Video Mode Support Data     4.2.8: 3D Video Mode Support Data     4.2.9: UCP Sub-Command Tests     4.2.9: UCP Sub-Commands Receiving Test     1    Iter 01: Test all supported Commands.     4.3.3: Link Layer Electrical: Absolute Maximum Voltages     4.3.3: CBE-Sink: VBUS Absolute Maximum Positive Voltage     4.3.6: Link Layer Electrical - DUT Output: Arbitration/Sync/Data Signaling     4.3.6.1: CBE-Sink: CBUS Capacitance     4.3.6.2: CBE-Sink: CBUS Capacitance     4.3.6.4: CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage     4.3.6.4: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage     4.3.8: Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times     4.3.8.1: CBT-Sink: Sink Never Sends Too Many Back-to-Back Packets     4.3.12: Link Layer Timing - DUT Output: Ill-formed packets     4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise     4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise     4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise </pre>	_
<ul> <li>4.2.8.1: 3D Video Mode Support Data</li> <li>4.2.9: UCP Sub-Command Tests</li> <li>4.2.9.1: UCP Sub-Commands Receiving Test</li> <li>Iter 01: Test all supported Commands.</li> <li>4.2.9.2: UCP Sub-Commands Transmitting Test</li> <li>Iter 01: Test all supported Commands.</li> <li>4.3.3: Link Laver Electrical: Absolute Maximum Voltages</li> <li>4.3.3.1: Common Test Environment</li> <li>4.3.3.2: CBE-Sink: VBUS Absolute Maximum Positive Voltage</li> <li>4.3.6: Link Laver Electrical - DUT Output: Arbitration/Svnc/Data Signaling</li> <li>4.3.6.3: CBE-Sink: CBUS Capacitance</li> <li>4.3.6.4: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage</li> <li>4.3.8: Link Laver Timing - DUT Output: Arbitration/Svnc/Data in Bit Times</li> <li>4.3.11: Link Laver Timing - DUT Output: Bus Re-Arbitration</li> <li>4.3.12: Link Laver Timing - DUT Output: Ill-formed packets</li> <li>4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise</li> </ul>	
<pre>4 ▶ 4.2.9: UCP Sub-Command Tests 4 ↓ 4.2.9.1: UCP Sub-Commands Receiving Test • Iter 01: Test all supported Commands. 4 ↓ 4.2.9.2: UCP Sub-Commands Transmitting Test • Iter 01: Test all supported Commands. 4 ↓ 4.3.3: Link Layer Electrical: Absolute Maximum Voltages • ↓ 4.3.3: CBE-Sink: VBUS Absolute Maximum Positive Voltage • ↓ 4.3.3.2: CBE-Sink: VBUS Absolute Maximum Positive Voltage • ↓ 4.3.3.3: CBE-Sink: CBUS Absolute Maximum Positive Voltage • ↓ 4.3.6: Link Layer Electrical - DUT Output: Arbitration/Sync/Data Signaling ↓ 4.3.6.2: CBE-Sink: Post-Discovery Passive Pull-down Z[CBUS SINK ON] Resistance ↓ ↓ 4.3.6.3: CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage ↓ ↓ 4.3.6.4: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage ↓ ↓ 4.3.8: Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times ↓ ↓ 4.3.11: Link Layer Timing - DUT Output: Bus Re-Arbitration ↓ ↓ 4.3.11: Link Layer Timing - DUT Output: Bus Re-Arbitration ↓ ↓ 4.3.11: Link Layer Timing - DUT Output: Ill-formed packets ↓ ↓ 4.3.12: Link Layer Timing - DUT Output: Ill-formed packets ↓ ↓ 4.3.12: Link Layer Timing - DUT Output: Ill-formed packets ↓ ↓ 4.3.12: Link Layer Timing - DUT Output: Sus Re-Arbitration ↓ ↓ 4.3.12: Link Layer Timing - DUT Output: Sus Re-Arbitration ↓ ↓ 4.3.12: Link Layer Timing - DUT Output: Sus Re-Arbitration ↓ ↓ 4.3.12: Link Layer Timing - DUT Output: Sus Re-Arbitration ↓ ↓ 4.3.12: Link Layer Timing - DUT Output: Sus Re-Arbitration ↓ ↓ 4.3.12: Link Layer Timing - DUT Output: Sus Re-Arbitration ↓ ↓ 4.3.12: Link Layer Timing - DUT Output: Sus Re-Arbitration ↓ ↓ 4.3.12: Link Layer Timing - DUT Output: Sus Re-Arbitration ↓ ↓ 4.3.12: Link Layer Timing - DUT Output: Sus Re-Arbitration ↓ ↓ 4.3.12: Link Layer Timing - DUT Output: Sus Re-Arbitration ↓ ↓ 4.3.12: Link Layer Timing - DUT Output: Sus Re-Arbitration ↓ ↓ 4.3.12: Link Layer Timing - DUT Output: Sus Re-Arbitration ↓ ↓ 4.3.12: Link Layer Timing - DUT Output: Sus Re-Arbitration ↓ ↓ 4.3.12: CBT-Sink: Sink Never Sends Impulse Noise</pre>	
<ul> <li>4.2.9.1: UCP Sub-Commands Receiving Test</li> <li>Iter 01: Test all supported Commands.</li> <li>4.2.9.2: UCP Sub-Commands Transmitting Test</li> <li>Iter 01: Test all supported Commands.</li> <li>4.3.3: Link Laver Electrical: Absolute Maximum Voltages</li> <li>4.3.3: CBE-Sink: CBUS Absolute Maximum Positive Voltage</li> <li>4.3.3: CBE-Sink: CBUS Absolute Maximum Positive Voltage</li> <li>4.3.6: Link Laver Electrical - DUT Output: Arbitration/Sync/Data Signaling</li> <li>4.3.6: CBE-Sink: CBUS Capacitance</li> <li>4.3.6: CBE-Sink: CBUS Capacitance</li> <li>4.3.6: CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage</li> <li>4.3.6: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage</li> <li>4.3.8: Link Laver Timing - DUT Output: Arbitration/Sync/Data in Bit Times</li> <li>4.3.11: Link Laver Timing - DUT Output: Bus Re-Arbitration</li> <li>4.3.11: Link Laver Timing - DUT Output: Bus Re-Arbitration</li> <li>4.3.11: Link Laver Timing - DUT Output: Bus Re-Arbitration</li> <li>4.3.11: Link Laver Timing - DUT Output: Bus Re-Arbitration</li> <li>4.3.12: Link Laver Timing - DUT Output: Till-formed packets</li> </ul>	
<ul> <li>Iter 01: Test all supported Commands.</li> <li>4.2.9.2: UCP Sub-Commands Transmitting Test</li> <li>Iter 01: Test all supported Commands.</li> <li>4.3.3: Link Laver Electrical: Absolute Maximum Voltages</li> <li>4.3.3: Common Test Environment</li> <li>4.3.3.2: CBE-Sink: VBUS Absolute Maximum Positive Voltage</li> <li>4.3.3: CBE-Sink: CBUS Absolute Maximum Positive Voltage</li> <li>4.3.6: Link Laver Electrical - DUT Output: Arbitration/Sync/Data Signaling</li> <li>4.3.6.1: CBE-Sink: CBUS Capacitance</li> <li>4.3.6.2: CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage</li> <li>4.3.6.4: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage</li> <li>4.3.8.2: CBE-Sink: Bit Timing - DUT Output: Arbitration/Sync/Data in Bit Times</li> <li>4.3.8.2: CBT-Sink: Sink Never Sends Too Many Back-to-Back Packets</li> <li>4.3.12: Link Laver Timing - DUT Output: Ill-formed packets</li> <li>4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise</li> </ul>	=
<pre>4 E 4.2.9.2: UCP Sub-Commands Transmitting Test • Iter 01: Test all supported Commands. 4 • 4.3.3: Link Laver Electrical: Absolute Maximum Voltages • 4.3.3: Common Test Environment • 4.3.3: CBE-Sink: VBUS Absolute Maximum Positive Voltage • 4.3.3: CBE-Sink: CBUS Absolute Maximum Positive Voltage • 4.3.6: Link Laver Electrical - DUT Output: Arbitration/Sync/Data Signaling • 4.3.6: CBE-Sink: CBUS Capacitance • 4.3.6.2: CBE-Sink: CBUS Capacitance • 4.3.6.3: CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage • 4.3.6.4: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage • 4.3.8: Link Laver Timing - DUT Output: Arbitration/Sync/Data in Bit Times • 4.3.8: Link Laver Timing - DUT Output: Bus Re-Arbitration • 4.3.11: Link Laver Timing - DUT Output: Bus Re-Arbitration • 4.3.11: Link Laver Timing - DUT Output: Ill-formed packets • 4.3.12: Link Laver Timing - DUT Output: Ill-formed packets • 4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise</pre>	_
<ul> <li>Iter 01: Test all supported Commands.</li> <li>4 &gt; 4.3.3: Link Laver Electrical: Absolute Maximum Voltages</li> <li>4.3.3: Common Test Environment</li> <li>4.3.3: CBE-Sink: VBUS Absolute Maximum Positive Voltage</li> <li>4.3.3: CBE-Sink: CBUS Absolute Maximum Positive Voltage</li> <li>4.3.6: Link Laver Electrical - DUT Output: Arbitration/Sync/Data Signaling</li> <li>4.3.6.1: CBE-Sink: Post-Discovery Passive Pull-down Z[CBUS SINK ON] Resistance</li> <li>4.3.6.2: CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage</li> <li>4.3.6.3: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage</li> <li>4.3.6.4: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage</li> <li>4.3.8: Link Laver Timing - DUT Output: Arbitration/Sync/Data in Bit Times</li> <li>4.3.11: Link Laver Timing - DUT Output: Bus Re-Arbitration</li> <li>4.3.12: Link Laver Timing - DUT Output: Ill-formed packets</li> <li>4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise</li> </ul>	_
<pre>4 4.3.3: Link Laver Electrical: Absolute Maximum Voltages  4 4.3.3: Link Laver Electrical: Absolute Maximum Positive Voltage  4 4.3.3: CBE-Sink: VBUS Absolute Maximum Positive Voltage  4 4.3.3: CBE-Sink: CBUS Absolute Maximum Positive Voltage  4 4.3.6: Link Laver Electrical - DUT Output: Arbitration/Sync/Data Signaling  4 4.3.6: CBE-Sink: Post-Discovery Passive Pull-down Z[CBUS SINK ON] Resistance  4 4.3.6: CBE-Sink: CBUS Capacitance  4 4.3.6: CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage  4 4.3.6: CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage  4 4.3.6: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage  4 4.3.8: Link Laver Timing - DUT Output: Arbitration/Sync/Data in Bit Times  4 4.3.11: Link Laver Timing - DUT Output: Bus Re-Arbitration  4 4.3.11: Link Laver Timing - DUT Output: Ill-formed packets  4 4.3.12: Link Laver Timing - DUT Output: Ill-formed packets  4 4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise  4 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5</pre>	
<ul> <li>4.3.3.1: Common Test Environment</li> <li>4.3.3.1: Common Test Environment</li> <li>4.3.3.2: CBE-Sink: VBUS Absolute Maximum Positive Voltage</li> <li>4.3.3.3: CBE-Sink: CBUS Absolute Maximum Positive Voltage</li> <li>4.3.6: Link Laver Electrical - DUT Output: Arbitration/Sync/Data Signaling</li> <li>4.3.6.1: CBE-Sink: Post-Discovery Passive Pull-down Z[CBUS SINK ON] Resistance</li> <li>4.3.6.2: CBE-Sink: CBUS Capacitance</li> <li>4.3.6.3: CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage</li> <li>4.3.6.4: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage</li> <li>4.3.8: Link Laver Timing - DUT Output: Arbitration/Sync/Data in Bit Times</li> <li>4.3.8.2: CBT-Sink: Bit Timing Variation within a Packet</li> <li>4.3.11: Link Laver Timing - DUT Output: Bus Re-Arbitration</li> <li>4.3.12: Link Laver Timing - DUT Output: Ill-formed packets</li> <li>4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise</li> </ul>	
<pre> 4.3.3.2: CBE-Sink: VBOS Absolute Maximum Positive Voltage 4.3.3.3: CBE-Sink: CBUS Absolute Maximum Positive Voltage 4.3.6: Link Laver Electrical - DUT Output: Arbitration/Sync/Data Signaling 4.3.6.1: CBE-Sink: Post-Discovery Passive Pull-down Z[CBUS SINK ON] Resistance 4.3.6.2: CBE-Sink: CBUS Capacitance 4.3.6.3: CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage 4.3.6.4: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage 4.3.8: Link Laver Timing - DUT Output: Arbitration/Sync/Data in Bit Times 4.3.11: Link Laver Timing - DUT Output: Bus Re-Arbitration 4.3.11: Link Laver Timing - DUT Output: Bus Re-Arbitration 4.3.11: Link Laver Timing - DUT Output: Ill-formed packets 4.3.12: Link Laver Timing - DUT Output: Ill-formed packets 4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise 4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise 4.3.12: Link Laver Timing - DUT Output: Might Noise 4.3.12: CBT-Sink: Sink Never Sends Impulse Noise 4.3.12: CBT-Sink: Sink Never Sends Impulse Noise 4.3.12: Link Laver Timing - DUT Output: Ill-formed packets 4.3.12: CBT-Sink: Sink Never Sends Impulse Noise 4.3.12: CBT-Sink:</pre>	
<ul> <li>4.3.3.3: CBE-SINK: CBOS ADSolute Maximum Positive Voltage</li> <li>4.3.6: Link Laver Electrical - DUT Output: Arbitration/Sync/Data Signaling</li> <li>4.3.6.1: CBE-Sink: Post-Discovery Passive Pull-down Z[CBUS SINK ON] Resistance</li> <li>4.3.6.2: CBE-Sink: CBUS Capacitance</li> <li>4.3.6.3: CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage</li> <li>4.3.6.4: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage</li> <li>4.3.8. Link Laver Timing - DUT Output: Arbitration/Sync/Data in Bit Times</li> <li>4.3.11: Link Laver Timing - DUT Output: Bus Re-Arbitration</li> <li>4.3.11: Link Laver Timing - DUT Output: Ill-formed packets</li> <li>4.3.12: Link Laver Timing - DUT Output: Ill-formed packets</li> </ul>	
<ul> <li>4.3.6: Link Laver Electrical - Dot Output: Arbitration/Sync/Data Signaling</li> <li>4.3.6.1: CBE-Sink: Post-Discovery Passive Pull-down Z[CBUS SINK ON] Resistance</li> <li>4.3.6.2: CBE-Sink: CBUS Capacitance</li> <li>4.3.6.3: CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage</li> <li>4.3.6.4: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage</li> <li>4.3.8. Link Laver Timing - DUT Output: Arbitration/Sync/Data in Bit Times</li> <li>4.3.11: Link Laver Timing - DUT Output: Bus Re-Arbitration</li> <li>4.3.11: Link Laver Timing - DUT Output: Ill-formed packets</li> <li>4.3.12: Link Laver Timing - DUT Output: Ill-formed packets</li> </ul>	_
<ul> <li>4.3.6.1: CBE Sink: Fost-Discovery Pastive Full down Flebos Sink ON Resistance</li> <li>4.3.6.2: CBE-Sink: CBUS Capacitance</li> <li>4.3.6.3: CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage</li> <li>4.3.6.4: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage</li> <li>4.3.8: Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times</li> <li>4.3.11: Link Layer Timing - DUT Output: Bus Re-Arbitration</li> <li>4.3.11: Link Layer Timing - DUT Output: Bus Re-Arbitration</li> <li>4.3.11: Link Layer Timing - DUT Output: Ill-formed packets</li> <li>4.3.12: Link Layer Timing - DUT Output: Ill-formed packets</li> </ul>	
<ul> <li>4.3.6.12: CBE Sink: Color Supervisite</li> <li>4.3.6.3: CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage</li> <li>4.3.6.4: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage</li> <li>4.3.8: Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times</li> <li>4.3.11: Link Layer Timing - DUT Output: Bus Re-Arbitration</li> <li>4.3.11: Link Layer Timing - DUT Output: Bus Re-Arbitration</li> <li>4.3.11: Link Layer Timing - DUT Output: Bus Re-Arbitration</li> <li>4.3.11: Link Layer Timing - DUT Output: Bus Re-Arbitration</li> <li>4.3.12: Link Layer Timing - DUT Output: Ill-formed packets</li> <li>4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise</li> </ul>	
<ul> <li>4.3.6.4: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage</li> <li>4.3.8: Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times</li> <li>4.3.8.2: CBT-Sink: Bit Timing Variation within a Packet</li> <li>4.3.11: Link Layer Timing - DUT Ouput: Bus Re-Arbitration</li> <li>4.3.11: Link Layer Timing - DUT Output: Bus Re-Arbitration</li> <li>4.3.12: Link Layer Timing - DUT Output: Ill-formed packets</li> <li>4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise</li> </ul>	
<ul> <li>4 &gt; 4.3.8: Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times</li> <li>4 &gt; 4.3.8.2: CBT-Sink: Bit Timing Variation within a Packet</li> <li>4 &gt; 4.3.11: Link Layer Timing - DUT Ouput: Bus Re-Arbitration</li> <li>4 - 4.3.11: Link Layer Timing - DUT Ouput: Bus Re-Arbitration</li> <li>4 - 4.3.12: Link Layer Timing - DUT Output: Ill-formed packets</li> <li>4 - 4.3.12: Link Layer Timing - DUT Output: Ill-formed packets</li> </ul>	
<ul> <li>4.3.8.2: CBT-Sink: Bit Timing Variation within a Packet</li> <li>4.3.11: Link Layer Timing - DUT Ouput: Bus Re-Arbitration</li> <li>4.3.12: Link Layer Timing - DUT Output: Ill-formed packets</li> <li>4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise</li> </ul>	
<ul> <li>4.3.11: Link Layer Timing - DUT Ouput: Bus Re-Arbitration</li> <li>4.3.11.4: CBT-Sink: Sink Never Sends Too Many Back-to-Back Packets</li> <li>4.3.12: Link Layer Timing - DUT Output: Ill-formed packets</li> <li>4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise</li> </ul>	
<ul> <li>▷ = 4.3.11.4: CBT-Sink: Sink Never Sends Too Many Back-to-Back Packets</li> <li>✓ 4.3.12: Link Laver Timing - DUT Output: Ill-formed packets</li> <li>○ = 4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise</li> </ul>	
▲ ▶ 4.3.12: Link Layer Timing - DUT Output: Ill-formed packets         ▷ ■ 4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise	
0 🖪 4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise 🗸 🗸	
🛛 📃 4.3.12.2: CBT-Sink: Sink Never Sends Partial Packets 🛛 🖌 🗸	
4.3.14: Link Layer Timing - DUT Input: Discovery OK	
🛛 🔄 4.3.14.1: CBT-Sink: Valid Wake Pulse Timing 🛛 🗸 🗸	
🛛 🖪 4.3.14.2: CBT-Sink: Valid Discovery Pulse Timing 🛛 🗸 🗸	
🛛 📃 4.3.14.3: CBT-Sink: Sink in Standby Discovers on Wake plus Discovery Pulse Sequel💙	
<ul> <li>Iter 01: PROC_SET_STANDBY marked as not supported in the CDF: Automatic PASS(SKIP)</li> </ul>	-

2. (Optional) Review the list of tests for each category. If you wish to skip some of the tests. You can skip tests by clicking on the Check mark on the right side of the **Test Options / Preview** panel.

The screen shot below shows some of the tests that have been skipped (highlighted in yellow with a red X).

Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Sink CT 2.0 🛛	
🖄 CDF Entry 🖌 Test Selection 🕨 Test Options / Preview	
Test List	
All 🖌 🗶 Instrument: My830 (192 163 254 163)	xecute Tests
Category / Test Name	¥ _
4 2.2.5: EDID Test and Device Capability / Device Status Register Test	
▷ 🛃 4.2.5.1: EDID Test	×
4.2.5.2: Device Capability Register Test	V
E 4.2.5.3: Device Status Registers Test	×
A.2.8: 3D Video Test	
•     •     •     •     •     •       •     •     •     •     •     •     •	× 🗸
4.2.9: UCP Sub-Command Tests	<b>_</b>
4.2.3.1: 0CP Sub-commands Receiving Test	
A 2.9 Star Sub-Commander Encademitting most	
Iter 01: Test all supported Commands	
A 2 2: Tink Taran Ploatnigal: Abgalute Maximum Voltages	·
4.3.3.1: Compon Test Environment.	$\checkmark$
4.3.3.2: CBE-Sink: VBUS Absolute Maximum Positive Voltage	×
4.3.3.3: CBE-Sink: CBUS Absolute Maximum Positive Voltage	V
4.3.6: Link Laver Electrical - DUT Output: Arbitration/Sync/Data Signaling	
A.3.6.1: CBE-Sink: Post-Discovery Passive Pull-down Z[CBUS SINK ON] Resistance	$\checkmark$
E 4.3.6.2: CBE-Sink: CBUS Capacitance	$\checkmark$
🔺 🖹 4.3.6.3: CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage	×
💥 Iter 01:	×
> 🛃 4.3.6.4: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage	$\checkmark$
4 - 4.3.8: Link Laver Timing - DUT Output: Arbitration/Sync/Data in Bit Times	
Isotropy 1.3.8.2: CBT-Sink: Bit Timing Variation within a Packet	$\checkmark$
4 4.3.11: Link Layer Timing - DUT Ouput: Bus Re-Arbitration	
E 4.3.11.4: CBT-Sink: Sink Never Sends Too Many Back-to-Back Packets	<b>V</b>
4 4.3.12: Link Laver Timing - DUT Output: Ill-formed packets	
• 4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise	×
<pre>&gt; [] 4.3.12.2: CBT-SINK: SINK Never Sends Partial Packets</pre>	V
4 5.14: LINK Layer Timing - DUT Input: Discovery OK 4 3 14 1: CPE-Sink: Walid Wake Dulse Timing	
$V \equiv 4.3.14.1$ . OBI-SINK, Valid Wake Fulse fiming	
4 4 3 14 3: CBT-Sink: Sink in Standby Discovers on Wake plus Discovery Dulse Secure	
a The of DDO CEM CENTRY	<u> </u>
4.3.6.3: CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage	

3. Click on the Execute Tests activation button to initiate the test suite. You will be prompted for a name for the tests. This dialog box is shown below.

CBUS Sink CT Results	Start Service	and the second s	
	🖪 Test Res	ults Name	
Execute CBUS Sink C	ompliance Tests on	Instrument: My980 @ 1	192.168.254.135
	Enter a name for	the Test Results.	
MyCBUS_Sink_Test1			
[	🔀 Cancel	🕝 Ok	

A screen will appear instructing you on how to connect your MHL CBUS sink device for testing. A sample screen is shown below:

CBUS Sink Compliance Test (1.2): "M	lyCBUS_Sink_Test2"			(a. 8. 8)
		Test List		
🗸 🖌 🖓 All 🕅 🖓 Reset	t Status			
Category / Test Name	me		V	Status 🔺
▶ 4.2.5: EDID 1	Test and Device Capa	bility Register Test		
4.2.5.1: EDI	ID Test			In Progress
🔶 Iter 01:			$\checkmark$	In Progress
■ 4.2.5.2: Dev	vice Capability Registe	er Test		Not Tested
▶ 4.3.3: Link 1	Laver Electrical: Ab	solute Maximum Voltages		
4.3.3.1: Com	mon Test Environment	te and assume the and deducers. The Data set		Not Tested
4.3.3.2: CBE	Sink: VBUS Absolute I	Maximum Positive Voltage	2	Not Tested
	-SINK: CBOS Absolute	Test Setup		Not lested
4.3.4: LINK	Sink: Powered-Off Z			Not Tested
• Iter 01: PRO	C SET STANDBY marked as not	Test 4.2.5.1, Iter-01	×	Not Tested
▶ 4.3.5: Link I	Laver Timing - DUT C	Verify that the DUT EDID is accessible and accurate.		
4.3.5.1: CBT	-Sink: Time from Sink		s HIGH-2	Not Tested
4.3.6: Link 1	Laver Electrical - D	Connect the input of the Sink DUT to the MHL output of the Test Instrument	ng	
🗏 4.3.6.1: CBE	E-Sink: Post-Discovery	as shown in the diagram below.		Not Tested
4.3.6.2: CBE	S-Sink: CBUS Capacitan	Apply power to the Sink DUT.		Not Tested
4.3.6.3: CBE	Sink: Arbitrate/Sync	Use the procedure specified below to put the Sink into an active state.		Not Tested
4.3.6.4: CBE	S-Sink: Arbitrate/Sync			Not Tested
▶ 4.3.7: Link 1	Laver Timing - DUT C	<procedure cdf="" in="" not="" specified="" the=""></procedure>	nds	N 1 m 1 1
4.3.7.1: CBT	-Sink: Arbitration/Sy			Not Tested
4.3.7.2: CB1	-Sink: Arbitration/sy		-	Not Tested
4.3.8: Link I	Laver Timing - DOT C	Cancel Compliance Test	S	
		Continue		
Line	Message			
• 0001	Compliance Test Start	ed.		
• 0002				
• 0003	Assembling the test li	st.		
• 0004	Transferring the CDF t	o the Test Instrument.		
• 0005	Test 4.2.5.1-01			
		Cancel the Compliance Test     Pause Test Execution		
E.				

During the test, the test results are shown under the Status column. There is a progress arrow which points to the test that is currently being run. The lower panel **Test Log** shows the testing activity as it occurs. Refer to the screen examples below.

	(1.2): Wycbo3_Sirk_1655		
	Test List		
🗸 All 🗶 All 🛛	Reset Status		
Category / Te	st Name	×	Status
4 > 4 2 5 · FT	TD Test and Device Canability Pegister Test		
⊿ 🗏 4.2.5.2	Device Capability Register Test		Fail
) 🕞 Iter 01	1	✓	Fail
4 ▶ 4.3.3: Li	ink Laver Electrical: Absolute Maximum Voltages		
Þ 📃 4.3.3.1	: Common Test Environment		Pass
▶ 📑 4.3.3.2	: CBE-Sink: VBUS Absolute Maximum Positive Voltage		Pass
▶ 📃 4.3.3.3	: CBE-Sink: CBUS Absolute Maximum Positive Voltage		Pass
• 🕨 4.3.5: Li	ink Layer Timing - DUT Output: Pre-Discovery		
4.3.5.1	: CBT-Sink: Time from Sink-side MHL Cable Detect until	Sink CBUS Leaves H1	Incomplete
💢 Iter 01	;	×	User Skipped
▶ 4.3.6: Li	ink Layer Electrical - DUT Output: Arbitration/Syn	c/Data Signaling	T
4 📑 4.3.6.1	CBE-SINK: Post-Discovery Passive Pull-down Z[CBUS SIN	K ONJ Resistance	Incomplete
	: CBE-Sink: CBUS Canaditance	~	The Progress
4.3.0.2	. CBE-SINK: CBOS Capacitance		In Progress
	CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage	· · · ·	Not Tested
4 4.3.6.4	: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage		Incomplete
X Iter 01	:	×	User Skipped
• ▶ 4.3.8: Tri	ink Laver Timing - DUT Output: Arbitration/Sync/Da	ta in Bit Times	
▶ 📑 4.3.8.1	CBT-Sink: Arb, Sync, Data HIGH and LOW Timing		Not Tested
▶ 🖪 4.3.8.2	: CBT-Sink: Bit Timing Variation within a Pack		Pass
4 🕨 4.3.9: Li	ink Layer Timing - DUT Output: Link Level CK		
Þ 📑 4.3.9.1	: CBT-Sink: Response to Link Level NACK		Not Tested
	Testion		
ine	Messarre		
0005	Configuration Changes INTAIONN > SINT ACTIVE		
0007	Everyting the test		
0008	Patrieving test results		
0000	Processing test results.		
0010	Frocessing test less		
0011	Test $4, 2, 5, 2$ Tter $01 \rightarrow Fail$		
0012	Test 4 3 6 2-01		
0013	Executing the test		
	Executing the test.		
	Cancel the Compliance Test	Test Execution	

You can view the details of failures or passes when they occur by exposing the navigation arrows on the left. Examples are shown on the following screen.

VAN       XAN       RestSatus            • Category / Test Name           • Sa.2.6: EDID and Device Capability Register Test           • Sa.2.6.1: EDID Reading Test             • If a.2.6.1: EDID Reading Test           • If a.2.6.1: EDID Reading Test           • If a.2.6.2: Device Capability Registers Test             • If a.2.6.2: Device Capability Registers Test           • If a.2.6.1: EDID Reading Test           • If a.2.6.2: Device Capability Registers Test             • If a.3.3.4: Link Laver Timing - DUT Output: Pre-Discovery           • Sa.3.4: If CBF-Source: Time from Source VBUS Application to Discovery Pulses             • Discovery pulses detected after 2010 ms               • Discovery pulses detected           • Sa.3.3: CBUS and VBUS within Absolute Maximum voltages during entire test             • Discovery pulses detected           • Sa.3.3: CBUS and VBUS within Absolute Maximum voltages during entire test             • Sa.3.3: CBUS and VBUS within Absolute Maximum voltages during entire test           • Sa.3.3: CBUS and VBUS within Absolute Maximum voltages during entire test             • Sa.3.3: CBUS and VBUS within Absolute Maximum voltages during entire test           • Sa.3.3: Link Laver Electrical - DUT Output: Discovery             • O1: DUT cnables VBUS           • O1: DUT cnables VBUS <th></th> <th></th> <th></th> <th>Test List</th>				Test List
<pre>Category / Test Name Category / Test Name Cate</pre>				V All X All Reset Status
<pre>&gt; 3.2.6: EDID and Device Capability Register Test</pre>	Status	<b>V</b>	×	Category / Test Name
<pre>     S.2.6.1: EDID Reading Test     Get ter 01:     S.2.6.2: Device Capability Registers Test     Get ter 01:     S.3.4: Link Layer Timing - DUT Output: Pre-Discovery     S.3.4.1: CBT-Source: Time from Source VBUS Application to Discovery Pulses     Get ter 01:     S.3.4.1: CBT-Source: Time from Source VBUS Application to Discovery Pulses     Get ter 01:     S.3.4.1: CBT-Source: Time from Source VBUS Application to Discovery Pulses     Get ter 01:     S.3.3.4: Discovery pulses detected after 2010 ms     S.3.3.5: Link Layer Timing back to back packets: 0 (good)     S.3.13.2: no bad packets from DUT detected     S.3.13.2: no bad packets from DUT detected     S.3.13.2: no bad packets from DUT detected     S.3.13.1: no narrow pulses detected     S.3.15.1: CBE-Source: Response to Initial Plug-In to MHL Device     S.3.5.5: Link Layer Electrical - DUT Output: Discovery     S.3.5.3: CBE-Source: Pre-Discovery Success Pull-up HIGH Voltage     Get ter 01:     S.3.9: Link Layer Timing - DUT Output: Arbitration/Svnc/Data in Bit Times     Test 6.3.18.1-01     Rescuting the test.     Retrieving test results.     Test 6.3.18.1 Iter 01 -&gt; Fail     Get 6.3.18.1 Iter 01 -&gt; Fail     Saving the test logs.     Test 6.3.18.1 Iter 01 -&gt; Fail     Saving the test logs.     Test 6.3.18.1 Iter 01 -&gt; Fail     Saving the test logs.     Test 6.3.18.1 Iter 01 -&gt; Fail     Saving the test logs.     Test 6.3.18.1 Iter 01 -&gt; Fail     Saving the test logs.     Test 6.3.18.1 Iter 01 -&gt; Fail     Saving the test logs.     Test 6.3.18.1 Iter 01 -&gt; Fail     Saving the test logs.     Test 6.3.18.1 Iter 01 -&gt; Fail     Saving the test logs.     Test 6.3.18.1 Iter 01 -&gt; Fail     Saving the test logs.     Test 6.3.18.1 Iter 01 -&gt; Fail     Saving the test logs.     Test 6.3.18.1 Iter 01 -&gt; Fail     Saving the test logs.     Test 6.3.18.1 Iter 01 -&gt; Fail     Saving the test logs.     Test 6.3.18.1 Iter 01 -&gt; Fail     Saving the test logs.     Test 6.3.18.1 Iter 01 -&gt; Fail     Saving the test logs.     Test 6.3.18.1 Iter 01 -&gt; Fail     Saving the test log</pre>				4 > 3.2.6: EDID and Device Capability Register Test
Iter 01:	Fail			3.2.6.1: EDID Reading Test
<pre>    </pre>	Fail	V	×	belief 01:
<pre>&gt; Iter 01: &gt; 3.3.4: Link Laver Timing - DUT Output: Pre-Discovery &gt; 3.3.4: Link Laver Timing - DUT Output: Pre-Discovery &gt; Discovery Pulses detected after 2010 ms &gt; Discovery pulses detected after 2010 ms &gt; Outmoods test results to follow &gt; 3.3.3: CBUS and VBUS within Absolute Maximum voltages during entire test &gt; 3.3.12.3: max incoming back to back packets: 0 (good) &gt; 3.3.13.1: no narrow pulses detected &gt; 3.3.12.3: max incoming back to back packets: 0 (good) &gt; 3.3.13.1: no narrow pulses detected &gt; 01: DUT enables VBUS &gt; 0 02: DUT drives CBUS HIGH Discovery pulses at proper time after VBUS enabled &gt; 3.3.5.1: CBE-Source: Response to Initial Plug-In to MHL Device &gt; 0 02: DUT drives CBUS HIGH Discovery Success Pull-up HIGH Voltage &gt; 0 01: DUT enables VBUS &gt; 0 02: DUT drives CBUS HIGH Discovery Success Pull-up HIGH Voltage &gt; 0 1ter 01: &gt; 3.3.9: Link Laver Timing - DUT Output: Arbitration/Svnc/Data in Bit Times Tetlog time Message 0 000  Test 6.3.18.1-01 - Securing the test. 0 011  Test 6.3.18.1-01  Test 6.3.18.1-01  Test 6.3.18.1-01  Test 6.3.18.1-01  Test 6.3.18.1-01  Test 6.3.18.2-01  Te</pre>	Fail			3.2.6.2: Device Capability Registers Test
3.3.4: Link Laver Timing - DUT Output: Pre-Discovery   3.3.4: Link Laver Timing - DUT Output: Pre-Discovery   3.3.4: CBT-Source: Time from Source VBUS Application to Discovery Pulses   • Discovery pulses detected after 2010 ms   • Continuous test results to follow   • 3.3.3: CBUS and VBUS within Absolute Maximum voltages during entire test   • 3.3.12: max incoming back to back packets: 0 (good)   • 3.3.12: mo bad packets from DUT detected   • 01: DUT enables VBUS   • 02: DUT drives CBUS HIGH Discovery pulses at proper time after VBUS enabled   • 3.3.5. 1: CBE-Source: Response to Initial Plug-in to MHL Device   • 02: DUT drives CBUS HIGH Discovery Success Pull-up HIGH Voltage   • 11: There 01:   • 3.3.9: Link Laver Timing - DUT Output: Arbitration/Svnc/Data in Bit Times        Test 6.3.18.1-01      Executing the test.      Retrieving test results.      Processing test results.      Suing test results.      Suing test results.      Suing test results.      Pulse test logs.       Pulse test logs.      Pulse test logs.       Pulse test.      Pulse test.      Pulse test logs.       Pulse test logs.       Pulse test logs.      Pulse test logs.       Pulse test.      Pulse test.      Pulse test.      Pulse test.       Pulse test logs.       Pulse test logs.       Pulse test logs.       Pulse test logs.       Pulse test.      Pulse test.      Pulse test.       Pulse test.       Pulse test.       Pulse test.       Pulse test logs.       Pulse test.      Pulse test.       Pulse test.	Fail	V	<b>V</b>	b 😝 Iter 01:
<pre>     [3.3.4.1: CBT-Source: Time from Source VBUS Application to Discovery Pulses</pre>				4 > 3.3.4: Link Layer Timing - DUT Output: Pre-Discovery
<pre>     Iter 01:     Discovery pulses detected after 2010 ms     Discovery pulses detected after 2010 ms     Continuous test results to follow     3.3.3: CBUS and VBUS within Absolute Maximum voltages during entire test     3.3.12.3: max incoming back to back packets: 0 (good)     3.3.13.1: no narrow pulses detected     3.3.13.1: no harrow pulses detected     3.3.13.2: no bad packets from DUT detected     3.3.13.2: no bad packets from DUT detected     3.3.5.1: CBE-Source: Response to Initial Plug-in to MHL Device     02: DUT drives CBUS HIGH Discovery pulses at proper time after VBUS enabled     3.3.5.1: CBE-Source: Response to Initial Plug-in to MHL Device     Ter 01:     3.3.5.3: CBE-Source: Pre-Discovery Success Pull-up HIGH Voltage     Test 0:     Test 6.3.12.5 Iter 01 -&gt; Fail     fet 01:     Test 6.3.18.1-01     Executing the test.     Retrieving test results.     Saving the test logs.     Test 6.3.18.1 Iter 01 -&gt; Fail     Forcessing test results.     Saving the test logs.     Test 6.3.18.1 Iter 01 -&gt; Fail     Test 6.3.18.2-01     Executing the test.     Saving the test logs.     Test 6.3.18.2-01     Executing the test.     Saving the test logs.     Test 6.3.18.2-01     Executing the test.     Saving the test logs.     Test 6.3.18.2-01     Executing the test.     Saving the test logs.     Test 6.3.18.2-01     Executing the test.     Saving the test logs.     Test 6.3.18.2-01     Executing the test.     Saving the test logs.     Test 6.3.18.2-01     Executing the test.     Saving the test logs.     Test 6.3.18.2-01     Executing the test.     Saving the test logs.     Test 6.3.18.2-01     Executing the test.     Saving the test logs.     Test 6.3.18.2-01     Executing the test.     Saving the test logs.     Test 6.3.18.2-01     Executing the test.     Saving the test logs.     Test 6.3.18.2-01     Executing the test.     Saving the test logs.     Test 6.3.18.2-01     Executing the test.     Saving the test logs.     Test 6.3.18.2-01     Executing the test.     Saving the test logs.     Test 6.3.18.2-01</pre>	Fail		ses	▲ 🗏 3.3.4.1: CBT-Source: Time from Source VBUS Application to Discovery Pulses
<ul> <li>Discovery pulses detected after 2010 ms</li> <li>Orntinuous test results to follow</li> <li>3.3.31 CBUS and VBUS within Absolute Maximum voltages during entire test</li> <li>3.3.12.3: max incoming back to back packets: 0 (good)</li> <li>3.3.13.1: no narrow pulses detected</li> <li>3.3.13.1: no harrow pulses detected</li> <li>3.3.13.2: no bad packets from DUT detected</li> <li>0.2: DUT enables VBUS</li> <li>0.2: DUT drives CBUS HIGH Discovery pulses at proper time after VBUS enabled</li> <li>3.3.5.1: CBE-Source: Response to Initial Plug-in to MHL Device</li> <li>3.3.5.3: CBE-Source: Pre-Discovery Success Pull-up HIGH Voltage</li> <li>1.3.3.9: Link Laver Timing - DUT Output: Arbitration/Svnc/Data in Bit Times</li> </ul> Iter 01: Test 6.3.18.1-01 Executing the test. 6.011 Executing the test. 6.013 Forest 6.3.18.1 tter 01 -> Fail 6.014 5.014 5.014 5.015 5.014 5.015 7.025 5.014 7.025 5.014 7.025 5.016 7.025 7.021 7.0214 7.025 7.021 7.0214 7.021 7.025 7.021 7.0214 7.021 7.021 7.025 7.021 7.021 7.025 7.021 7.021 7.025 7.021 7.021 7.025 7.021 7.021 7.025 7.021 7.021 7.025 7.021 7.021 7.025 7.021 7.021 7.021 7.025 7.021 <p< td=""><td>Fail</td><td>V</td><td><b>V</b></td><td>a 😝 Iter 01:</td></p<>	Fail	V	<b>V</b>	a 😝 Iter 01:
<ul> <li>Continuous test results to follow</li> <li>3.3.3: GBUS and VBUS within Absolute Maximum voltages during entire test</li> <li>3.3.12.3: max incoming back to back packets: 0 (good)</li> <li>3.3.13.1: no narrow pulses detected</li> <li>3.3.13.2: no bad packets from DUT detected</li> <li>0 01: DUT enables VBUS</li> <li>0 02: DUT drives CBUS HIGH Discovery pulses at proper time after VBUS enabled</li> <li>3.3.5.1: CBE-Source: Response to Initial Plug-in to MHL Device</li> <li>0 1: DIT enables VBUS</li> <li>1 3.3.5.3: CBE-Source: Pre-Discovery Success Pull-up HIGH Voltage</li> <li>1 3.3.5.3: CBE-Source: Pre-Discovery Success Pull-up HIGH Voltage</li> <li>1 3.3.5.9: Link Laver Timing - DUT Output: Arbitration/Svnc/Data in Bit Times</li> </ul>				Discovery pulses detected after 2010 ms
<ul> <li>Continuous test results to follow</li> <li>3.3.3: CBUS and VBUS within Absolute Maximum voltage during entire test</li> <li>3.3.12.3: max incoming back to back packets: 0 (good)</li> <li>3.3.13.1: no narrow pulses detected</li> <li>3.3.13.2: no bad packets from DUT detected</li> <li>01: DUT drives CBUS HIGH Discovery pulses at proper time after VBUS enabled</li> <li>02: DUT drives CBUS HIGH Discovery pulses at proper time after VBUS enabled</li> <li>3.3.5.1: CBE-Source: Response to Initial Plug-in to MHL Device</li> <li>○ 1. EUT drives CBUS PUS</li> <li>○ 1. EUT drives CBUS HIGH Discovery Success Pull-up HIGH Voltage</li> <li>○ 1. EUT drives CBUS Pulley Success Pull-up HIGH Voltage</li> <li>○ 1. Eutog</li> </ul> Test 6.3.12.5 Iter 01 -> Fail <ul> <li>0109</li> <li>Test 6.3.18.1-01</li> <li>Executing the test.</li> <li>0114</li> <li>Saving the test logs.</li> <li>0115</li> <li>Test 6.3.18.1 ther 01 -&gt; Fail</li> <li>0116</li> <li> Test 6.3.18.1-01</li> <li>Executing the test.</li> <li>0116</li> <li> Test 6.3.18.1-01</li> <li>Executing the test.</li> <li>0116</li> <li> Test 6.3.18.2-01</li> <li>Executing the test.</li> </ul>				ø
<ul> <li>3.3.3: CBUS and VBUS within Absolute Maximum voltages during entire test</li> <li>3.3.12: max incoming back to back packets: 0 (good)</li> <li>3.3.13.1: no narrow pulses detected</li> <li>3.3.13.2: no bad packets from DUT detected</li> <li>3.3.13.2: no bad packets from DUT detected</li> <li>0.1: DUT enables VBUS</li> <li>0.2: DUT drives CBUS HIGH Discovery pulses at proper time after VBUS enabled</li> <li>3.3.5.1: CBE-Source: Response to Initial Plug-in to MHL Device</li> <li>3.3.5.3: CBE-Source: Pre-Discovery Success Pull-up HIGH Voltage</li> <li>3.3.9: Link Laver Timing - DUT Output: Arbitration/Svnc/Data in Bit Times</li> </ul>				• Continuous test results to follow
<ul> <li>3.3.12.3: max incoming back to back packets: 0 (good)</li> <li>3.3.13.1: no narrow pulses detected</li> <li>3.3.13.2: no bad packets from DUT detected</li> <li>0.1: DUT enables VBUS</li> <li>0.1: DUT enables VBUS</li> <li>0.1: DUT drives CBUS HIGH Discovery pulses at proper time after VBUS enabled</li> <li>3.3.5.1: CBE-Source: Response to Initial Plug-in to MHL Device</li> <li>3.3.5.3: CBE-Source: Pre-Discovery Success Pull-up HIGH Voltage</li> <li>3.3.5.3: CBE-Source: Pre-Discovery Success Pull-up HIGH Voltage</li> <li>3.3.5.3: CBE-Source: Pre-Discovery Success Pull-up HIGH Voltage</li> <li>3.3.9: Link Laver Timing - DUT Output: Arbitration/Svnc/Data in Bit Times</li> </ul>				<ul> <li>3.3.3: CBUS and VBUS within Absolute Maximum voltages during entire test</li> </ul>
<ul> <li>3.3.13.1: no narrow pulses detected</li> <li>3.3.13.2: no bad packets from DUT detected</li> <li>0.1: DUT enables VBUS</li> <li>0.2: DUT drives CBUS HIGH Discovery pulses at proper time after VBUS enabled</li> <li>3.3.5: Link Laver Electrical - DUT Output: Discovery</li> <li>3.3.5.1: CEE-Source: Response to Initial Plug-in to MHL Device</li> <li>Iter 01:</li> <li>3.3.5.3: CEE-Source: Pre-Discovery Success Pull-up HIGH Voltage</li> <li>Iter 01:</li> <li>3.3.9: Link Laver Timing - DUT Output: Arbitration/Svnc/Data in Bit Times</li> </ul>				<ul> <li>3.3.12.3: max incoming back to back packets: 0 (good)</li> </ul>
<ul> <li>3.3.13.2: no bad packets from DUT detected</li> <li></li></ul>				• 3.3.13.1: no narrow pulses detected
<pre>&gt; ● 01: DUT enables VEUS</pre>				• 3.3.13.2: no bad packets from DUT detected
▶ © 02: DUT drives CBUS HIGH Discovery pulses at proper time after VBUS enabled          3.3.5.1: CBE-Source: Response to Initial Plug-in to MHL Device         ▶ © Iter 01:         ③ 3.3.5.3: CBE-Source: Pre-Discovery Success Pull-up HIGH Voltage         ▶ ③ Iter 01:         ● Iter 01:         ● ③ Iter 01:         ● ○ Iter 01:         ● ○ Iter 01:         ● ○ Iter 01:         ● ○ Iter 01:	Fail			>> 😔 01: DUT enables VBUS
<pre>3.3.5: Link Laver Electrical - DUT Output: Discovery</pre>	Fail		enabled	✓ ▷
3.3.5.1: CEE-Source: Response to Initial Plug-in to MHL Device         Image: State of the				3.3.5: Link Laver Electrical - DUT Output: Discovery
↓ ↓ Iter 01:       ↓ ↓         ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓	Pass			3.3.5.1: CBE-Source: Response to Initial Plug-in to MHL Device
▲ 3.3.5.3: CBE-Source: Pre-Discovery Success Pull-up HIGH Voltage         ▶ Iter 01:         ▲ 3.3.9: Link Laver Timing - DUT Output: Arbitration/Svnc/Data in Bit Times         Tettog         Inter 01:         ▲ 3.3.9: Link Laver Timing - DUT Output: Arbitration/Svnc/Data in Bit Times         Tettog         Inter 01:         ▲ 4       Save         Tettog         ■ 0109       Test 6.3.18.1-01         ● 0110       Test 6.3.18.1-01         ● 0111       Executing the test.         ● 0112       Retrieving test results.         ● 0113       Processing test results.         ● 0114       Saving the test logs.         ● 0115       Test 6.3.18.1 Ther 01 -> Fail         ● 0116       Test 6.3.18.2-01         ● 0117       Executing the test.	Pass	V	V	▶   Iter 01:
▶ error       Iter 01:         ▶ 3.3.9: Link Laver Timing - DUT Output: Arbitration/Svnc/Data in Bit Times         Test 6.3.19.1         Iter 01 -> Fail         • 0109       Test 6.3.18.1-01         • 0110       Test 6.3.18.1-01         • 0111       Executing the test.         • 0112       Retrieving test results.         • 0113       Processing test results.         • 0114       Saving the test logs.         • 0115       Test 6.3.18.1 ther 01 -> Fail         • 0116       Test 6.3.18.2-01         • 0117       Executing the test.	Fail			A 3.3.5.3: CBE-Source: Pre-Discovery Success Pull-up HIGH Voltage
▲ ▶ 3.3.9: Link Laver Timing - DUT Output: Arbitration/Svnc/Data in Bit Times         Testlog         Line       Message         • 0109       Test 6.3.12.5 Iter 01 -> Fail         • 0110       Test 6.3.18.1-01         • 0111       Executing the test.         • 0112       Retrieving test results.         • 0113       Processing test results.         • 0114       Saving the test logs.         • 0115       Test 6.3.18.1 Tter 01 -> Fail         • 0116       Test 6.3.18.2-01         • 0117       Executing the test.	Fail	V	×	▷
Testlog           Line         Message           • 0109         Test 6.3.12.5 Iter 01 -> Fail           • 0110         Test 6.3.18.1-01           • 0110         Test 6.3.18.1-01           • 0111         Executing the test.           • 0112         Retrieving test results.           • 0113         Processing test results.           • 0114         Saving the test logs.           • 0115         Test 6.3.18.1 Iter 01 -> Fail           • 0116         Test 6.3.18.2-01           • 0117         Executing the test.			Times	3.3.9: Link Laver Timing - DUT Output: Arbitration/Svnc/Data in Bit Ti
Tetteg       Line     Message       0109     Test 6.3.12.5 Iter 01 $\rightarrow$ Fail       0110     Test 6.3.18.1-01       0111     Executing the test.       0112     Retrieving test results.       0113     Processing test results.       0114     Saving the test logs.       0115     Test 6.3.18.1 Iter 01 -> Fail       0116     Test 6.3.18.2-01       0117     Executing the test.				
Line         Message           • 0109         Test 6.3.12.5 Iter 01 -> Fail           • 0110         Test 6.3.18.1-01           • 0111         Executing the test.           • 0112         Retrieving test results.           • 0113         Processing test results.           • 0114         Saving the test logs.           • 0115         Test 6.3.18.1 Iter 01 -> Fail           • 0116         Test 6.3.18.2-01           • 0117         Executing the test.				Test Log
• 0109       Test 6.3.12.5 Iter 01 -> Fail         • 0110       Test 6.3.18.1-01         • 0111       Executing the test.         • 0112       Retrieving test results.         • 0113       Processing test results.         • 0114       Saving the test logs.         • 0115       Test 6.3.18.1 Iter 01 -> Fail         • 0116       Test 6.3.18.2-01         • 0117       Executing the test.				Line Message
• 0110       Test 6.3.18.1-01         • 0111       Executing the test.         • 0112       Retrieving test results.         • 0113       Processing test results.         • 0114       Saving the test logs.         • 0115       Test 6.3.18.1 Iter 01 -> Fail         • 0116       Test 6.3.18.2-01         • 0117       Executing the test.				• 0109 Test 6.3.12.5 Iter 01 -> Fail
• 0111       Executing the test.         • 0112       Retrieving test results.         • 0113       Processing test results.         • 0114       Saving the test logs.         • 0115       Test 6.3.18.1 Iter 01 -> Fail         • 0116       Test 6.3.18.2-01         • 0117       Executing the test.				• 0110 Test 6.3.18.1-01
0112Retrieving test results. $0113$ Processing test results. $0114$ Saving the test logs. $0115$ Test 6.3.18.1 Iter 01 -> Fail $0116$ Test 6.3.18.2-01 $0017$ Executing the test.				• 0111 Executing the test.
• 0113         Processing test results.           • 0114         Saving the test logs.           • 0115         Test 6.3.18.1 Iter 01 -> Fail           • 0116         Test 6.3.18.2-01           • 0117         Executing the test.				• 0112 Betrieving test results.
• 0114         Saving the test logs.           • 0115         Test 6.3.18.1 Iter 01 -> Fail           • 0116         Test 6.3.18.2-01           > 0117         Executing the test.				0113 Processing test results.
outs       Test $6.3.18.1$ Iter $01 \rightarrow$ Fail         outs       Test $6.3.18.2 - 01$ b0117       Executing the test.				
0116     Test 6.3.18.2-01       0117     Executing the test.				$ \begin{array}{c} \text{ outs} \\ \text{ for a 18 1 ter 01 } \text{ -> Fail} \\ \end{array} $
10117 Executing the test.				
And Executing the test.				Salla Example tost
				Directing the test.

The log will indicate when the tests have completed. You can cancel the compliance test or pause at any time. If you pause the test you can resume later at any time even if you exit the 980 Manager application. Refer to the following screen example.

Test list         Vall       X A"       Reset Status         Category / Test Name       Image: Status       Status         Image: Descent status       Image: Status       Image: Status       Status         Image: Descent status       Image: Status       Image: Status       Image: Status       Status         Image: Descent status       Image: Status       Image: Status       Image: Status       Image: Status       Image: Status         Image: Descent status       Image: Status <th image:="" st<="" th=""><th></th></th>	<th></th>	
Image: Status       Image: Status         Image: Status		
▶ Category / Test Name       ✓       Status         ▶ Iter 01:       ✓       Fail		
→ → Iter 01:       ✓       Fail         → ⊕ Iter 01:       ✓       Fail		
<pre></pre>		
▶ Iter 01: Fail Fail		
( ) 6 3 11, MCC - DUM Input, Ennoug and Exceptions		
- 6.3.11: MSC - DOT INDUC: EFFORS and Exceptions		
• 🗄 6.3.11.3: CBM: DUT Receives Data While No Command Outstanding Fail		
Fail		
A [] 6.3.11.5: CBM: DUT Receives (0x34) a NACK Packet While No Command Outstanding		
Pall		
• 0.3.12: MSC - DUT INDUT: Argument Timeouts		
No Ther Di		
A 5 3 12 3' CBM' DIF Receives (0x60) SET INT - Data Timeout		
▶ Iter 01:		
A 0.3,12,5: CBM: DUT Receives (0x6C) WRITE BURST - Offset Timeout		
Fail		
▲ ▶ 6.3.18: DDC - DUT Output; Normal Operation		
# 0.3.18.1: CBM-Source: DUT Issues DDC Short Read and Current Read         Fail		
👂 📔 Iter 01: 🛛 🖌 🖌 Fail	=	
A 🖪 6.3.18.2: CBM-Source: DUT Issues Regular DDC Read		
P G Iter 01:		
A 1 6.3.18.3: CBM-Source: DUT Issues DDC Segment Read Fail		
▶    Fail		
	•	
Test Log		
Line Message	<b>^</b>	
• 0120 Saving the test logs.		
• 0121 Test 6.3.18.2 Iter 01 -> Fail		
• 0122 Test 6.3.18.3-01		
• 0123 Executing the test.		
0124 Retrieving test results.		
• 0125 Processing test results.		
• 0126 Saving the test logs.		
• 0127 Test 6.3.18.3 Iter 01 -> Fail		
• 0128 Tests completed	*	
Close Window Continue Testing		

When the tests are completed the test window that shows the current activity will close. A new tab and panel will appear next to the **CBUS Sink CT 1.2** tab called the **CT Results** tab. You can view the test results in this panel. Refer to the following screen shots to see examples of the **CT Results** panel.

🔠 Event Plot 🔤 Edid Editor 🔯 EDID CT 1.4a 🔯 CBUS Src CT 1.2 🔯 CBUS Sink CT 1.2 📑 CT Results 🛛		
CBUS Sink Compliance Test Results	•	
Results Name: MyCBUS_Sink_Test2 Manufacturer: Acme		HTML Report
Date Tested: September 14, 2012 12:01 PM Model Name: XYZ		
Overall Status: CTS 1.2 - Canceled Port Tested: 1		
Test Results		
Test Name / Details	0	Status ^
4.2.5.1: EDID Test		Fail
4.2.5.2: Device Capability Register Test		Fail
4.3.3.1: Common Test Environment		Pass =
🖪 4.3.3.2: CBE-Sink: VBUS Absolute Maximum Positive Voltaç		Pass
4.3.3.3: CBE-Sink: CBUS Absolute Maximum Positive Volta		Pass
4.3.4.1: CBE-Sink: Powered-Off Z[CBUS SINK DISCOVER]		Skipped
4.3.5.1: CBT-Sink: Time from Sink-side MHL Cable Detect		Skipped
4.3.6.1: CBE-Sink: Post-Discovery Passive Pull-down Z[CF		Fail
4.3.6.2: CBE-Sink: CBUS Capacitance		Fail
4.3.6.3: CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage		Fail
4.3.6.4: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltac		Fail
4.3.7.1: CBT-Sink: Arbitration/Sync/Data Active Drive H		Fail
4.3.7.2: CBT-Sink: Arbitration/Sync/Data Edge Rate		Fail
4.3.8.1: CBT-Sink: Arb, Sync, Data HIGH and LOW Timing		Fail
4.3.8.2: CBT-Sink: Bit Timing Variation within a Packet		Pass
4.3.9.1: CBT-Sink: Response to Link Level NACK		Fail
4.3.10.1: CBT-Sink: ACK Output Timing in Nanoseconds		Fail
4.3.10.2: CBT-Sink: ACK Drive HIGH Duration		Fail
4.3.11.1: CBT-Sink: Sink uses Case 2 Regular Arbitration		Fall
4.3.11.2: CBT-Sink: Sink Case 3 Long Re-arbitration when		Fall
4.3.11.3: CBT-Sink: Sink Uses Case 1 Back-to-Back Timing		Fall
4.3.11.4: CBT-Sink: Sink Never Sends Too Many Back-to-Ba		Pass
4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise		Pass
4.3.12.2: CBT-Sink: Sink Never Sends Partial Packets		Pass
4.3.13.1: CBE-Sink: Discovery Sensitivity to Input Volta		Pall
4.3.14.1: CBT-Sink: Valid Wake Pulse Timing		Pall
4.5.14.2: CBT-SINK: Valid Discovery Pulse Timing		Skinned
4.3.14.3: CBT-SINK: SINK IN Standby Discovers on wake pi		Skipped
W 4.5.15.1. OBT-SINK: FILSE DISCOVERY Pulse should be ight		rati
Instrument: My980 [192.168.254.135]		Continue Test Execution

When you have completed the test series you will have an opportunity to view the detailed data for a particular failure. Use the following procedures to view the details of a test.

#### To view the details of each test:

1. Expose the detailed results of a failure and highlight a failure. Refer to the screen example below.

🗄 Event Plot 🔤 Edid Editor 🔯 EDID CT 1.4a 🔞 CBUS Sink CT 1.2 🔞 CBUS Src CT 1.2 🔞 CBUS Dongle CT 1.2 📳 CT Results 🛛 📃 🗖					
CBUS Sink Compliance Test Results					
Results Name: MyCBUS_Sink_Test2 Manufacturer: Acme		HTML Report			
Date Tested: September 14, 2012 12:01 PM Model Name: XYZ					
Overall Status: CTS 1.2 - Canceled Port Tested: 1					
Test Results					
Test Name / Details	0	Status ^			
▶ 🗏 4.3.6.4: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage		Fail			
▶ 4.3.7.1: CBT-Sink: Arbitration/Sync/Data Active Drive HIGH Duration		Fail			
▶ 📑 4.3.7.2: CBT-Sink: Arbitration/Sync/Data Edge Rate		Fail			
▶ 📑 4.3.8.1: CBT-Sink: Arb, Sync, Data HIGH and LOW Timing		Fail			
B 4.3.8.2: CBT-Sink: Bit Timing Variation within a Packet		Pass			
▶ 📃 4.3.9.1: CBT-Sink: Response to Link Level NACK		Fail			
▶ 🛃 4.3.10.1: CBT-Sink: ACK Output Timing in Nanoseconds		Fail			
▶ 🛃 4.3.10.2: CBT-Sink: ACK Drive HIGH Duration		Fail			
4.3.11.1: CBT-Sink: Sink uses Case 2 Regular Arbitration after NACK		Fail			
4 🗄 4.3.11.2: CBT-Sink: Sink Case 3 Long Re-arbitration when it Gives up the Bus		Fail			
A 😝 Iter 01:		Fail			
<ul> <li>DUT failed to discover. Timed out after 13000 ms.</li> </ul>					
• timed out					
▲ ♥ 01: DUT does eventually send a data packet.		Fail			
UUT did not send a data packet in response to GET_STATE					
© 02: DUT does NOT do re-arbitration (after an ACR) sooner than TWAIT (expres		Pass			
A.3.11.3: CBT-Sink: Sink Uses Case 1 Back-to-Back Timing (No Re-arbitration)		Fall			
• 4.3.11.4: CBT-Sink: Sink Never Sends Too Many Back-to-Back Packets		Pass			
• 4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise		Pass			
• 4.3.12.2: CBT-Sink: Sink Never Sends Partial Packets		Pass			
A 4.3.13.1: CBE-Sink: Discovery Sensitivity to Input Voltages		Pall			
P 4.3.14.1: CBT-SINK: Valid Wake Pulse Timing		Fall			
P 4.3.14.2: CBT-SINK: Valid Discovery Pulse Timing 4 2.14.2: CBT Gink: Gink in Standby: Discovery on Wake plug Discovery Pulse Series		Skippod			
P 4.3.14.3. OBF-SINK. SINK IN SCALARY DISCOVERS ON WARE PUTS DISCOVERY PUTSE Sequences of the second se		Fail			
N = 4.3.15.2. CBT Sink. First Discovery Fulse should be Ignored		Fail			
N = 4 3 16 1. CBF Sink. Bast Discovery rules should be ignored		Fail			
1 3 17 1: CBT-Sink: Bend of Discovery to Early Source-side Arbitration		Fail			
• 4.3.17.2: CBT-Sink: Sink Loss Arbitration Collision Correctly		Fail -			
Instrument: My980 [192.168.254.135]	_ P	Continue Test Execution			

# 4.10 Accessing the test results through the navigator panel

You can view the results of the tests at any time after you run them through the 980 GUI Manager's **Navigator** panel. Use the following procedures to view the details of a test.

#### To access the test results:

1. Access the **Navigator** tab and select **Compliance**. Refer to the screen example below.



2. Double click on the Results file you wish to view. The results will appear in a CT Results window on the right. Refer to the screen example below.

Event Plot 🔤 Edid Editor 🥸 EDID CT 1.4a 🥸 CBUS Src CT 1.2 🥸 CBUS Sink	CT12 CT Results		
Results Name: MyCBUS_Sink_Test2 Date Tested: September 14, 2012 12:01 PM Overall Status: CTS 1.2 - Canceled	Manufacturer: Acme Model Name: Unknown Port Tested: 1		HTML Rep
	Test Results		
Test Name / Details		0	Status
4.2.5.1: EDID Test			Fail
4.2.5.2: Device Capability Register Test			Fail
4.3.3.1: Common Test Environment			Pass
4.3.3.2: CBE-Sink: VBUS Absolute Maximum	Positive Voltage		Pass
4.3.3.3: CBE-Sink: CBUS Absolute Maximum	Positive Voltage		Pass
4.3.4.1: CBE-Sink: Powered-Off Z[CBUS SIN	K DISCOVER]		Skipped
4.3.5.1: CBT-Sink: Time from Sink-side MB	HL Cable Detect until Sin		Skipped
4.3.6.1: CBE-Sink: Post-Discovery Passive	Pull-down Z[CBUS SINK O		Fail
4.3.6.2: CBE-Sink: CBUS Capacitance			Fail
4.3.6.3: CBE-Sink: Arbitrate/Sync/Data Dr	rive LOW Voltage		Fail
4.3.6.4: CBE-Sink: Arbitrate/Sync/Data Dr	rive HIGH Voltage		Fail
4.3.7.1: CBT-Sink: Arbitration/Sync/Data	Active Drive HIGH Durati		Fail
4.3.7.2: CBT-Sink: Arbitration/Sync/Data	Edge Rate		Fail
4.3.8.1: CBT-Sink: Arb, Sync, Data HIGH a	and LOW Timing	_	Fail
4.3.8.2: CBT-Sink: Bit Timing Variation v	vithin a Packet		Pass
4.3.9.1: CBT-Sink: Response to Link Level	NACK		Fail
4.3.10.1: CBT-Sink: ACK Output Timing in	Nanoseconds		Fail
4.3.10.2: CBT-Sink: ACK Drive HIGH Durati	lon		Fail
4.3.11.1: CBT-Sink: Sink uses Case 2 Regu	alar Arbitration after NA		Fail
4.3.11.2: CBT-Sink: Sink Case 3 Long Re-a	arbitration when it Gives		Fail
4.3.11.3: CBT-Sink: Sink Uses Case 1 Back	c-to-Back Timing (No Re-a		Fail
4.3.11.4: CBT-Sink: Sink Never Sends Too	Many Back-to-Back Packet		Pass
4.3.12.1: CBT-Sink: Sink Never Sends Impu	ilse Noise		Pass
4.3.12.2: CBT-Sink: Sink Never Sends Part	tial Packets		Pass
4.3.13.1: CBE-Sink: Discovery Sensitivity	to Input Voltages		Fail
4.3.14.1: CBT-Sink: Valid Wake Pulse Timi	ing		Fail
4.3.14.2: CBT-Sink: Valid Discovery Pulse	a Timing		Fail
4.3.14.3: CBT-Sink: Sink in Standby Disco	overs on Wake plus Discov		Skipped
4.3.15.1: CBT-Sink: First Discovery Pulse	e should be Ignored		Pail

# 4.11 Viewing the MHL Sink Compliance HTML test report

After you have completed the tests, an HTML Report activation button will appear in the upper right of the screen which enables you to access the html report of the test results. Use the following procedures to view the html test report.

#### To view the html test report:

1. Select the CT Results panel as shown below.

CBUS Sink Compliance Test Results		
sults Name: MyCBUS_Sink_Test2 Manufacturer: Acine		
Date Tested: September 14, 2012 12:01 PM Model Name: Unknown		· · · · ·
erall Status: CTS 1.2 - Canceled Port Tested: 1		
Test Results		
Test Name / Details	Q	Status
4.2.5.1: EDID Test		Fail
4.2.5.2: Device Capability Register Test		Fail
4.3.3.1: Common Test Environment		Pass
4.3.3.2: CBE-Sink: VBUS Absolute Maximum Positive Voltage		Pass
4.3.3.3: CBE-Sink: CBUS Absolute Maximum Positive Voltage		Pass
4.3.4.1: CBE-Sink: Powered-Off Z[CBUS SINK DISCOVER]		Skipped
4.3.5.1: CBT-Sink: Time from Sink-side MHL Cable Detect until	Sin	Skipped
4.3.6.1: CBE-Sink: Post-Discovery Passive Pull-down Z[CBUS SI	NK O	Fail
4.3.6.2: CBE-Sink: CBUS Capacitance		Fail
4.3.6.3: CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage		Fail
4.3.6.4: CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage		Fail
4.3.7.1: CBT-Sink: Arbitration/Sync/Data Active Drive HIGH Du	rati	Fail
4.3.7.2: CBT-Sink: Arbitration/Sync/Data Edge Rate		Fail
4.3.8.1: CBT-Sink: Arb, Sync, Data HIGH and LOW Timing		Fail
4.3.8.2: CBT-Sink: Bit Timing Variation within a Packet		Pass
4.3.9.1: CBT-Sink: Response to Link Level NACK		Fail
4.3.10.1: CBT-Sink: ACK Output Timing in Nanoseconds		Fail
4.3.10.2: CBT-Sink: ACK Drive HIGH Duration		Fail
🗄 4.3.11.1: CBT-Sink: Sink uses Case 2 Regular Arbitration afte	r NA	Fail
4.3.11.2: CBT-Sink: Sink Case 3 Long Re-arbitration when it G	ives	Fail
4.3.11.3: CBT-Sink: Sink Uses Case 1 Back-to-Back Timing (No	Re-a	Fail
4.3.11.4: CBT-Sink: Sink Never Sends Too Many Back-to-Back Pa	cket	Pass
4.3.12.1: CBT-Sink: Sink Never Sends Impulse Noise		Pass
4.3.12.2: CBT-Sink: Sink Never Sends Partial Packets		Pass
4.3.13.1: CBE-Sink: Discovery Sensitivity to Input Voltages		Fail
4.3.14.1: CBT-Sink: Valid Wake Pulse Timing		Fail
4.3.14.2: CBT-Sink: Valid Discovery Pulse Timing		Fail
4.3.14.3: CBT-Sink: Sink in Standby Discovers on Wake plus Di	scov	Skipped
4.3.15.1: CBT-Sink: First Discovery Pulse should be Ignored	5	Pail

2. Click on the HTML Report activation button.

A dialog box will appear asking if you want a summary of the test results or a version that includes the CDF. This dialog box is shown in the screen shot below.

Generate Report				
🗟 HTML Report				
MyCBUS_Sink_Test2				
Select the desired report options.				
Show Test Summary Only.				
Include CDF Information.				
🗙 Cancel				

Specify if you want to see a summary report and if you want to see the CDF. If you leave Show Test Summary Only unchecked the application will produce a full detailed report. The following screens provide samples of the report.

Note: This example shows an MHL 1.2 test result; MHL 2.0 test results are similar in content and structure.

HTML Vie	ewer					
	C:\Use	rs\nkendall\Desktop\980_CBUS_GUI\980mgr\cbussinkct\results\MyCBUS_Sink_	Test2\Report_Summary_Co	lf.htm		
Repor	t generated on: September 17, 2012 5:05 PM				www.quantumda	ata.com
		<u>Quantum Data</u>				=
		CBUS Sink Compliance Test	t Report			
	0101.2					
	Results Name:	MvCBUS Sink Test2	Manuf	acturer:	Samsung	1
	Date Tested:	September 14, 2012 12:01 PM	Model	l Name:	Unknown	
	Overall Status:	Canceled	Port	Tested:	-	
						L
		Capabilities Declaration Form (CD	F)			
		General				
	CDF_MFR_NAME				Samsung	
	CDF_MODEL_NUMBER			τ	Unknown	
	CDF_SINK_CBUS_THRES	HOLD_V			0.78	
	CDF_SINK_CABLE_DETE	CT_TO_R_DISCOVER			60	
	CDF_PROC_SET_ACTIVE			No	ot Specified	
	CDF_PROC_SET_STAND	3Y		No	t Supported	1
	CDF_RCP_RECEIVE				YES	1
	CDF_RCP_SEND				YES	1
	CDF_LOG_DEV_MAP_CHANGE				NO	1
	Capability Registers					
	CDF_CR_MHL_VER_MAJOR				1	1
	CDF_CR_MHL_VER_MINOR				1	]
	CDF_CR_DEV_TYPE				1	1
	CDF_CR_POW				1	1
	CDF_CR_ADOPTER_ID_H	1			0	]
	CDE CP ADOPTEP ID I					1 -
			Sack Sack	Forward	📙 Save As  💥	Close

The CDF is shown below:

HTML Viewer		
C:\Users\nkendall\Desktop\980_CBUS_GUI\980mgr\cbussinkct\results\MyCBUS_Sink_Test2\Report_Summary_Cdf.htn	n	
Test 4.2.5.1	Fail	I [
Test 4.2.5.2 Device Capability Register Test	Fail	
Test 4.3.3.1 Common Test Environment	Pass	
Test 4.3.3.2 CBE-Sink: VBUS Absolute Maximum Positive Voltage	Pass	
Test 4.3.3.3 CBE-Sink: CBUS Absolute Maximum Positive Voltage	Pass	
Test 4.3.4.1 CBE-Sink: Powered-Off Z[CBUS_SINK_DISCOVER]	Skipped	
Test 4.3.5.1 CBT-Sink: Time from Sink-side MHL Cable Detect until Sink CBUS Leaves HIGH-Z	Skipped	
Test 4.3.6.1 CBE-Sink: Post-Discovery Passive Pull-down Z[CBUS_SINK_ON] Resistance	Fail	=
Test 4.3.6.2 CBE-Sink: CBUS Capacitance	Fail	
Test 4.3.6.3 CBE-Sink: Arbitrate/Sync/Data Drive LOW Voltage	Fail	
Test 4.3.6.4 CBE-Sink: Arbitrate/Sync/Data Drive HIGH Voltage	Fail	
Test 4.3.7.1 CBT-Sink: Arbitration/Sync/Data Active Drive HIGH Duration	Fail	
Test 4.3.7.2 CBT-Sink: Arbitration/Sync/Data Edge Rate	Fail	
Test 4.3.8.1 CBT-Sink: Arb, Sync, Data HIGH and LOW Timing	Fail	
Test 4.3.8.2 CBT-Sink: Bit Timing Variation within a Packet	Pass	
Test 4.3.9.1 CBT-Sink: Response to Link Level NACK	Fail	
Test 4.3.10.1 CBT-Sink: ACK Output Timing in Nanoseconds	Fail	-
🗢 Back 🌩 Fo	orward 🔡 Save	As 🔀 Close

The final page of the report shows the test equipment configuration as shown below.

Instrument           Name: My980           IF Address: 192.168.254.135           Net Mask: 255.255.255.0           Gateway IP: 192.168.254.1           Free Space: 121.08 GB of 144.22 GB (84.0%)           Version:           Advanced Test platform Release: 4.5.27           MHL CBUS Protocol Analyzer in slot 1:           Gateware: [Version: 0 Build Number: 4 (09:11:2012 121000) pcb: 23232323]           Firmware: [Version: 1.0.1 Build Number: 1978 (mblair 09:13:2012 09:21:52 CDT)]           System Information:           System SN : [ 47A7D6F8C0A385A0::N/A]           SN : [ 318383010000::11120010c]           Main Board : [ "PDF0TE"]
<pre>Name: My980 IP Address: 192.168.254.135 Net Mask: 255.255.255.0 Gateway IP: 192.168.254.1 Free Space: 121.08 GB of 144.22 GB (84.0%) Version: Advanced Test platform Release: 4.5.27 MHL CBUS Protocol Analyzer in slot 1: Gateware: [Version: 0 Build Number: 4 (09:11:2012 121000) pcb: 23232323] Firmware: [Version: 0 Build Number: 4 (09:11:2012 121000) pcb: 23232323] Firmware: [Version: 1.0.1 Build Number: 1978 (mblair 09:13:2012 09:21:52 CDT)] System Information: System SN : [ 47A7D6F8C0A385A0::N/A] SN : [ 318383010000::11120010c] Main Board : [ "DF67DE"]</pre>
<pre>IP Address: 192.168.254.135 Net Mask: 255.255.255.0 Gateway IP: 192.168.254.1 Free Space: 121.08 GB of 144.22 GB (84.0%) Version:     Advanced Test platform Release: 4.5.27     MHL CBUS Protocol Analyzer in slot 1:         Gateware: [Version: 0 Build Number: 4 (09:11:2012 121000) pcb: 23232323]         Firmware: [Version: 10.1 Build Number: 1978 (mblair 09:13:2012 09:21:52 CDT)]     System Information:         System SN : [ 47A7D6F8C0A385A0::N/A]         SN : [ 318383010000::11120010c]         Main Board : [ "DP67DE"]</pre>
<pre>Net Mask: 253:253:253:0 Gateway IP: 192.168:254.1 Free Space: 121.08 GB of 144.22 GB (84.0%) Version: Advanced Test platform Release: 4.5.27 MHL CBUS Protocol Analyzer in slot 1: Gateware: [Version: 0 Build Number: 4 (09:11:2012 121000) pcb: 23232323] Firmware: [Version: 0 Build Number: 1978 (mblair 09:13:2012 09:21:52 CDT)] System Information: System SN : [ 47A7D6F8C0A385A0::N/A] SN : [ 318383010000:11120010c] Main Board : [ "DF0TE"]</pre>
<pre>Free Space: 121.08 GB of 144.22 GB (84.0%) Version:</pre>
<pre>Version: Advanced Test platform Release: 4.5.27 MHL CBUS Protocol Analyzer in slot 1: Gateware: [Version: 0 Build Number: 4 (09:11:2012 121000) pcb: 23232323] Firmware: [Version: 1.0.1 Build Number: 1978 (mblair 09:13:2012 09:21:52 CDT)] System Information: System SN : [ 47A7D6F8COA385A0::N/A] SN : [ 318383010000::11120010c] Main Board : [ "DP67DE"]</pre>
<pre>MHL CBUS Protocol Analyzer in slot 1: Gateware: [Version: 0 Build Number: 4 (09:11:2012 121000) pcb: 23232323] Firmware: [Version: 1.0.1 Build Number: 1978 (mblair 09:13:2012 09:21:52 CDT)] System Information: System SN : [ 47A7D6F8COA385A0::N/A] SN : [ 318383010000::11120010c] Main Board : [ "DP67DE"]</pre>
Gateware: [Version: 0 Build Number: 4 (09:11:2012 121000) pcb: 23232323] Firmware: [Version: 1.0.1 Build Number: 1978 (mblair 09:13:2012 09:21:52 CDT)] System Information: System SN : [ 47A7D6F8C0A385A0::N/A] SN : [ 318383010000::11120010c] Main Board : [ "DF67DE"]
System Information: System SN : [ 47A7D6F8C0A385A0::N/A] SN : [ 318383010000::11120010c] Main Board : [ "DF67DE"]
System SN : [ 47A7D6F8C0A385A0::N/A] SN : [ 318383010000::11120010c] Main Board : [ "DF67DE"]
Main Board : [ "DP67DE"]
CPUx4 : [ 6.42.7 "Intel(R) Core(TM) i3-2100 CPU @ 3.10GHz"] DDR : [ 3 GB + 768 MB]
HD : [ WD1600BEVT-1]
OS : [ Linux xpscope-81 2.6.26-2-686 #1 SMP Wed Sep 21 04:35:47 UTC 2011 1686 GNU/Linux] GUI manager : [ Version 4.5.27 39005 201209061011]
1 : [ lo inet 127.0.0.178 scope host lo]
2 : [ etn0 inet 192.168.254.135/24 prd 192.168.254.255 scope global etn0] HDMI SINK CTS: [ 3.1.7]
HDMI SRC CTS: [3.1.8]
MHL SINK CTS: [ 1.2.0] MHL SRC CTS: [ 1.2.1]
Host
UI Name: Quantum Data 980 Manager - Version 4.5.29
UI Home: platform:/base/plugins/com.quantumdata.i980.app Java Vendor: Null
Java Runtime: 1.6.0_15-b03
Java Home: C:\Users\nkendall\Desktop\980_Release_5_29\980mgr\jre 05: win32
00. #1102
OS Arch: x86

# 4.12 CBUS Log Plot

The **CBUS Log Plot** panel (shown below) is panel used for viewing the bit and byte timing events of the CBUS controls and commands that occurred during a specific test. A **CBUS Log Plot** is provided for each source CBUS compliance test. The panel has both a graphical depiction of CBUS timing events and a sequential table list out of each event. The vertical axis shows the various CBUS event types. The **CBUS Log Plot** panel provides a set of CBUS event types labeled on the left that indicate the type of event. The horizontal axis is time.

The CBUS Log Plot is useful diagnosing CBUS compliance test failures.

The example below shows a series of events captured during a source test.

For more detailed information about the CBUS Log Plot, please refer to CBUS Log Plot.

# 5 MHL CBUS Dongle Compliance Tests

This chapter describes how to run the MHL CBUS dongle compliance tests. Please note you will have to purchase the optional 980 MHL CBUS Compliance Test module in order to run these tests.

The 980 MHL CBUS Compliance test module supports the test sections listed below in the MHL 1.2 and 2.0 Compliance Test specification. *Please note that some non-CBUS compliance tests are also covered by the 980 MHL CBUS Compliance Test module*.

## 5.1 System Test – Section 5.2

- 5.2.5.1 EDID Test
- 5.2.5.2 Device Capability Register Test
- 5.2.6 RCP Sub-command Tests
- 5.2.8.1 3D Video Mode Support Data (MHL 2.0)
- 5.2.9 UCP Sub-Commands Tests (MHL 2.0)

## 5.2 CBUS Tests – Section 5.3

- 5.3.1 CBUS Dongle DUT Common Test Equipment Setups
- 5.3.2 CBUS Dongle DUT Common Required Methodologies
- 5.3.3 Link Layer Electrical Dongle Absolute Maximum Voltages
- 5.3.4 Link Layer Electrical Dongle DUT Output: Standby Discovery Impedance
- 5.3.5 Link Layer Timing Dongle DUT Output: Pre-Discovery
- 5.3.6 Link Layer Electrical Dongle DUT Output: Arbitration/Sync/Data Signaling
- 5.3.7 Link Layer Timing Dongle DUT Output: Arbitration/Sync/Data in Nanoseconds
- 5.3.8 Link Layer Timing Dongle DUT Output: Arbitration/Sync/Data in Bit Times
- 5.3.9 Link Layer Timing Dongle DUT Output: Link Level NACK
- 5.3.10 Link Layer Timing Dongle DUT Output: Link Level ACK
- 5.3.11 Link Layer Timing Dongle DUT Output: Bus Re-Arbitration
- 5.3.12 Link Layer Timing Dongle DUT Output: Ill-formed packets
- 5.3.13 Link Layer Electrical Dongle DUT Input: Discovery
- 5.3.14 Link Layer Timing Dongle DUT Input: Discovery OK
- 5.3.15 Link Layer Timing Dongle DUT Input: Discovery Reject
- 5.3.16 Link Layer Electrical Sink DUT Input: Arbitration/Sync/Data Signaling
- 5.3.17 Link Layer Timing Sink DUT Input: Arbitration
- 5.3.18 Link Layer Timing Sink DUT Input: Data
- 5.3.19 Link Layer Timing Sink DUT Input: NACK
- 5.3.20 Link Layer Timing Dongle DUT Input: ACK
- 5.3.21 Link Layer Timing Dongle DUT Input: Bus Re-Arbitration
- 5.3.22 Link Layer Timing Sink DUT Input: Ill-formed Packets

- 5.3.23 Link Layer Timing Sink DUT Input: Disconnect
- 5.3.24 Link Layer Electrical Sink DUT VBUS Output
- 5.3.25 Link Layer Timing Sink DUT VBUS Turn On Transition

# 5.3 CBUS Common Tests – Section 6.3

- 6.3.1 MSC Source and Sink DUT Input: Device Register Space Contents; Reads
- 6.3.2 MSC Source and Sink DUT Output: NACK Packet Response to MSC\_MSG
- 6.3.3 MSC Source and Sink DUT Output: Never Initiates Bad Commands
- 6.3.5 MSC Source and Sink DUT Output: Errors and Exceptions
- 6.3.6 MSC Source and Sink DUT Input: Device Register Space Contents; Writes
- 6.3.7 MSC Source and Sink DUT Input: Vendor Specific and Reserved Header Values
- 6.3.8 MSC Source and Sink DUT Input: Device Register Space Contents; Writes
- 6.3.9 MSC Source and Sink DUT Input: Vendor-specific and Reserved Header Values
- 6.3.10 MSC Source and Sink DUT Input: Normal Commands
- 6.3.11 MSC Source and Sink DUT Input: Errors and Exceptions
- 6.3.12 MSC Source and Sink DUT Input: Argument Timeouts
- 6.3.15 MSC Sink DUT Output: Normal Commands
- 6.3.16 MSC Sink DUT Input: Errors and Exceptions
- 6.3.20 DDC Sink DUT Input; Continuous Monitors and Normal Operation
- 6.3.21 DDC Sink DUT Input; Normal Operation
- 6.3.22 DDC Sink DUT Input; Illegal Responses

# 5.4 Workflow for running the MHL CBUS Dongle Compliance Tests

The list below is the high level workflow for running the MHL CBUS Dongle Compliance Tests. Note that the installation of the external 980 GUI Manager and the Ethernet session are optional; you can run the compliance tests through the embedded GUI Manager.

1. Power up the 980. Refer to the procedures in Getting Started.

**Note**: The power switch in the front is used when you are turning off the 980 for a short period of time. For extended periods of off time, it is best to power the 980 down by first using the power button on the front and then the rocker switch on the back.

- 2. (Optional; only necessary if using the external 980 GUI Manager) Establish an Ethernet/IP connection between the external 980 GUI Manager and the 980.
- 3. Connect the MHL dongle device under test to the CBUS MHL Out (MHL micro USB) port on the 980 MHL CBUS Compliance Test module.
- 4. Complete a (or load an existing) Capabilities Declaration Form (CDF) for the device under test using the **CDF Entry** panel.
- 5. Select the tests that you wish to run from the **Test Selection** panel.
- 6. Initiate the tests through the Test Options / Review panel.
- 7. View the detailed data for test failures if failures occur.
- 8. View the results in the **Test Results** panel under the **Navigator** panel.

# 5.5 Making the physical MHL connections

This subsection describes the physical MHL connections required to run the MHL CBUS dongle compliance tests.



### To make the physical MHL connections:

This procedure assumes that you have assembled the 980 with the MHL CBUS Compliance Test module and the MHL dongle device under test and applied power to all these devices. Refer to the procedures below and the diagram above.

- 1. Connect your MHL dongle device under test to the top most OUT connector (MHL micro USB) on the 980 MHL CBUS Compliance Test module as shown in the figure above. Use the cable connected to the dongle.
- 2. Connect your HDMI sink device to the MHL dongle using a standard HDMI cable.

# 5.6 Completing the CDF

Use the following procedures to complete the CDF for the MHL CBUS dongle compliance tests.

**Note**: The workflow screen examples in this section show MHL 2.0 except where noted. MHL 1.2 workflow and screens are similar.

## To complete the CDF:

1. From the View menu, enable viewing of the MHL CBUS Dongle CT panel.

File Edid Instrument Options	Compliance View	Н	elp
🔳 Generator 🚺 ACA	HDMI 🕨	1	
Capture Control	MHL 🕨	1	Source Test
			Sink Test
			Dongle Test
🕨 🖾 L 🗙 🔍 🔄		1	CBUS Source Test
Name	Date / Tim	1	CBUS Sink Test
Capture		2	CBUS Dongle Test

2. Select the **CDF Entry** panel as shown below.

**Note**: A read status message will appear indicating if you have not completed all the essential fields. This is shown in the example below.

🗄 Event Plot 🖄 MHL Sink CT 2.0 🖄 CBUS Dongle CT 2.0 🖄 🔨	- 0)
1 CDF Entry  √ Test Selection    Test Options / Preview	
CDF File: < not saved>	
General @ Video @ Audio @ Registers @ RCP Roy @ RCP Send @ RCP ID Map @ UCP Roy (2.0) @ UCP Send (2.0) @ 3D Video (	20)
Manufacturer or Model field can not be blank.	
CTS Version to test against.	
○ 1.2 ◎ 2.0	
CDE MER NAME What is the product manufacturer's name?	
CDF_MODEL_NUMBER What is the model name/number of the product?	_
	-
Set Device into Active Mode for Discovery Tests.	
CDF_PROC_SET_ACTIVE Edit Procedure	
Set Device into Standby Mode for Discovery Tests.	
CDF_PROC_SET_STANDBY Standby Mode Supported? Edit Procedure	=
	-
CDF_HDCP_SUPPORT Is HDCP supported on this DUT?	
○ Yes ◎ No	-
CDF_DDC_SEGMENT_READ_SUPPORT	
Voltage at which CBUS Timing Measurements should be taken. This voltage should be balfway between the	-
CDF_D_CBUS_THRESHOLD_V HIGH and LOW CBUS voltages for data driven by this device. This will be related to the device's VOH.	
0.90 V (0.75 to 1.05)	
CDE D. MAX. CRUS. CAD. Specify the Dongle's maximum capacitance on CBUS.	
0.1 pF	
CDE D MAX STANDRY TO ACTIVE Maximum time from Wake Pulses until device leaves Standby Mode. Visible as Z[CBUS_SINK_DISCOVER].	
60 sec.	
CDE D. ACCEPTS POWER FROM SOURCE Does the Dongle accept VBUS power input from the Source?	-
Ves  No	
CDF D POWFRFD Does the DUT have its own power?	-

3. To create a new CDF, click on the **New** activation button.

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You will be prompted with a confirmation that you want to start a new CDF and reset the values. Click **OK** to proceed.



4. To open an existing CDF, click on the **Open** activation button.

You will be prompted with a dialog box that enables you to open a CDF. Select a CDF and then **OK** to proceed.

Note: You can save these CDFs to your PC for use on other PCs and by other colleagues.

S	ave CDF	
	🕲 CDF Name	
	Enter a name for the CDF	
	Acme_XYZ_MHL_CBUS_Dongle_CDF	
	<sup>™</sup> My980_Dongle <sup>™</sup> MySelect_Dongle <sup>™</sup> MySelect_Dongle_MB <sup>™</sup> MySelect_Dongle_MB2	
	Cancel Ck	

After you open an existing CDF or save it the name will appear beside the **Save** activation button as shown below:

Ē	🗄 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBU	JS Dongle CT 2.0 🕱				
Γ	🕲 CDF Entry 🗹 Test Selection 🕨 Te	est Options / Preview				
	CDF File: Acme_XYZ_MHL_CBUS_Dongle_CDF					
	General Video Audio	Registers   RCP Rcv  RCP Send  RCP LD Map  UCP Rcv (2.0)  UCP Send (2.0)  RCP	Video (2.0)			
		CTC Manufacture de deservaciones				
	CDE CTS VERSION	CTS Version to test against.				
		○ 1.2				

- 5. Complete the items in the **General** tab of the CDF Entry panel shown below. Note that you will have to complete the essential fields in order to proceed.
- 6. **Note**: A read status message will appear indicating if you have not completed all the essential fields. This is shown in the example below.

🖶 Event Plot 🔯 MHL Sink CT 2.0 🔯 CB	US Dongle CT 2.0 🛛 🗧	
🕲 CDF Entry 🧹 Test Selection 🕨 T	est Options / Preview	
🔄 Open 🔒 New 🔚 Save CDF Fi	le: <not saved=""></not>	
General O Video O Audio O	Registers  RCP Rcv RCP Send RCP LD Map UCP Rcv (2.0) UCP Send (2.0) RCP Send (2.0) RCP Send (2.0)	0
Manufacturer or Model field can not be	blank.	
	CTE Version to toot ensist	
CDF_CTS_VERSION		1
	0 1.2 0 2.0	
CDF_MFR_NAME	What is the product manufacturer's name?	
	What is the model name/number of the product?	
CDF_MODEL_NUMBER		
	Set Device into Active Mode for Discovery Tests.	
CDF_PROC_SET_ACTIVE	Edit Procedure	
	Set Device into Standby Mode for Discovery Tests.	
CDF_PROC_SET_STANDBY	Standby Mode Supported? Edit Procedure	=
CDF_HDCP_SUPPORT	© Yes © No	
	Can this device support DDC Segment Read?	
CDF_DDC_SEGMENT_READ_SUPPORT	⊙ Yes ⊚ No	
	Voltage at which CBUS Timing Measurements should be taken. This voltage should be halfway between the	
CDF_D_CBUS_THRESHOLD_V	0.90 V (0.75 to 1.05)	
	Specify the Dongle's maximum capacitance on CBUS.	
CDF_D_MAX_CBUS_CAP	0.1 pF	
	Maximum time from Wake Pulses until device leaves Standby Mode. Visible as Z[CBUS_SINK_DISCOVER].	
	60 sec.	
CDF D ACCEPTS POWER FROM SOURCE	Does the Dongle accept VBUS power input from the Source?	
	O Yes  No	
CDF D POWERED	Does the DUT have its own power?	-

When you have entered in all the required fields the error indication will go away as shown in the example below.

🔠 Event Plot 🔯 MHL Sink CT 2.0 🔯 CB	US Dongle CT 2.0 🕱 📃 🗖		
🕲 CDF Entry 🧹 Test Selection 🕨 T	est Options / Preview		
CDF File: Acme_XYZ_MHL_CBUS_Dongle_CDF			
● General ● Video ● Audio ●	Registers   RCP Rcv  RCP Send  RCP Send  RCP LD Map  UCP Rcv  (2.0)  RCP Send  C.0)  SD Video  (2.0)  RCP Send  C.0)  RCP Send  C.0)  RCP Send  RCP  RCP  RCP  RCP  RCP  RCP  RCP  RC		
CDF_CTS_VERSION	CTS Version to test against.		
CDF_MFR_NAME	What is the product manufacturer's name? Acme		
CDF_MODEL_NUMBER	What is the model name/number of the product?           XYZ		
CDF_PROC_SET_ACTIVE	Set Device into Active Mode for Discovery Tests. Edit Procedure		
CDF_PROC_SET_STANDBY	Set Dev into Standby Mode for Discovery Tests.		
CDF_HDCP_SUPPORT	Is HDCP supported on this DUT? © Yes  © No		
CDF_DDC_SEGMENT_READ_SUPPORT	Can this device support DDC Segment Read?  () Yes () No		
CDF_D_CBUS_THRESHOLD_V	Voltage at which CBUS Timing Measurements should be taken. This voltage should be halfway between the HIGH and LOW CBUS voltages for data driven by this device. This will be related to the device's VOH.         0.90       V (0.75 to 1.05)		
CDF_D_MAX_CBUS_CAP	Specify the Dongle's maximum capacitance on CBUS.           0.1         pF		
CDF_D_MAX_STANDBY_TO_ACTIVE	Maximum time from Wake Pulses until device leaves Standby Mode. Visible as Z[CBUS_SINK_DISCOVER].         60       sec.		
CDF_D_ACCEPTS_POWER_FROM_SOURCE	Does the Dongle accept VBUS power input from the Source? <ul> <li>Yes</li> <li>No</li> </ul>		
CDF D POWFRED	Does the DUT have its own power?		

You can enter helpful information using the "Edit Procedure" dialog box to instruct a test engineer how to put the device in the proper mode. The information entered into this dialog box will appear during the test.

## 7. Complete the items in the **Video** tab.

🖶 Event Plot 🔯 MHL Sink	CT 2.0 🔯 CBUS Dongle CT 2.0 🕱 🗧				
😢 CDF Entry 🗹 Test Selection 🕨 Test Options / Preview					
CDF File: Acme_XYZ_MHL_CBUS_Dongle_CDF					
General     Video	General     Video     Audio     Registers     RCP Rcv     RCP Send     RCP LD Map     UCP Rcv     (2.0)     UCP Send     (2.0)     O     JD Video     (2.0)				
CDF_VIDEO_RGB	CDF_VIDEO_RGB Over the DUT support RGB encoding?				
CDF_VIDEO_YCBCR_444	VIDEO_YCBCR_444 Does the DUT support YCBCR 4:4:4 encoding?				
CDF_VIDEO_YCBCR_422 Over the DUT support YCBCR 4:2:2 encoding? Over the DUT support YCBCR 4:2:2 encoding? Over the DUT support YCBCR 4:2:2 encoding?					
CDF VIDEO PACKEDPIXEL	CDE VIDEO PACKEDDIXEI Does the DUT support PackedPixel encoding?				
	O Yes 💿 No				
	Supported Normal Mode Video Formats				
CDF_VIDEO_VGA	Yes No (1) 640x480p(VGA) 59.94/60Hz				
CDF_VIDEO_480p_60					
CDF_VIDEO_720p_60					
CDF_VIDEO_1080i_60					
CDF_VIDEO_480i_60_2X					
CDF_VIDEO_480i_60_4X					
CDF_VIDEO_480p_60_2X	○ Yes				
CDF_VIDEO_576p_50					
CDF_VIDEO_720p_50					
CDF_VIDEO_1080i_50	⑦ Yes				
CDF_VIDEO_576i_50_2X					
CDF_VIDEO_576i_50_4X					
CDF_VIDEO_576p_50_2X	○ Yes				
CDF_VIDEO_1080p_24					
CDF_VIDEO_1080p_25					
CDF_VIDEO_1080p_30					
CDF_VIDEO_1080p_60					
CDF_VIDEO_1080p_50					

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## 8. Complete the items in the Audio tab.

🗄 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Dongle CT 2.0 🕴 🧧 🗖		
CDF Entry V Test Selection F Test Options / Preview		
CDF File: Acme_XYZ_MHL_CBUS_Dongle_CDF		
🔍 General 🔍 Video 🔍 A	Audio • Registers • RCP Rcv • RCP Send • RCP LD Map • UCP Rcv (2.0) • UCP Send (2.0) • 3D Video (2.0)	
	Linear PCM Audio Support	
CDF_AUDIO_2CH_S_Hz	Ø Yes ◎ No PCM 2Ch 32kHz Audio?	
CDF_AUDIO_2CH_44.1kHz	Yes      No PCM 2Ch 44.1kHz Audio?	
CDF_AUDIO_2CH_48kHz	Ø Yes ◎ No PCM 2Ch 48kHz Audio?	
CDF_AUDIO_2CH_88.2kHz	O Yes O No PCM 2Ch 88.2kHz Audio?	
CDF_AUDIO_2CH_96kHz	O Yes O No PCM 2Ch 96kHz Audio?	
CDF_AUDIO_2CH_176.4kHz	O Yes O No PCM 2Ch 176.4kHz Audio?	
CDF_AUDIO_2CH_192kHz	O Yes O No PCM 2Ch 192kHz Audio?	
CD5 AUDIO DCM Channels	Max supported Channel Count.	
CDF_AUDIO_PCIM_Channels	0 0 2 3 4 5 6 7 8	
	Maximum Freq for multi-channel audio (kHz)	
CDF_AUDIO_Max_Fs_Multi_Cn	© 32kHz ◎ 44.1kHz ◎ 48kHz ◎ 88.2kHz ◎ 96kHz ◎ 176.4kHz ◎ 192kHz	
Non-PCM Audio Support		
CDF_AUDIO_AC3	O Yes O No 2: AC-3 (Dolby Digital)	
CDF_AUDIO_MPEG1	○ Yes	
CDF_AUDIO_MP3	O Yes O No 4: MP3: MPEG1 Layer 3	
CDF_AUDIO_MPEG2	O Yes  No 5: MPEG2 (multichannel)	
CDF_AUDIO_AAC	© Yes ⊚ No 6: AAC	

## 9. Complete the items in the **Registers** tab.

🗄 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Dongle CT 2.0 🛛 🧧 🗖				
🔯 CDF Entry 🗹 Test Selection 🕨 Test Options / Preview				
CDF File: Acme_XYZ_MHL_CBUS_Dongle_CDF				
◎ General ◎ Video ◎	Audio 🔍 Registers 🔹 RCP	Rcv		
	Declare the expected value o	f each of the DUT's Capability Registers.		
CDF_CR_MHL_VER_MAJOR	Register: MHL_VERSION 1	Field: MHL_VER_MAJOR		
CDF_CR_MHL_VER_MINOR	Register: MHL_VERSION 0	Field: MHL_VER_MINOR		
CDF_CR_DEV_TYPE	Register: DEV_CAT Field: DEV	/_TYPE		
CDF_CR_ADOPTER_ID_H	Register: ADOPTER_ID_H	Field: ADOPTER_ID_H 00 - FF		
CDF_CR_ADOPTER_ID_L	Register: ADOPTER_ID_L 0	Field: ADOPTER_ID_L 00 - FF		
CDF_CR_DEVICE_ID_H	Register: DEVICE_ID_H	Field: DEVICE_ID_H 00 - FF		
CDF_CR_DEVICE_ID_L	Register: DEVICE_ID_L 0	Field: DEVICE_ID_L 00 - FF		
CDF_CR_BANDWIDTH	Register: BANDWIDTH 15	Field: BANDWIDTH 5.15		
CDF_CR_INT_SIZE	Register: INT_STAT_SIZE 4	Field: INT_SIZE 4.15		
CDF_CR_STAT_SIZE	Register: INT_STAT_SIZE 4	Field: STAT_SIZE 4.15		
CDF_CR_SP_SIZE	Register: SCRATCHPAD_SIZE 0	Field: SP_SIZE 0 or 1664		
CDF_CR_POW	Register: DEV_CAT Field: POV	N		

10. Complete the items in the RCP Rcv tab.

You can enter helpful information using the "Edit Procedure" dialog box. The information entered into this dialog box will help a test engineer determine if the device behaves properly when the various RCP commands are received.

🗄 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Dongle CT 2.0 🗵 🧧 🗖		
🔯 CDF Entry 🖌 Test Selection 🕨 Test Options / Preview		
CDF File: Acme_XYZ_MHL_CBUS_Dongle_CDF		
General     Video     Audio     Registers     RCP Rcv     RCP Send     RCP LD Map     UCP Rcv (2.0)     UCP Send (2.0)     O     JD Video (2.0)		
CDF_RCP_RECEIVE Does the DUT receive RCP? If yes, provide expected behavior for the supported RCP command below.		
	Select the RCP commands the DUT can receive. Specify the expected behavior for each supported command so that the Test Engineer can verify the correct behavior when each RCP command is received by the DUT.	
CDF_RCP_RCV_BEHAVIOR_00	0x00: Select () Required By: GUI Supported? Edit Behavior	
CDF_RCP_RCV_BEHAVIOR_01	0x01: Up () Required By: GUI Supported? Edit Behavior	
CDF_RCP_RCV_BEHAVIOR_02	0x02: Down (1) Required By: GUI Supported? Edit Behavior	
CDF_RCP_RCV_BEHAVIOR_03	0x03: Left Required By: GUI Supported? Edit Behavior	
CDF_RCP_RCV_BEHAVIOR_04	0x04: Right Required By: GUI Supported? Edit Behavior	
CDF_RCP_RCV_BEHAVIOR_05	0x05: Right-Up () Supported? Edit Behavior	

11. Complete the items in the **RCP Send** tab.

You can enter helpful information using the "**Edit Procedure**" dialog box. The information entered into this dialog box will appear during the test and can be helpful to instruct a test engineer on how to set up a device in order to run a particular test. In the example below you would enter in procedural information which a test engineer could use to cause the dongle to issue the various RCP commands.

掛 Event Plot 隧 MHL Sink CT 2.0	D 😢 CBUS Dongle CT 2.0 🛛 🗖 🗖		
😢 CDF Entry 🧹 Test Selection 🕨 Test Options / Preview			
CDF File: Acme_XYZ_MHL_CBUS_Dongle_CD			
General     Video     Audio     Registers     RCP Rcv     RCP Send     RCP LD Map     UCP Rcv     C2.0)     UCP Send     C2.0)     O     UCP Send     C2.0)			
CDF_RCP_SEND	Does the DUT send RCP?       ▲         If yes, provide procedures for each supported RCP command below.       ●         ● Yes       ● No		
	Select the RCP commands the DUT can send. Specify the procedure for each supported command so that the Test Engineer can force the DUT to output each RCP command,using these detailed steps and the DUT's user interface.		
	0x00: Select 🕕		
CDF_RCP_SEND_PROCEDURE_00	Supported? Edit Procedure		
	0x01: Up 🕦		
CDF_RCP_SEND_PROCEDURE_01	Supported? Edit Procedure		
	0x02: Down 🕕		
CDF_RCP_SEND_PROCEDURE_02	Supported? Edit Procedure		
	0x03: Left 🕕		
CDF_RCP_SEND_PROCEDURE_03	Supported? Edit Procedure		
	0x04: Right 🕕		
CDF_RCP_SEND_PROCEDURE_04	Supported? Edit Procedure		
	0x05: Right-Up 🕕		
CDF_RCP_SEND_PROCEDURE_05	Supported? Edit Procedure		
	0x06: Right-Down 🕕		
CDF_RCP_SEND_PROCEDURE_06	Supported? Edit Procedure		

12. Complete the items in the **RCP LD Map** tab.

You can enter helpful information using the "Edit Procedure" dialog box. The information entered into this dialog box will appear during the test to assist the test engineer. In the example below you would enter in procedural information which a test engineer could use to force the dongle into the proper mode for further testing of each logical device.

🗄 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Dongle CT 2.0 🛛 🗖 🗖		
🖄 CDF Entry 🖌 Test Selection 🕨 Test Options / Preview		
Open         New         Save         CDF File: Acme_XYZ_MHL_CBUS_Dongle_CDF		
General     Video     Audio     Registers     RCP Rcv     RCP Send     RCP LD Map     UCP Rcv (2.0)     UCP Send (2.0)     ST Video (2.0)		
CDF_LOG_DEV_MAP_CHANGE       Does the DUT support more than one setting in its LOG_DEV_MAP register?         If yes, provide procedures to change to each setting below.		
Add as many settings as the DUT supports using the "Add" button below. For each, define a procedure so that the Test Engineer can force the DUT into each of these modes for further testing of each Logical Device.		
Add Remove All		
CDF_PROC_LOG_DEV_MAP_1 VIDEO AUDIO MEDIA TUNER RECORD SPEAKER GUI		

13. Complete the items in the UCP Rcv tab.

You can enter helpful information using the "Edit Procedure" dialog box. The information entered into this dialog box will appear during the test to assist a test engineer. You can enter in the expected behavior for each supported command so that the test engineer can verify that the dongle DUT behaves properly when receiving the various UCP commands.

🗄 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Dongle CT 2.0 🛛 🗖 🗖		
😂 CDF Entry 🧹 Test Selection 🕨 Test Options / Preview		
CDF File: Acme_XYZ_MHL_CBUS_Dongle_CDF		
General     Video     Audio     Registers     RCP Rcv     RCP Send     RCP LD Map     UCP Rcv (2.0)     UCP Send (2.0)     O     SD Video (2.0)		
CDF_UCP_SEND_SUPPORT Does the DUT support sending UCP sub-commands?  Yes ONo		
CDF_UCP_SEND_APPLICATION     DUT UCP Application Instructions       Edit Procedure		
UCP Commands		
Add (# of Entries: 1)		
Command #01		
Hex Byte Data:		

14. Complete the items in the UCP Send tab.

You can enter helpful information using the "**Edit Procedure**" dialog box. The information entered into this dialog box will appear during the test and can be helpful to instruct a test engineer on how to set up a device in
order to run a particular test. In the example below you would enter in procedural information which a test engineer could use to cause the dongle to issue the various UCP commands.

🗄 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Sink CT 2.0 🕱 🗧 🗖					
CDF Entry 🗸 Test Selection 🕨 Test Options / Preview					
CDF File: Acme_XYZ_MHL_CBUS_Sink_CDF					
General     Video     Audio     Registers     RCP Rcv     RCP Send     RCP LD Map     UCP Rcv (2.0)     UCP Send (2.0)     O     3D Video (2.0)					
CDF_UCP_SEND_SUPPORT Does the DUT support sending UCP sub-commands?					
CDF_UCP_SEND_APPLICATION Edit Procedure					
UCP Commands					
Add (# of Entries: 1)					
<b>K</b> Command #01					
Hex Byte Data:					

15. Complete the items in the **3D Video** tab.

뒢 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS D	ongle CT 2.0 🕱				
🖄 CDF Entry 🧹 Test Selection 🕨 Test O	)ptions / Preview				
CDF File: Acme_XYZ_MHL_CBUS_Dongle_CDF					
General Video Audio Reg	isters	cv 🛛	RCP Send   RCP LD Map  UC	CP Rcv (2.0)    UCP Send (2.0)     JUCP Send (2.0)     UCP Send (2.0)	
CDE VIDEO 3D Does the DUT support 3D video?					
	🖲 Yes 🔘 No				
	Suppo	orted No	ormal Mode 3D Video Formats		
CDF_VIDEO_1280x720P_60_3D_Top_Bottom	🖲 Yes 🔘 No	(4)	1280x720p 59.94/60Hz,	3D, Top-Bottom	
CDF_VIDEO_1280x720P_50_3D_Top_Bottom	🖲 Yes 🔘 No	(19)	1280x720p 50Hz,	3D, Top-Bottom	
CDF_VIDEO_1920x1080p_24_Top_Bottom	🖲 Yes 🔘 No	(32)	1920x1080p 23.97/24Hz,	3D, Top-Bottom	
CDF_VIDEO_1920x1080i_60_3D_Left_Right	🔘 Yes 🔘 No	(5)	1920x1080i 59.94/60Hz,	3D, Left-Right	
CDF_VIDEO_1920x1080i_50_3D_Left_Right	🔘 Yes 🔘 No	(20)	1920x1080i 50Hz,	3D, Left-Right	
CDF_VIDEO_1280x720P_60_3D_Frame	🖲 Yes 🔘 No	(4)	1280x720p 59.94/60Hz,	3D, Frame-Sequential	
CDF_VIDEO_1280x720P_50_3D_Frame	🖲 Yes 🔘 No	(19)	1280x720p 50Hz,	3D, Frame-Sequential	
CDF_VIDEO_1920x1080p_24_Frame	🖲 Yes 🔘 No	(32)	1920x1080p 23.97/24Hz,	3D, Frame-Sequential	
	Support	ed Pixel	Packed Mode 3D Video Formats		
CDF_VIDEO_1280x720P_60_3D_Top_Bottom	🔘 Yes 🔘 No	(4)	1280x720p 59.94/60Hz,	3D, Top-Bottom	
CDF_VIDEO_1280x720P_50_3D_Top_Bottom	🔘 Yes 💿 No	(19)	1280x720p 50Hz,	3D, Top-Bottom	
CDF_VIDEO_1920x1080p_24_Top_Bottom	🔘 Yes 🔘 No	(32)	1920x1080p 23.97/24Hz,	3D, Top-Bottom	
CDF_VIDEO_1920x1080i_60_3D_Left_Right	🔘 Yes 🔘 No	(5)	1920x1080i 59.94/60Hz,	3D, Left-Right	
CDF_VIDEO_1920x1080i_50_3D_Left_Right	🔘 Yes 🔘 No	(20)	1920x1080i 50Hz,	3D, Left-Right	
CDF_VIDEO_1280x720P_60_3D_Frame	🔘 Yes 💿 No	(4)	1280x720p 59.94/60Hz,	3D, Frame-Sequential	
CDF_VIDEO_1280x720P_50_3D_Frame	🔘 Yes 💿 No	(19)	1280x720p 50Hz,	3D, Frame-Sequential	
CDF_VIDEO_1920x1080p_24_Frame	🔘 Yes 🔘 No	(32)	1920x1080p 23.97/24Hz,	3D, Frame-Sequential	

16. Save the CDF. If you have not already saved the CDF, you can do so with the **Save** activation button. Alternatively you can save the CDF under a different name.

Save CDF	
🖾 CDF Name	
Enter a name for the CDF	
Acme_XYZ_MHL_CBUS_Dongle_CDF	
The name already exists.	
SAcme_XYZ_MHL_CBUS_Dongle_CDF	
🔯 My980_Dongle	
<sup>™</sup> MySelect_Dongle	
₩ MySelect_Dongle_MB	
<sup>™</sup> MySelect_Dongle_MB2	
Cancel Ok	

## 5.7 Selecting which tests to run

Use the following procedures to select the tests to run. There are multiple tabs which correspond to each section in the CTS.

**Note**: The workflow screen examples in this section show MHL 2.0 except where noted. MHL 1.2 workflow and screens are similar.

#### To select the tests to run:

- 1. Select the **Test Selection** panel as shown below.
- 2. If you have an existing Test Selection option file saved you can recall that for use in your testing. Simply click on the **Open** activation button.

🗄 Event Plot 🥸 MHL Sink CT 2.0 🔯 CBUS Dongle CT 2.0 🗵	
CDF Entry V Test Selection > Test Options / Preview	
Copen Select All Tests Deselect All Tests	
▶ Dongle (6/40) ▶ Common (0/69) ▶ EDID (0/3) ▶ RCP (0/2) ▶ 3D (0/1) ▶ UCP (0/2)	

A dialog box will appear as follows. Simply select the file and click on the **OK** activation button.

**Note**: You can save the Test Selection files to your host PC and transfer them to other PCs and for others to use.

CBUS Sink Compliance Test	
Open Test Selection File	
Select an Test Selection file to open.	
MySelect1.xml MySelect_Sink.xml	
Cancel 📀 Ok	]

3. Complete the items in the **Sink** tab of the **Test Selection** panel shown below.

For convenience you can Select All or Deselect All tests using the activation buttons provided.

Check box indicators inform how many tests in each section and how many are selected. Each tab (Sink, Common or RCP) inform you of how many tests in that section have been selected.

Each test section list includes several tests. In the example shown below, the 5.3.17 Link Layer Timing – DUT Input: Arbitration Test section is selected and the specific tests in that section are then available to be selected.

**Note**: Some tests are run in background and cannot be deselected such as the 5.3.12. The background tests are highlighted in a light blue as shown in the example below.

Open	Save Select All Tests Deselect All Tests	
Dongle (6/40	Save Select All Tests Deselect All Tests	
Dongle (6/40		
E11 -	)) - Common (0/69) - EDID (0/3) - RCP (0/2) - 3D (0/1) - UCP (0/2)	
2.1.1	TMDS Electrical Tests	0/2
5.3.3	Link Layer Electrical: Absolute Maximum Voltages	3/3 🗖
5.3.4	Link Layer Electrical - DUT Output: Discovery Impedance	0/3
5.3.5	Link Layer Timing - DUT Output: Pre-Discovery	1/1
5.3.6	Link Layer Electrical - DUT Output: Arbitration/Sync/Data Signaling	0/4
5.3.7	Link Layer Timing - DUT Output: Arbitration/Sync/Data in Nanoseconds	0/2
5.3.8	Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit Times	1/2
5.3.9	Link Layer Timing - DUT Output: Link Level NACK	0/1
5.3.10	Link Layer Timing - DUT Output: Link Level NACK	2/2
5.3.11	Link Layer Timing - DUT Ouput: Bus Re-Arbitration	1/4
5.3.12	Link Layer Timing - DUT Output: III-formed packets	2/2 🗹
5.3.13	Link Layer Electrical - DUT Input: Discovery	0/1
5.3.14	Link Layer Timing - DUT Input: Discovery OK	0/3
5.3.15	Link Layer Timing - DUT Input: Discovery Reject	0/2
5.3.16	Link Layer Electrical - DUT Input: Arbitration/Sync/Data Signaling	0/1
5.3.17	Link Layer Timing - DUT Input: Arbitration	3/3 🖬
5.3.18	Link Layer Timing - DUT Input: Data	0/1
5.3.19	Link Layer Timing - DUT Input: NACK	0/1
5.3.20	Link Layer Timing - DUT Input: ACK	0/1
5.3.21	Link Layer Timing - DUT Input: Bus Re-Arbitration	0/1
5.3.22	Link Layer Timing - DUT Input: Ill-formed Packets	0/1
5.3.23	Link Layer Timing - DUT Input: Disconnect	0/3
5.3.24	Link Layer Electrical - DUT VBUS Output	0/1
5.3.25	Link Layer Electrical - DUT VBUS Input	0/1
5.3.26	Link Layer Timing - DUT VBUS Transition	0/1

4. Complete the items in the **Common** tab of the **Test Selection** panel shown below.

For convenience you can Select All or Deselect All tests using the activation buttons provided.

🖶 Event Plot 🐧	MHL Sink CT 2.0 🔯 CBUS Dongle CT 2.0 🛛		
🔯 CDF Entry	V Test Selection F Test Options / Preview		
Copen [	Save Select All Tests Deselect All Tests		
🕨 Dongle (6/	40)  Common (69/69) (3)  RCP (0/2)  SD (0/1)  UCP (0/2)		
▶ 6.3.1	MSC - DUT Input: Device Register Space Contents; Reads	1/1	
▶ 6.3.2	MSC - DUT Output: Vendor-specific and Reserved Header Values	1/1	
▶ 6.3.3	MSC - DUT Output: Normal Commands	7/7	
▶ 6.3.5	MSC - DUT Output: Never Initiates Bad Commands	8/8	
▶ 6.3.6	MSC - DUT Output: Errors and Exceptions	5/5	
▶ 6.3.7	MSC - DUT Output: Disconnect	1/1	
▶ 6.3.8	MSC - DUT Input: Device Register Space Contents; Writes	2/2	
▶ 6.3.9	MSC - DUT Input: Vendor-specific and Reserved Header Values	1/1	
▶ 6.3.10	MSC - DUT Input: Normal Commands	8/8	
▶ 6.3.11	MSC - DUT Input: Errors and Exceptions	23/23	
▶ 6.3.12	MSC - DUT Input: Argument Timeouts	9/9	
▶ 6.3.15	MSC - DUT Output: Normal Commands	2/2	
▶ 6.3.16	MSC - DUT Input: Errors and Exceptions	2/2	
▶ 6.3.20	DDC - DUT Input; Continuous Monitors and Normal Operation	2/2	
▶ 6.3.21	DDC - DUT Input; Normal Operation	5/5	
▶ 6.3.22	DDC - DUT Input; Illegal Responses	3/3	
<b>6.3</b> .1	10.1: CBM: DUT receives (0x62) GET_STATE Command		Â
Verify	that if DUT responds appropriately when it receives a GET_STATE. It should		
return	the value defined in the MHL Spec as the value stored in the DEV_STATE		
Capai	bility Register, which is always U.		
			E
⊻ 6.3.	LO.2: CBM: DUT receives (0x63) GET_VENDOR_ID Command		
Verity This t	that if DUT responds appropriately when it receives a GET_VENDOR_ID.		
0 63	10.3: CBM: DUT receives (0v61) DEAD DEVCAR Command		
Verify	that if DUT responds appropriately when it receives a READ DEVCAP.		
This t	est returns the values found in the CDF in section 2.3 (MHL Capability Registers).		
☑ 6.3.1	L0.4: CBM: DUT Receives (0x6B) GET MSC ERRORCODE Command (When No Error)		
Verify	that if DUT responds appropriately when it receives a MSC_ERRORCODE when		
no err	or has occurred.		
63	10.5: CBM: DUT Receives (0x6B) GFT MSC FRRORCODF Command (When Frror)		<b>•</b>

5. Complete the items in the EDID tab of the Test Selection panel shown below.

🗄 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Dongle CT 2.0 🛛	
CDF Entry V Test Selection > Test Options / Preview	
C Open Save Select All Tests Deselect All Tests	
▶ Dongle (6/40)         ▶ Common (69/69)         ▶ EDID (3/3)         ≥         2)         ▶ 3D (0/1)         ▶ UCP (0/2)	
✓ 5.2.5.1: EDID Test Verify that the DUT EDID is accessible and accurate.	
✓ 5.2.5.2: Device Capability Register Test Verify that the Device Capability Registers have accurate values.	
✓ 5.2.5.3: Device Status Registers Test Verify that the Device Status Registers have proper values.	
(CTS 2.0 Only)	

6. Complete the items in the **RCP** tab of the **Test Selection** panel shown below.

🗄 Event Plot 🥸 MHL Sink CT 2.0 🔯 CBUS Dongle CT 2.0 🕱				
CDF Entry ✓ Test Selection ► Test Options / Preview				
Copen Save Select All Tests Deselect All Tests				
▶ Dongle (6/40) ▶ Common (69/69) ▶ EDID (3/3) ▶ RCP (0/2) ▶ 3D (0/1) ▶ UCP (0/2)				
5.2.6.1: RCP Sub-Commands Receiving Test Verify that DUT responds properly to all incoming RCP sub-commands, according to the logical device type of types indicated in the CDF.				
5.2.6.2: RCP Sub-Commands Transmitting Test Verify that DUT transmits properly each required RCP sub-command, according to the logical device type of types indicated for the Dongle DUT in the CDF.				

7. Complete the items in the **3D** tab of the **Test Selection** panel shown below.

🗄 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Dongle CT 2.0 🛛	
CDF Entry V Test Selection > Test Options / Preview	
Copen Save Select All Tests Deselect All Tests	
▶ Dongle (6/40) ▶ Common (69/69) ▶ EDID (3/3) ▶ RCP (0/2) ▶ 3D (0/1) ▶ UCP (0/2)	
<ul> <li>5.2.8.1: 3D Video Mode Support Data         Verify that the DUT responds to 3D_REQ and sends the list of 3D video modes supported by the DUT.         (CTS 2.0 Only)         </li> </ul>	

8. Complete the items in the **UCP** tab of the **Test Selection** panel shown below.

🗄 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Dongle CT 2.0 🗵	- 0
CDF Entry V Test Selection > Test Options / Preview	
Copen Save Select All Tests Deselect All Tests	
▶ Dongle (6/40)         ▶ Common (69/69)         ▶ EDID (3/3)         ▶ RCP (0/2)         ▶ 3D (0/1)         ▶ UCP (0/2)	
<ul> <li>5.2.9.1: UCP Sub-Commands Receiving Test         Verify that the DUT responds to valid UCP sub-commands by displaying the character         or characters sent in the UCP command, or response to invalid UCP sub-commands by         displaying an error message.         (CTS 2.0 Only)</li> </ul>	
<ul> <li>5.2.9.2: UCP Sub-Commands Transmitting Test         Verify that the DUT sends valid UCP sub-commands by initiating the sending of UTF-8             characters in various formats through the user interface on the DUT.         (CTS 2.0 Only)         </li> </ul>	

9. You can save the Test Selection options using the **Save** activation button.

🗄 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Dongle CT 2.0 🕱	
😢 CDF Entry 🗸 Test Selection 🕨 Test Options / Preview	
Copen Save Contect All Tests Deselect All Tests	
▶ Dongle (6/40) ▶ Common (69/69) ▶ EDID (3/3) ▶ RCP (0/2) ▶ 3D (0/1) ▶ UCP (0/2)	

10. A dialog box will appear as follows. Simply assign a name and click on the **OK** activation button. Click **Cancel** to exit.

CBUS Dongle CT: Save Test Selections
Test Selection File
Enter a file name for the Test Selection.
My980_Select_Dongle_1 xml
My980_Select_Dongle.xml MySelect_Dongle.xml
Cancel Ok

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## 5.8 Executing the MHL CBUS Dongle Compliance Tests

Use the following procedures to initiate the execution of an MHL CBUS Dongle Compliance test series.

**Note**: The workflow screen examples in this section show MHL 2.0 except where noted. MHL 1.2 workflow and screens are similar.

### To initiate a test series:

1. Select the **Test Options / Preview** panel as shown below.

**Note**: The background tests are highlighted in light blue. These are tests that are run in the background during the remaining test suite. Refer to the two screen shots below.

Event Plot 隧 MHL Sink CT 2.0 🔯 CBUS Dongle CT 2.0 🛛	
CDF Entry 🗸 Test Selection 🕨 Test Options	
Test List	
All V X Instrument: [My980 [192.168.254.163]	ute Tests
Category / Test Name	1
5.2.5: EDID Test and Device Capability / Device Status Register Test	
▶ 5.2.5.1: EDID Test	V
5.2.5.2: Device Capability Register Test	E
5.2.5.3: Device Status Registers Test	<b>V</b>
5.2.8: 3D Video Test 5.2.8: 1: 3D Video Mode Support Data	
A = 5 2 9: UCP Sub-Command Tests	·
5.2.9.1: UCP Sub-Commands Receiving Test	1
• Iter 01: Test all supported Commands.	V
▲ 📃 5.2.9.2: UCP Sub-Commands Transmitting Test	V
Iter 01: Test all supported Commands.	$\checkmark$
5.3.3: Link Layer Electrical: Absolute Maximum Voltages	
5.3.3.1: Common Test Environment	$\checkmark$
5.3.3.2: CBE-Dongle: VBUS Absolute Maximum Positive Voltage	$\checkmark$
▶ 5.3.3.3: CBE-Dongle: CBUS Absolute Maximum Positive Voltage	<b>V</b>
4 5.3.5: Link Layer Timing - DUT Output: Pre-Discovery	
Iter 01: The Dongle is not nowered: Automatic PASS(SVIP)	
▲ ► 5.3.8: Link Laver Timing - DUT Output: Arbitration/Sung/Data in Bit Tim	
5.3.8.2: CBT-Dongle: Bit Timing Variation within a Packet	$\checkmark$
↓ 5.3.10: Link Laver Timing - DUT Output: Link Level NACK	
5.3.10.1: CBT-Dongle: ACK Output Timing in Nanoseconds	$\checkmark$
5.3.10.2: CBT-Dongle: ACK Drive HIGH Duration	$\checkmark$
5.3.11: Link Layer Timing - DUT Ouput: Bus Re-Arbitration	
5.3.11.4: CBT-Dongle: Dongle Never Sends Too Many Back-to-Back Packets	$\checkmark$
5.3.12: Link Layer Timing - DUT Output: Ill-formed packets	
5.3.12.1: CBT-Dongle: Dongle Never Sends Impulse Noise	<b>V</b>
▶ 5.3.12.2: CBT-Dongle: Dongle Never Sends Partial Packets	<b>V</b>
5.3.1/: LINK Layer Timing - DUT Input: Arbitration 5.3.17 1: CPT-Dongle: Loses Arbitration Correctly	
▶ ■ 5.3.17.1. CBT-Dongle: End of Discovery to Early Source-side Arbitration	$\checkmark$
E 5 3 17 3. CDT-Donglo: Donglo Losos Arbitration Collision Corroctly	
	•

2. (Optional) Review the list of tests for each category. If you wish to skip some of the tests. You can skip tests by clicking on the Check mark on the right side of the **Test Options / Preview** panel.

The screen shot below shows some of the tests that have been skipped (highlighted in yellow with a red X).

🗄 Event Plot 🔯 MHL Sink CT 2.0 🔯 CBUS Dongle CT 2.0 🛛	- 8
🔯 CDF Entry 🗹 Test Selection 🕨 Test Options / Preview	
Test List	
☑ All         ✓         X         Instrument:         My980 [192.168.254.163]         ▼         ► E	(ecute Tests
Category / Test Name	× ^
▲ ▶ 5.2.5: EDID Test and Device Capability / Device Status Register Test	
▶ 5.2.5.1: EDID Test	
5.2.5.2: Device Capability Register Test	
A b 5 2 9: 2D Video Test	
5.2.8.1: 3D Video Mode Support Data	×
X Iter 01:	×
▲ ▶ 5.2.9: UCP Sub-Command Tests	
5.2.9.1: UCP Sub-Commands Receiving Test	×
X Iter 01: Test all supported Commands.	×
4 5.2.9.2: UCP Sub-Commands Transmitting Test	
• Iter of: Test all supported commands.	V
5.3.3.1: Common Test Environment	$\checkmark$
5.3.3.2: CBE-Dongle: VBUS Absolute Maximum Positive Voltage	$\checkmark$
5.3.3.3: CBE-Dongle: CBUS Absolute Maximum Positive Voltage	$\checkmark$
5.3.5: Link Layer Timing - DUT Output: Pre-Discovery	
🔺 📃 5.3.5.1: CBT-Dongle: Time from Dongle Power applied until Dongle CBUS leave	×
X Iter 01: The Dongle is not powered: Automatic PASS(SKIP)	×
5.3.8: Link Layer Timing - DUT Output: Arbitration/Sync/Data in Bit T:	
↓ 5 3 10: Link Laver Timing - DUT Output: Link Level NACK	~
▶ 5.3.10.1: CBT-Dongle: ACK Output Timing in Nanoseconds	<b>V</b>
5.3.10.2: CBT-Dongle: ACK Drive HIGH Duration	V
▲ ▶ 5.3.11: Link Layer Timing - DUT Ouput: Bus Re-Arbitration	
5.3.11.4: CBT-Dongle: Dongle Never Sends Too Many Back-to-Back Packets	$\checkmark$
5.3.12: Link Layer Timing - DUT Output: Ill-formed packets	
5.3.12.1: CBT-Dongle: Dongle Never Sends Impulse Noise	
5.3.12.2: CBT-Dongle: Dongle Never Sends Partial Packets	V
5.3.17: LINK Layer Timing - DUT input: Arbitration	$\checkmark$
5.3.17.2: CBT-Dongle: End of Discovery to Early Source-side Arbitration	×
E F O 17 O. ADM Devels, Devels free Babitantine Arllinian Armonthe	<u></u>

3. Click on the Execute Tests activation button to initiate the test suite. You will be prompted for a name for the tests. This dialog box is shown below.

BUS Dongle CT Results				
📃 Test Results Name				
Execute CBUS Dongle Compliance Tests on Instrument: My980 @ 192.168.254.163				
Enter a name for the Test Results.				
Acme_XYZ_Dongle_Test_1				
Dongle_Test_1				
Cancel Ok				

A screen will appear instructing you on how to connect your MHL CBUS dongle device for testing. A sample screen is shown below:



During the test, the test results are shown. There is a progress arrow which points to the test that is currently being run. The lower panel **Test Log** shows the testing activity as it occurs. Refer to the screen examples below.



You can cancel the compliance test or pause it at any time. If you pause the test you can resume later at any time even if you exit the 980 Manager application. Refer to the following screen example.



You can view the details of failures and passes when they occur by exposing the navigation arrows on the left. Examples are shown on the following two screens.

	Test List		
🖌 All 🔀 All	Reset Status		
Category / Tes	st Name	V	Status
> \varTheta Iter 01		Image: A start of the start	Pass
▶ 6.3.5: MS	C - DUT Output: Never Initiates Bad Commands		
▶ 📑 6.3.5.1:	CBM: DUT Never Sends Reserved Commands		Pass
▶ 📃 6.3.5.2:	CBM: DUT Never Sends Illegal Commands		Pass
▶ 📑 6.3.5.3:	CBM: DUT Never Sends Data While No Command is Outstanding		Pass
▶ 5.3.5.4:	CBM: DUT Never Sends (0x33) ACK packet While No Command is Out	standi	Pass
▶ 📑 6.3.5.5:	CBM: DUT Never Sends (0x34) NACK Packet While No Command is Ou	itstand:	Pass
▲ 🖪 6.3.5.6:	CBM: DUT Never Sends (0x35) ABORT While No Command is Outstand	ling	Fail
⊿ ⊌ Iter 01	Continuous Background Test		Fail
6.3.2	1.2: At 01067298.50 us, DUT sent unexpected ABORT		
6.3.2	1.2: At 04137449.22 us, DUT sent unexpected ABORT		
6.3.2	1.2: At 07207399.58 us, DUT sent unexpected ABORT		
6.3.2	1.2: At 102/7341.05 us, Dor sent unexpected ABORT		
6.3.2	1.2: bol sent 4 unexpected Aborts		
6.3.2	1.3: At 04137660 33 ps. DUT sent unexpected ABODT		
6 3 2	1.3: At 07207665.35 us, DUT sent unexpected ABORT		
6 3 2	1.3: At 10277580 78 us, DUT sent unexpected ABORT		
6.3.2	1.3: DUT sent 4 unexpected ABORTs		
6.3.2	1.4: At 01067252.66 us. DUT sent unexpected ABORT		
6.3.2	1.4: At 04137408.50 us, DUT sent unexpected ABORT		
6.3.2	1.4: At 07207421.03 us, DUT sent unexpected ABORT		
6.3.2	1.4: At 10277348.73 us, DUT sent unexpected ABORT		
	Testlar		
	Test Log		
ine	Message		
0638	Saving the test logs.		
0639	Test 6.3.22.2 Iter 01 $\rightarrow$ Pass		
0640	Test 6.3.22.3-01		
0641	Executing the test.		
0642	Retrieving test results.		
0643	Processing test results.		
0644	Saving the test logs.		
0645	Test $6.3.22.3$ Iter $01 \rightarrow Pass$		
0646	Tests completed		

	Test List		
V All 🗶 All 🔄 Reset St	atus		
Category / Test Name		×	Status
⊿ 🗏 6.3.10.7: CBM	: DUT Receives (0x68) MSC MSG Command - RCP Support == 1 a	nd RAP	Pass
Iter 01:		<b>V</b>	Pass
🔺 🖪 6.3.10.8: CBM	: DUT Receives (0x6A) GET DDC ERRORCODE Command		Pass
þ 🔵 Iter 01:		<b>V</b>	Pass
▲ ▶ 6.3.11: MSC -	DUT Input: Errors and Exceptions		
⊿ 📑 6.3.11.1: CBM	: DUT Receives Reserved Commands		Pass
Iter 01:		$\checkmark$	Pass
▲ 📙 6.3.11.2: CBM	: DUT Receives Illegal Commands		Pass
b lter 01:		<b>V</b>	Pass
- 6.3.11.3: CBM	: DUT Receives Data While No Command Outstanding		Pass
▶ 😂 Iter 01:		<b>V</b>	Pass
▲ 🗄 6.3.11.4: CBM	: DUT Receives (0x33) ACK Packet While No Command Outstand	ling	Pass
> U Iter 01:		<b>V</b>	Pass
▲ 📑 6.3.11.5: CBM	: DUT Receives (0x34) a NACK Packet While No Command Outst	anding	Pass
>   Iter 01:		×	Pass
▲ [5 6.3.11.6: CBM	: DUT Receives (0x32) EOF While No Command Outstanding		Pass
→ ■ Iter U1:	· Dim Developer (0-25) BDODM Middle Me General Orbeiter diese	×	Pass
▲ [] 0.3.11.7: CBM	: DUT Receives (0x35) ABORT While No Command Outstanding		Fall P-il
	: DUE Receiver (0x61) PEAD DEVCAD - Offset Centrel	✓	Dass
▶ ▲ Iter 01:	. DOI RECEIVES (ONDI) READ DEVCAP OFFSet CONCIDE	<u> </u>	Pass
▲ ■ 6 3 11 9: CBM	: DUT Receives (0x61) READ DEVCAP - Offset Invalid	· · · ·	In Progress
→ Iter 01:	· boi Moorres (Wor) has shown orrest invaria		In Progress
4/1001 011		v	in Hogeboo
	Test Log		
Line Me	ssage		
• 0424 Te	st 6.3.11.7 Iter 01 -> Fail		
• 0425	- Test 6.3.11.8-01		
• 0426			
• 0427	Retrieving test results.		
• 0428	Processing test results.		
• 0429	Saving the test logs.		
• 0430 Te	st 6.3.11.8 Iter 01 -> Pass		
• 0431	- Test 6.3.11.9-01		
A 420	Executing the test		

The log will indicate when the tests have completed.

SUS Dongle Compliance Test (1.2): "Dongle_Test_1"		(m)	
Test List			
🖌 All 🙀 All 🔅 Reset Status			
Category / Test Name	1	Status	
A > 2.26. Tink Taken Timing - DIT VALUE Transition	· ·		
A 5.3.26. If the Layer I find a Dor VBUS Transition		Skipped	
• Iter 01: The Dongle does not accept power from the Source: Automatic PASS(SKIP)	<b>V</b>	Skipped	
6.3.1: MSC - DUT Input: Device Register Space Contents: Reads			
■ ■ 6.3.1.1: CBM: Capability Regs; READ DEVCAP of Capability Register Contents		Fail	
4 😝 Iter 01:	<b>V</b>	Fail	
• DUT discovered in 470 ms.			
🧼 01: procedure did not TIMEOUT		Pass	
$\ominus$ 02: replied with an ACK packet followed by a Data packet within 2 * TPK	Γ.5	Pass	
⊖ 03: read data documented in the CDF		Pass	-
$\triangleright \ominus$ 04: DUT is a Source or Sink and RCP SUPPORT and RAP SUPPORT are both 1		Fail	
• $\bigcirc$ 05: DUT is a Source or Sink and SP SUPPORT is 1		Fail	
UUT is a Source or Sink and SP_SUPPORT is not 1			
⊖ 06: SP SUPPORT is 1 and SCRATCHPAD SIZE is between 16 and 64		Pass	
Q 07: value in bits [7:4] is greater than or equal to 0x3		Pass	
$\ominus$ 08: value in bits [3:0] is greater than or equal to 0x3		Pass	_
6.3.2: MSC - DUT Output: Vendor-specific and Reserved Header Values			_
▶ ■ 6.3.2.1: CBM: DUT Sends Vendor-Specific and Reserved Header Values		Pass	
6.3.3: MSC - DUT Output: Normal Commands	_	D	_
▲ 6.3.3.1: CEM: DUT sends (Ux62) GET STATE Command		Pass	
▶ Ther u: ■ 5 2 2 0, CPU: DUE goods (0x52) CPE UENDOR ID Command	×	Pass	
A top 11		Pass	
▷ Uter u:	V	Pass	·
Test Log			
Line Message			
• 0638 Saving the test logs.			
• 0639 Test 6.3.22.2 Iter 01 -> Pass			
• 0640 Test 6.3.22.3-01			
• 0641 Executing the test.			
• 0642 Retrieving test results.			
0643 Processing test results.			
• 0644 Saving the test logs.			
• 0645 Test 6.3.22.3 Iter 01 -> Pass			_
• 0646 Tests completed			
💢 Close Window 🔰 🕨 Continue Testing			

When the tests are completed the test window that shows the current activity will close. A new tab and panel will appear next to the **CBUS Dongle CT 1.2** tab called the **CT Results** tab. You can view the test results in this panel. Refer to the following screen shots to see examples of the **CT Results** panel.

🖶 Event Plot 🔤 Edid Editor 🔯 EDID CT 1.4a	CBUS Src CT1.2 🔯 CBUS Dongle CT1.2 📄 CT Results 🖂		- 8
Results Name: Dongle_Test_1	CBUS Dongle compliance lest results Manufacturer: QD		ma HTML Report
Date Tested: September 13, 2012 4:24 PM	Model Name: XYZ		
Overall Status: CTS 1.2 - Fail	Port Tested: 1		
	Test Results		
Test Name / Details		1	Status ^
5 2 5 1: EDID Tost		~	Fail
5 2 5 2: Device Capab	ility Register Test		Fail
5 3 3 1: Common Test	Environment		Pass
5.3.3.2: CBE-Dongle: 1	VBUS Absolute Maximum Positive Voltage		Pass
5.3.3.3: CBE-Dongle:	CBUS Absolute Maximum Positive Voltage		Pass
5.3.4.1: CBE-Dongle:	Powered-Off Z[CBUS SINK DISCOVER]		Skipped
5.3.4.2: CBE-Dongle:	VBUS-Powered Z[CBUS SINK DISCOVER]		Pass
5.3.4.3: CBE-Dongle:	Locally-Powered Z[CBUS SINK DISCOVER]		Pass
5.3.5.1: CBT-Dongle:	Time from Dongle Power applied until Dongle CBUS leaves HIGH-	-	Fail
5.3.6.1: CBE-Dongle:	Post-Discovery Passive Pulldown Z[CBUS SINK ON] Resistance		Pass
5.3.6.2: CBE-Dongle:	CBUS Capacitance		Fail
5.3.6.3: CBE-Dongle: 1	Arbitrate/Sync/Data Drive LOW Voltage		Pass
5.3.6.4: CBE-Dongle: 1	Arbitrate/Sync/Data Drive HIGH Voltage		Pass
5.3.7.1: CBT-Dongle: 1	Arbitration/Sync/Data Active Drive HIGH Duration		Pass
5.3.7.2: CBT-Dongle: 1	Arbitration/Sync/Data Edge Rate		Pass
5.3.8.1: CBT-Dongle: 2	Arb, Sync, Data HIGH and LOW Timing		Pass
5.3.8.2: CBT-Dongle: 1	Bit Timing Variation within a Packet		Fail
5.3.9.1: CBT-Dongle: 1	Response to Link Level NACK		Pass
5.3.10.1: CBT-Dongle:	ACK Output Timing in Nanoseconds		Pass
5.3.10.2: CBT-Dongle:	ACK Drive HIGH Duration		Pass
5.3.11.1: CBT-Dongle:	Dongle uses Case 2 Regular Arbitration after NACK		Pass
5.3.11.2: CBT-Dongle:	Dongle uses Case 3 Long Re-arbitration when it Gives up the		Pass
5.3.11.3: CBT-Dongle:	Dongle uses Case 1 Back-to-Back Timing (No Re-arbitration)		Pass
5.3.11.4: CBT-Dongle:	Dongle Never Sends Too Many Back-to-Back Packets		Pass
5.3.12.1: CBT-Dongle:	Dongle Never Sends Impulse Noise		Pass
5.3.12.2: CBT-Dongle:	Dongle Never Sends Partial Packets		Pass
5.3.13.1: CBE-Dongle:	Discovery Sensitivity to Input Voltages		Fail
5.3.14.1: CBT-Dongle:	Valid Wake Pulse Timing		Pass
5.3.14.2: CBT-Dongle:	Valid Discovery Pulse Timing		Pass 🔻
Instrument: My980 [192.168.254.135]			Continue Test Execution

## 5.9 Viewing Details of Dongle Compliance Test Passes or Failures

When you have completed the test series you will have an opportunity to view the detailed data for a particular failure. Use the following procedures to view the details of a test.

#### To view the details of each test:

1. Expose the detailed results of a failure and highlight a failure. Refer to the screen example below.

CBUS Dongle Compliance Test Results			
weights Name:     Dongle_Test_1     Manufacturer:     QD       Date Tested:     September 13, 2012 4:24 PM     Model Name:     XYZ       verall Status:     CTS 1.2 - Fail     Port Tested:     1			L R
Test Results			
Test Name / Details	0	Status	
5.2.5.1: EDID Test		Fail	
5.2.5.2: Device Capability Register Test		Fail	
E 5.3.3.1: Common Test Environment		Pass	
🛛 🗏 5.3.3.2: CBE-Dongle: VBUS Absolute Maximum Positive Voltage		Pass	
🛛 🗏 5.3.3.3: CBE-Dongle: CBUS Absolute Maximum Positive Voltage		Pass	
E 5.3.4.1: CBE-Dongle: Powered-Off Z[CBUS SINK DISCOVER]		Skipped	
E 5.3.4.2: CBE-Dongle: VBUS-Powered Z[CBUS SINK DISCOVER]		Pass	
E 5.3.4.3: CBE-Dongle: Locally-Powered Z[CBUS SINK DISCOVER]		Pass	
🛛 📃 5.3.5.1: CBT-Dongle: Time from Dongle Power applied until Dongle CBU	s	Fail	
4 😝 Iter 01:		Fail	
\varTheta This test is not ready for general usage yet.			
🥚 01: DUT CBUS enters HIGH-Z state within the Dongle Power-up time		Pass	
👄 02: DUT remains in high-z state for at least TSINK CBUS FLOAT		Pass	
$_{\odot}$ $_{\odot}$ 03: DUT asserts a valid ZCBUS DONGLE DISCOVER after the float per	r	Pass	
😑 😔 04: Dongle DUT posts a DCAP CHG interrupt within TDONGLE DCAP CHG	3	Pass	
🔺 🖌 🖉 05: Dongle DUT does not time out		Fail	
error Hait_Capability_Registers_Valid timed out.			
V 😔 06: READ DEVCAP succeeds		Pass	
		Pass	
👄 08: VBUS stays high, driven by Powered Dongle		Pass	
● 09: unfinished		Pass	
5.3.6.1: CBE-Dongle: Post-Discovery Passive Pulldown Z[CBUS SINK ON]		Pass	
5.3.6.2: CBE-Dongle: CBUS Capacitance		Fail	
5.3.6.3: CBE-Dongle: Arbitrate/Sync/Data Drive LOW Voltage		Pass	
5.3.6.4: CBE-Dongle: Arbitrate/Sync/Data Drive HIGH Voltage		Pass	
5.3.7.1: CBT-Dongle: Arbitration/Sync/Data Active Drive HIGH Duration	a 🗧	Pass	
5.3.7.2: CBT-Dongle: Arbitration/Sync/Data Edge Rate		Pass	
5.3.8.1: CBT-Dongle: Arb, Sync, Data HIGH and LOW Timing		Pass	
E 5.3.8.2: CBT-Dongle: Bit Timing Variation within a Packet		Fail	

Similarly, you can view the details of a test which passed as shown below:

Results Name: Dongle_Test_1 M	anufacturer: QD		
Date Tested: September 13, 2012 4:24 PM	Model Name: XYZ		
Overall Status: CTS 1.2 - Fail	Port Tested: 1		
	Test Results		
Test Name / Details		Ö	Status
▷ 📑 5.2.5.1: EDID Test			Fail
5.2.5.2: Device Capability Register Test			Fail
5.3.3.1: Common Test Environment			Pass
▷ 5.3.3.2: CBE-Dongle: VBUS Absolute Maximum	Positive Voltage		Pass
▷ 5.3.3.3: CBE-Dongle: CBUS Absolute Maximum	Positive Voltage		Pass
<pre>&gt; 5.3.4.1: CBE-Dongle: Powered-Off Z[CBUS SIN</pre>	IK DISCOVER]		Skipped
<pre>&gt; 5.3.4.2: CBE-Dongle: VBUS-Powered Z[CBUS S]</pre>	INK DISCOVER]		Pass
5.3.4.3: CBE-Dongle: Locally-Powered Z[CBUS	SINK DISCOVER]		Pass
5.3.5.1: CBT-Dongle: Time from Dongle Power	applied until Dongle CBUS		Fail
5.3.6.1: CBE-Dongle: Post-Discovery Passive	Pulldown Z[CBUS SINK ON]		Pass
5.3.6.2: CBE-Dongle: CBUS Capacitance			Fail
5.3.6.3: CBE-Dongle: Arbitrate/Sync/Data Dr	rive LOW Voltage		Pass
▲ 📑 5.3.6.4: CBE-Dongle: Arbitrate/Sync/Data Dr	rive HIGH Voltage		Pass
4 🔰 Iter 01:			Pass
• DUT discovered in 440 ms.			
Incoming ack bit time: 1006 hs			<b>D</b>
01: DUT arbitrates for the bus to send	a data packet to the Teste		Pass
V A U2: DUT drives CBUS below Vol CDUs{max}	during Arbitration, Sync,		Pass
<ul> <li>analyzing arp pulse</li> <li>low pplace time below midpoints 00000001 00</li> </ul>	time below Vol: 0000001 00		
<ul> <li>Low purse: time below micpoint: 00000001.00 us</li> <li>analyzing sums pulse</li> </ul>	; cime below vol: 00000001.00 us		
<ul> <li>andryzing sync purse</li> <li>Low pulse; time below midpoint; 00000001 49 pc</li> </ul>	time below Vol: 00000001 49 mg		
analyzing header control data and parity pu	lees		
I low pulse: time below midpoint: 00000000 48 pe	time below Vol: 00000000 48 ne		
Low pulse: time below midpoint: 00000001 01 ps	: time below Vol: 00000001 01 us		
<ul> <li>Low pulse: time below midpoint: 00000001 02 ps</li> </ul>	: time below Vol: 00000001.01 us		
▶ ■ 5 3 7 1: CRT-Dongle: Arbitration/Sync/Data	Active Drive HIGH Duration		Pass
▶ 5.3.7.2: CBT-Dongle: Arbitration/Sync/Data	Edge Rate		Pass
5.3.8.1: CBT-Dongle: Arb, Sync, Data HIGH a	and LOW Timing		Pass
5.2.5.1: EDID Tect			

## 5.10 Accessing the test results through the navigator panel

You can view the results of the tests at any time after you run them through the 980 GUI Manager's **Navigator** panel. Use the following procedures to view the details of a test.

### To access the test results:

1. Access the **Navigator** tab and select **Compliance**. Refer to the screen example below.



2. Double click on the Results file you wish to view. The results will appear in a CT Results window on the right. Refer to the screen example below.

🔠 Event Plot 🔤 Edid Editor 🔯 EDID CT 1.4a 🔯 CBUS Src CT 1.2 🔯 CBUS Dongle CT 1.2 📳 CT Results 🗵		- 6
CBUS Dongle Compliance Test Results		
Results Name:         Dongle_Test_1         Manufacturer:         QD           Date Tested:         September 13, 2012 4:24 PM         Model Name:         XVZ           Overall Status:         CTS 1.2 - Fail         Port Tested: 1		HTML Report
Test Results		
Test Name / Details	0	Status
■ 5.2.5.1: EDID Test		Fail
5.2.5.2: Device Capability Register Test		Fail
5.3.3.1: Common Test Environment		Pass =
E 5.3.3.2: CBE-Dongle: VBUS Absolute Maximum Positive Voltage		Pass
📙 5.3.3.3: CBE-Dongle: CBUS Absolute Maximum Positive Voltage		Pass
5.3.4.1: CBE-Dongle: Powered-Off Z[CBUS SINK DISCOVER]		Skipped
5.3.4.2: CBE-Dongle: VBUS-Powered Z[CBUS SINK DISCOVER]		Pass
5.3.4.3: CBE-Dongle: Locally-Powered Z[CBUS SINK DISCOVER]		Pass
5.3.5.1: CBT-Dongle: Time from Dongle Power applied until Dongle CBUS leaves HIGH-		Fail
5.3.6.1: CBE-Dongle: Post-Discovery Passive Pulldown Z[CBUS SINK ON] Resistance		Pass
5.3.6.2: CBE-Dongle: CBUS Capacitance		Fail
5.3.6.3: CBE-Dongle: Arbitrate/Sync/Data Drive LOW Voltage		Pass
5.3.6.4: CBE-Dongle: Arbitrate/Sync/Data Drive HIGH Voltage		Pass
5.3.7.1: CBT-Dongle: Arbitration/Sync/Data Active Drive HIGH Duration		Pass
5.3.7.2: CBT-Dongle: Arbitration/Sync/Data Edge Rate		Pass
5.3.8.1: CBT-Dongle: Arb, Sync, Data HIGH and LOW Timing		Pass
5.3.8.2: CBT-Dongle: Bit Timing Variation within a Packet		Fail
5.3.9.1: CBT-Dongle: Response to Link Level NACK		Pass
5.3.10.1: CBT-Dongle: ACK Output Timing in Nanoseconds		Pass
5.3.10.2: CBT-Dongle: ACK Drive HIGH Duration		Pass
5.3.11.1: CBT-Dongle: Dongle uses Case 2 Regular Arbitration after NACK		Pass
5.3.11.2: CBT-Dongle: Dongle uses Case 3 Long Re-arbitration when it Gives up the		Pass
5.3.11.3: CBT-Dongle: Dongle uses Case 1 Back-to-Back Timing (No Re-arbitration)		Pass
5.3.11.4: CBT-Dongle: Dongle Never Sends Too Many Back-to-Back Packets		Pass
5.3.12.1: CBT-Dongle: Dongle Never Sends Impulse Noise		Pass
5.3.12.2: CBT-Dongle: Dongle Never Sends Partial Packets		Pass
5.3.13.1: CBE-Dongle: Discovery Sensitivity to Input Voltages		Fail
5.3.14.1: CBT-Dongle: Valid Wake Pulse Timing		Pass
5.3.14.2: CBT-Dongle: Valid Discovery Pulse Timing		Pass T
Instrument: My980 [192.168.254.135]		Continue Test Execution

# 5.11 Viewing the MHL Dongle Compliance HTML test report

After you have completed the tests, an HTML Report activation button will appear in the upper right of the screen which enables you to access the html report of the test results. Use the following procedures to view the html test report.

### To view the html test report:

1. Select the CT Results panel as shown below.

🗄 Event Plot 🔤 Edid Editor 😢 EDID CT 1.4a 🥸 CBUS Src CT 1.2 🔯 CBUS Dongle CT 1.2 📑 CT Results 🛛		(B
CBUS Dongle Compliance Test Results		
Results Name: Dongle_Test_1 Manufacturer: QD		HTML Report
Date Tested: September 13, 2012 4:24 PM Model Name: XYZ		
Overall Status: CTS 1.2 - Fail Port Tested: 1		
Test Results		
Test Name / Details	Ö	Status
E 5.2.5.1: EDID Test		Fail
📙 5.2.5.2: Device Capability Register Test		Fail
5.3.3.1: Common Test Environment		Pass
📙 5.3.3.2: CBE-Dongle: VBUS Absolute Maximum Positive Voltage		Pass
📙 5.3.3.3: CBE-Dongle: CBUS Absolute Maximum Positive Voltage		Pass
5.3.4.1: CBE-Dongle: Powered-Off Z[CBUS SINK DISCOVER]		Skipped
5.3.4.2: CBE-Dongle: VBUS-Powered Z[CBUS SINK DISCOVER]		Pass
5.3.4.3: CBE-Dongle: Locally-Powered Z[CBUS SINK DISCOVER]		Pass
5.3.5.1: CBT-Dongle: Time from Dongle Power applied until Dongle CBUS leaves HIGH-		Fail
📙 5.3.6.1: CBE-Dongle: Post-Discovery Passive Pulldown Z[CBUS SINK ON] Resistance		Pass
5.3.6.2: CBE-Dongle: CBUS Capacitance		Fail
📙 5.3.6.3: CBE-Dongle: Arbitrate/Sync/Data Drive LOW Voltage		Pass
5.3.6.4: CBE-Dongle: Arbitrate/Sync/Data Drive HIGH Voltage		Pass
5.3.7.1: CBT-Dongle: Arbitration/Sync/Data Active Drive HIGH Duration		Pass
5.3.7.2: CBT-Dongle: Arbitration/Sync/Data Edge Rate		Pass
📃 5.3.8.1: CBT-Dongle: Arb, Sync, Data HIGH and LOW Timing		Pass
📙 5.3.8.2: CBT-Dongle: Bit Timing Variation within a Packet		Fail
5.3.9.1: CBT-Dongle: Response to Link Level NACK		Pass
5.3.10.1: CBT-Dongle: ACK Output Timing in Nanoseconds		Pass
5.3.10.2: CBT-Dongle: ACK Drive HIGH Duration		Pass
📃 5.3.11.1: CBT-Dongle: Dongle uses Case 2 Regular Arbitration after NACK		Pass
5.3.11.2: CBT-Dongle: Dongle uses Case 3 Long Re-arbitration when it Gives up the		Pass
📃 5.3.11.3: CBT-Dongle: Dongle uses Case 1 Back-to-Back Timing (No Re-arbitration)		Pass
📃 5.3.11.4: CBT-Dongle: Dongle Never Sends Too Many Back-to-Back Packets		Pass
5.3.12.1: CBT-Dongle: Dongle Never Sends Impulse Noise		Pass
5.3.12.2: CBT-Dongle: Dongle Never Sends Partial Packets		Pass
5.3.13.1: CBE-Dongle: Discovery Sensitivity to Input Voltages		Fail
5.3.14.1: CBT-Dongle: Valid Wake Pulse Timing		Pass
5.3.14.2: CBT-Dongle: Valid Discovery Pulse Timing		Pass -
Instrument: My980 [192.168.254.135]		▼ ► Continue Test Execution

2. Click on the HTML Report activation button.

A dialog box will appear asking if you want a summary of the test results or a version that includes the CDF. This dialog box is shown in the screen shot below.

Generate Report
HTML Report
Dongle_Test_1
Select the desired report options.
Show Test Summary Only.
✓ Include CDF Information.
Cancel V OK

Specify if you want to see a summary report and if you want to see the CDF. If you leave Show Test Summary Only unchecked the application will produce a full detailed report. The following screens provide samples of the report. Note the first items in the CDF shown below.

Note: This example shows an MHL 1.2 test result; MHL 2.0 test results are similar in content and structure.

C:\Users\nkendall	,Desktop\980_CBUS_GUI\980mgr\cbusdonglect\results\Dongle_Test_1	\Report_Summary_Cdf.htm							
Ot generated on: September 17, 2012 4:50 PM CBUS Dongle Compliance Test Report CTS 1.2									
Results Name: Date Tested: <b>Overall Status:</b>	Dongle_Test_1 September 13, 2012 4:24 PM Fail	Manufacturer: QD Model Name: XYZ Port Tested: -							
	Capabilities Declaration Form (CDF)	)							
	General								
CDF_MFR_NAME	QD								
CDF_MODEL_NUMBER	XYZ								
CDF_D_CBUS_THRESHOLD_V		0.90							
CDF_D_CBUS_THRESHOLD_V CDF_D_MAX_CBUS_CAP		0.90							
CDF_D_CBUS_THRESHOLD_V CDF_D_MAX_CBUS_CAP CDF_D_POWERED		0.90 0.1 YES							
CDF_D_CBUS_THRESHOLD_V CDF_D_MAX_CBUS_CAP CDF_D_POWERED CDF_D_MAX_POWER_DOWN		0.90 0.1 YES 500							
CDF_D_CBUS_THRESHOLD_V CDF_D_MAX_CBUS_CAP CDF_D_POWERED CDF_D_MAX_POWER_DOWN CDF_D_MAX_POWER_UP		0.90 0.1 YES 500 500							
CDF_D_CBUS_THRESHOLD_V CDF_D_MAX_CBUS_CAP CDF_D_POWERED CDF_D_MAX_POWER_DOWN CDF_D_MAX_POWER_UP CDF_D_MAX_STANDBY_TO_ACTI	VE	0.90 0.1 YES 500 60							
CDF_D_CBUS_THRESHOLD_V CDF_D_MAX_CBUS_CAP CDF_D_POWERED CDF_D_MAX_POWER_DOWN CDF_D_MAX_POWER_UP CDF_D_MAX_STANDBY_TO_ACTI CDF_PROC_SET_ACTIVE	VE	0.90 0.1 YES 500 500 60 Not Specified							
CDF_D_CBUS_THRESHOLD_V CDF_D_MAX_CBUS_CAP CDF_D_POWERED CDF_D_MAX_POWER_DOWN CDF_D_MAX_POWER_UP CDF_D_MAX_STANDBY_TO_ACTI CDF_PROC_SET_ACTIVE CDF_PROC_SET_STANDBY	VE	0.90 0.1 YES 500 60 Not Specified Not Supported							
CDF_D_CBUS_THRESHOLD_V CDF_D_MAX_CBUS_CAP CDF_D_POWERED CDF_D_MAX_POWER_DOWN CDF_D_MAX_POWER_UP CDF_D_MAX_STANDBY_TO_ACTI CDF_PROC_SET_ACTIVE CDF_PROC_SET_STANDBY CDF_RCP_RECEIVE	VE	0.90 0.1 YES 500 60 Not Specified Not Supported NO							
CDF_D_CBUS_THRESHOLD_V CDF_D_MAX_CBUS_CAP CDF_D_POWERED CDF_D_MAX_POWER_DOWN CDF_D_MAX_POWER_UP CDF_D_MAX_STANDBY_TO_ACTI CDF_PROC_SET_ACTIVE CDF_PROC_SET_STANDBY CDF_RCP_RECEIVE CDF_RCP_SEND	VE	0.90 0.1 YES 500 60 Not Specified Not Supported NO NO							
CDF_D_CBUS_THRESHOLD_V CDF_D_MAX_CBUS_CAP CDF_D_POWERED CDF_D_MAX_POWER_DOWN CDF_D_MAX_POWER_UP CDF_D_MAX_STANDBY_TO_ACTI CDF_PROC_SET_ACTIVE CDF_PROC_SET_STANDBY CDF_RCP_RECEIVE CDF_RCP_SEND CDF_LOG_DEV_MAP_CHANGE	VE	0.90           0.1           YES           500           60           Not Specified           Not Supported           NO           NO           NO           NO							
CDF_D_CBUS_THRESHOLD_V CDF_D_MAX_CBUS_CAP CDF_D_POWERED CDF_D_MAX_POWER_DOWN CDF_D_MAX_POWER_UP CDF_D_MAX_STANDBY_TO_ACTI CDF_PROC_SET_ACTIVE CDF_PROC_SET_STANDBY CDF_RCP_RECEIVE CDF_RCP_SEND CDF_LOG_DEV_MAP_CHANGE	VE Capability Registers	0.90           0.1           YES           500           60           Not Specified           NO           NO           NO							
CDF_D_CBUS_THRESHOLD_V CDF_D_MAX_CBUS_CAP CDF_D_POWERED CDF_D_MAX_POWER_DOWN CDF_D_MAX_POWER_UP CDF_D_MAX_STANDBY_TO_ACTI CDF_PROC_SET_ACTIVE CDF_PROC_SET_STANDBY CDF_RCP_RECEIVE CDF_RCP_SEND CDF_LOG_DEV_MAP_CHANGE CDF_CR_MHL_VER_MAJOR	VE Capability Registers	0.90           0.1           YES           500           60           Not Specified           Not Supported           NO           NO           1							

The summary results are shown below:

Viewer						
Test 5 3 23 2	C:\Users\nkendall\D Fail	esktop\980_CBUS_GUI\980mg Test 5 3 23 3	r\cbusdonglect\results\Dongl	le_Test_1\Report_Cdf.htm Test 5 3 24 1	Pass	
Test 5 3 25 1	Skinned	Test 5 3 26 1	Skinned	Test 6 3 1 1	Fail	
Test 6 3 2 1	Pass	Test 6 3 3 1	Pass	Test 6 3 3 2	Pass	
Test 6.3.3.3	Pass	Test 6 3 3 4	Pass	Test 6 3 3 5	Pass	
Test 6.3.3.6	Pass	Test 6 3 3 7	Pass	Test 6 3 5 1	Pass	
Test 6 2 5 2	Pass	Test 6 3 5 3	Pass	Test 6.3.5.4	Pass	
Test 6.3.5.5	Pass	Test 6.3.5.6	Fail	Test 6 3 5 7	Para	
Test 6 3 6 1	Pass	Test 6 3 6 2	Pass	Test 6 3 6 3	Para	
Test 6.2.6.4	T ass	Test 6.3.6.5	T ass	Test 6.2.7.1	T ass	
Test 6.3.0.4	Pass	Test 6.3.0.3	Pan	Test 6.2.0.1	Pass	
Test 6 2 10 1	Pass	Test 6.2.10.2	r ass	Test 6.2.10.2	Pass	
<u>1est 6.3.10.1</u>	Pass	<u>Test 6.3.10.2</u>	Pass	<u>1est 6.3.10.3</u>	Pass	
<u>1est 6.3.10.4</u>	Pass	Test 6.3.10.5	Pass	<u>1est 6.3.10.6</u>	Pass	
<u>1est 6.3.10.7</u>	Pass	<u>1est 6.3.10.8</u>	Pass	<u>1est 6.3.11.1</u>	Pass	
<u>Test 6.3.11.2</u>	Pass	Test 6.3.11.3	Pass	<u>Test 6.3.11.4</u>	Pass	
<u>Test 6.3.11.5</u>	Pass	Test 6.3.11.6	Pass	<u>Test 6.3.11.7</u>	Fail	
Test 6.3.11.8	Pass	Test 6.3.11.9	Pass	Test 6.3.11.10	Pass	
Test 6.3.11.11	Pass	Test 6.3.11.12	Pass	Test 6.3.11.13	Pass	
Test 6.3.11.14	Pass	Test 6.3.11.15	Fail	Test 6.3.11.16	Pass	
Test 6.3.11.17	Pass	Test 6.3.11.19	Pass	Test 6.3.11.20	Pass	
Test 6.3.11.21	Fail	Test 6.3.11.22	Pass	Test 6.3.11.23	Pass	
Test 6.3.11.24	Pass	Test 6.3.12.1	Fail	Test 6.3.12.2	Fail	
Test 6.3.12.3	Fail	Test 6.3.12.4	Fail	Test 6.3.12.5	Pass	
Test 6.3.12.6	Pass	Test 6.3.12.7	Pass	Test 6.3.12.8	Pass	
Test 6.3.12.9	Pass	Test 6.3.15.1	Skipped	Test 6.3.15.2	Skipped	1
Test 6.3.16.1	Skipped	Test 6.3.16.2	Skipped	Test 6.3.20.2	Pass	
Test 6.3.20.3	Pass	Test 6.3.21.1	Pass	Test 6.3.21.2	Pass	
Test 6.3.21.3	Pass	Test 6.3.21.4	Pass	Test 6.3.21.5	Fail	
Test 6.3.22.1	Pass	Test 6.3.22.2	Pass	Test 6.3.22.3	Pass	
Cl	DF	Equipn	nent Info			1
				•		•

Close

The final page of the report shows the test equipment configuration as shown below.

Name: My980 IP Address: 192.168.254.135 Net Mask: 255.255.255.0 Gateway IP: 192.168.254.1 Free Space: 121.08 GB of 144.22 GB (84.0%) Version: Advanced Test platform Release: 4.5.27	
Name: My980 IP Address: 192.168.254.135 Net Mask: 255.255.255.0 Gateway IP: 192.168.254.1 Free Space: 121.08 GB of 144.22 GB (84.0%) Version: Advanced Test platform Release: 4.5.27	
Name: My980 IP Address: 192.168.254.135 Net Mask: 255.255.255.0 Gateway IP: 192.168.254.1 Free Space: 121.08 GB of 144.22 GB (84.0%) Version: Advanced Test platform Release: 4.5.27	
Net Mask: 255.255.255.0 Gateway IP: 192.168.254.1 Free Space: 121.08 GB of 144.22 GB (84.0%) Version: Advanced Test platform Release: 4.5.27	
Gateway IP: 192.168.254.1 Free Space: 121.08 GB of 144.22 GB (84.0%) Version: Advanced Test platform Release: 4.5.27	
Free Space: 121.08 GB of 144.22 GB (84.0%) Version: Advanced Test platform Release: 4.5.27	
Version: Advanced Test platform Release: 4.5.27	
Advanced Test platform Release: 4.5.27	
MHL CBUS Protocol Analyzer in slot 1:	
Gateware: [Version: 0 Build Number: 4 (09:11:2012 121000) pcb: 23232323]	
Sustem Information: 1.0.1 Dulid Number: 19/6 (mblair 09:13:2012 09:21:52 CDI)]	
System SN : [ 47A7D6F8C0A385A0::N/A]	
SN : [ 318383010000::11120010c]	
Main Board : [ "DP67DE"]	
CPUx4 : [ 6.42.7 "Intel(R) Core(TM) i3-2100 CPU @ 3.10GHz"]	
DDR : [ 3 GB + 768 MB]	
HD : [ WD1600BEVI-1]	
GUI manager : [ Version 4.5.27 39005 201209061011]	1
1 : [ lo inet 127.0.0.1/8 scope host lo]	
2 : [ eth0 inet 192.168.254.135/24 brd 192.168.254.255 scope global eth0]	
HDMI SINK CTS: [ 3.1.7]	
HDMI SRC CTS: [ 3.1.8]	
MHL SINK CIS: [ 1.2.0] MHI SEC CIS: [ 1.2.1]	
Host	
HT Names Quantum Data 000 Manager - Version 4 5 30	
UI Home: platform:/base/pluging/com.guantumdata.j980.app	
Java Vendor: Null	
Java Runtime: 1.6.0_15-b03	
Java Home: C:\Users\nkendall\Desktop\980_Release_5_29\980mgr\jre	
OS: win32	
OS Arch: x86	
Locale: en US	
free Space: 13.60 GD 01 133.60 GD (3.0%)	

# 6 CBUS Log Plot

The **CBUS Log Plot** panel (shown below) is panel used for viewing the bit and byte timing events of the CBUS controls and commands that occurred during a specific test. A CBUS Log Plot is provided for each source, sink and dongle CBUS compliance tests. You can disseminate these Log Plots to colleagues as part of the test results. Your colleagues, subject matter experts are not required to have a 980 test instrument to view them; they simply need to download the 980 GUI Manager application from the Quantum Data website.

The panel has both a graphical depiction of CBUS timing events and a sequential table list out of each event. The vertical axis shows the various CBUS event types. The **CBUS Log Plot** panel provides a set of CBUS event types labeled on the left that indicate the type of event. The horizontal axis is time. The scale along the bottom of the **CBUS Log Plot** shows the timestamp for each point in time.

The **CBUS Log Plot** is useful diagnosing CBUS compliance test failures.

The example below shows a series of events captured during a source test. The test section and number are shown on the top of the panel.

🖶 Event Plo	t 🕂 CBUS Plot 🛛 🚺	CT Results				- 0	
Data: MHL_C	BUS_2.0_121105\3_3_10_1_	01					
Rows     Rows	Segment						
	Zoom %:	0.252	A Marker 1		Marker 2 💽 💿 Đ		
0:0:1.501.489	.486						
(							
PASS			Pa	ss 1			
PACKET							
CBUS L/V							
PULSE							
CBUS DRV		DUT			DUT	DUT	
VBUS DRV			Те	ster			
VBUS LVL							
CBUS TRM	1000 ohms r	ulldown		100 k-oh	ms pulldown		
TMDS TRM	biob	-	70 ohm cullun				
THUS TRM	Tigh	2		70 01			
RXS+							
RXS-							
0:0:1.500	.598.325 0:0	0:1.501.365.345	0:0:1.50 Time (H:M:	2.136.797 S.ms.us.ns)	0:0:1.502.908.250	0:0:1.503.679.703	
TimeStamp		Туре	Description			•	
0:0:1.50	1.750.210	CBUS LVL	HIGH (0:0:0.00	00.499.540)		0	
0:0:1.50	1.750.290	CBUS TRM	100 k-ohms pulldown				
0:0:1.50	1.750.340	TMDS TRM	70 ohm pullup				
0:0:1.50	2.249.450	CBUS DRV	Tester is driv	Tester is driving CBUS			
0:0:1.50	2.249.750	CBUS LVL	LOW (0:0:0.000	0.001.050)			
0:0:1.50	2.249.750	PULSE	Sink arbitrate	es (case 3)			
0:0:1.50	2.249.750	PACKET	Sink -> Source	e <msc clr_hpd=""></msc>			
0:0:1.50	2.250.800	CBUS LVL	HIGH (0:0:0.00	00.003.980)			
0:0:1.50	2.250.850	CBUS DRV	DUT is driving	J CBUS			
0:0:1.50	2.234.480	CBUS DRV	lester is driv	ring CBUS		$\bigcirc$	
Events	🔯 Find						

# 6.1 Accessing the CBUS Log Plots

You can access the **CBUS Log Plot** through the **Navigator/Compliance** panel shown. There is a separate **CBUS Log Plot** for each test in a series of tests. Simply select the log and double click, select open from the right click menu or select the Open icon near the top of the panel to open a **CBUS Log Plot**. Refer to the following two screen shots to view the method of access for the **CBUS Log Plot**.







# 6.2 Locating Data in the CBUS Log Plot Panel

The **CBUS Log Plot** enables you to locate events by searching for specific event types, panning, scrolling and zooming using various techniques. You can filter the events by type to limit the amount of events to sift through. You can synchronize between the upper graphical section of the panel and the lower tabular section.

A scroll bar is provided to enable you to quickly browse through the data. The scroll bar is under the set of function icons just above the data panel where the data is displayed. You can also scroll to the end, scroll by page or scroll incrementally in either direction using the set of function backward and forward activation buttons. See the screen shot below.





## 6.3 Viewing Events in the CBUS Log Plot Panel

You can zoom in and zoom out and pan across the events using the slide bars provided. You can also zoom by surrounding a specific section of the captured events. These functions are described in the following table.

Even Plot Zoom & Panning Icons	Function
Icons – Zoom and Panning	<ul> <li>Surround activation button – You can select an area of the CBUS Log Plot by clicking and dragging across. When you do this the new view will be limited to the horizontal range that you selected. The midpoint of the selection will become the new center of the data displayed.</li> </ul>
	<ul> <li>Zoom % – The Zoom % function enables you to enter a specific zoom amount in the associated field provided.</li> </ul>
	<ul> <li>Zoom In/Out icons • The Zoom In/Out function buttons enables you to zoom in and zoom out by clicking on the activation button. The centered point will remain the same.     </li> </ul>
	<ul> <li>Panning Panning – The panning function enables you scan across the data quickly by clicking and dragging.</li> </ul>
	<ul> <li>Pointer          — The pointer icon enables you to click on any point and obtain information such as the data packet type and the timestamp, about that data packet. The information is displayed in a dark panel just above the scroll bar and below the icons.</li> </ul>

### 6.3.1 Surrounding and Zooming with the Range Zoom tool

The **CBUS Log Plot** provides a Range Zoom tool . You can select an area of the plot by clicking and dragging across. When you do this the new view will be limited to the horizontal range that you selected. The midpoint of the selection will become the new center of the events displayed. The two screens below show an example of surrounding a segment of data. The rectangular section identified by the arrows in the screen example below indicates the section that is surrounded. The second view shows the resulting view.



The resulting view is shown below.



# 6.4 Viewing the Timestamps of the Events

There is a scroll bar on the status panel just above the events that indicates the location of the scroll bar. When you scroll or pan through the data, the timestamps are shown in the status panel below the window where the events are displayed. If you use the pointer tool to select a particular event, the timestamp will be shown in the dark strip above the graphical window and below the control icons. The timestamp in this area always reflects the location of

the cursor. Also when you click on an item in the graphical window the event item will be shown in lower table view. In the example below, a selection has been made on a sync pulse with the pointer tool.

🖶 Event Plot 🔂 CBUS Plot 🕱 📳 CT Results 🗧 🗖							
Data: MHL_C	BUS_2.0_121105\3_3_10_1	01					
€ /s	Segment						
	🖑 🔍 Zoom %:	2.999	🔍 🔍 📃 Marker 1		Marker 2 🗲 🔹 🔁		
0:0:0.612.182	2.639						
DASS			Dage 1				
FA33			Fass 1				
PACKET		innene					
CBUS L/V							
PULSE	wake to discover lov	v					
CBUS DRV	DUT		DUT		DUT		
VBUS DRV		<b>`</b>	Tester				
VBUS LVL							
CBUS TRM	1000 ohms pulldov	wn		100 k-ohms pulldo	wn		
TMDS TRM	high z			70 ohm pullup			
RXS+							
RXS-							
0:0 90	.928.286 0:	0:1.500.074.366	0:0:1.509 Time (H:M:S	0.273.315 S.ms.us.ns)	0:0:1.518.472.263	0:0:1.527.671.211	
TimeStamp		Туре	Description			•	
0:0:1.03	36.414.600	CBUS LVL	HIGH (0:0:0.02	1.114.600)			
0:0:1.03	36.414.600	PULSE	wake group 1 h	igh 2		61	
0:0:1.05	57.529.200	CBUS LVL	LOW (0:0:0.062	.579.200)			
0:0:1.05	57.529.200	PULSE	wake inter-gro	up low			
0:0:1.12	20.108.400	CBUS LVL	HIGH (0:0:0.02	1.095.450)			
0:0:1.12	20.108.400	PULSE	wake group 2 h	igh 1			
0:0:1.141.203.850 CBUS LVL			LOW (0:0:0.021	.113.670)			
0:0:1.14	1.203.850	PULSE	wake group 2 1	wo.			
0:0:1.16	52.317.520	CBUS LVL	HIGH (0:0:0.02	1.115.110)			
0:0:1.16	52.317.520	PULSE	wake group 2 h	igh 2		$\odot$	
Events	🔯 Find						

# 6.5 General Controls – CBUS Log Plot

The various other icons and controls in the **CBUS Log Plot** are described in the tables and screens that follow. There are two tables below, one describing the icons on the top and a second table describing the items on the bottom of the **CBUS Log Plot**.

CBUS Log Plot Icons – Upper Status Section	Function
Icons – General Control	<ul> <li>User path status Date: MHL_CBUS_20_121105\3_3_10_101 — shows the name of the capture file and its location.</li> <li>Rows Rows — The Rows activation button enables you to configure the data types that appears in the CBUS Log Plot window. When you click on this icon a dialog box appears enabling you to configure the rows. This dialog box is described further below.</li> <li>Segment – Large captures are broken into smaller distinct sections called segments to make them more manageable and to improve speed and performance. When you click on the Segment activation button, a dialog box appears enabling you to select and load another segment. In the example to the left, there are no segments to the button is grayed out (as shown in the example).</li> </ul>

## 6.5.1 Configuring Row Information on the CBUS Log Plot

You can customize the CBUS events that appear on the **CBUS Log Plot** Row using the Row configuration dialog. The default configuration is shown below. Simply check the additional items that you wish to show in the **CBUS Log Plot**. Then click OK.

Row Selection	
Row Selection	
Select the rows to display in the Event Plot.	
PASS Test Pass Id	
PACKET     Packet Annotation	
CBUS L/V CBUS Level (High or Low) and Voltage (V).	l
PULSE     Pulse Annotation	
CBUS DRV CBUS Driver (Tester or DUT)	
VBUS DRV VBUS Driver (Tester or DUT)	
VBUS LVL VBUS Level	
CBUS TRM CBUS Termination	
TMDS TRM TMDS Termination	
RXS+ RxSense+ (High or Low)	
RXS- RxSense- (High or Low)	
Cther All other logged events.	
Cancel	
- curce	

The various other icons and controls in the CBUS Log Plot are described in the tables and screens that follow.

CBUS Log Plot Icons – Bottom Status Section			Fu	Inction
Icons - General (         0:0:48.701.894.720         0:0:48.701.894.720         0:0:48.701.894.800         0:0:48.701.894.850         0:0:48.702.134.030         0:0:48.702.134.330         0:0:48.702.134.330         Image: Second Se	CBUS LVL CBUS TRM TMDS TRM CBUS DRV CBUS LVL PULSE	HIGH (0:0:0.000.239.610) 100 k-ohms pulldown 70 ohm pullup Tester is driving CBUS LOW (0:0:0.000.001.050) Sink arbitrates (case 3)	-	Events — The Events activation button enables you to filter the captured data by type. When you click on the Events button a dialog box appears enable you do select or deselect data types individually or a page at a time. This dialog box is described further below. Find — The Find activation button enables you to locate captured data by type. When you click on the Find button a dialog box appears enable you do specify

CBUS Log Plot Icons – Bottom Status Section	Function
	a data type to search on. This dialog box is described further below.

### 6.5.2 Filtering Events on the CBUS Log Plot

You can filter the CBUS events that appear on the **CBUS Log Plot** using the **Event** button and associated dialog box. Simply click on the **Event** button and check the event types on the dialog box that you wish to view on the **CBUS Log Plot**. Then click OK. The screen examples below depict an Event filter scenario.

👍 Event Plo	t 🕂 CBUS Plot 🛛	📃 CT Results							
Data: MHL_C	BUS_2.0_121105\6_3_11_2	2_01							
Rows     Rows	Segment								
	200m %:	0.003	Q	🔽 Mark	er 1 💽 💿	▶ 🗸	Marker 2	3 • 🗗	
0:0:48.692.86	5.664								
ſ									
ſ									
PASS				F	ass 13				
PACKET									
CBUS L/V									
PULSE	wake	to discover low							
CBUS DRV		DUT		/00000		DUT		DUT	
VBUS DRV				Tester					
VBUS LVL									
CBUS TRM	100	0 ohms pulldown		100 k-ohms pulldown					
TMDS TRM		high z		CBUS Event Selection					
RXS+					Type Count Description				
RXS-				CBUS LVL 130215 CBUS L			CBUS Lev	vel (High or Low).	
10,0				C C	BUS DRV	18635	CBUS Dri	iver (Tester or DUT)	
0:0:48.686	5.301.146 0:	0:48.694.311.245			CBUS V 0 CBUS Voltage (V)			ltage (V)	
TimeChanne		Time	D	C C	BUS TRM	723	CBUS Ter	mination	
Timestamp	C 05C C50	Туре	Descri		MDS TRM	482	TMDS Ter	mination	
0:0:1.50	6.956.650	CBUS IVI	LOW		PULSE	85435 Pulse Appotation		notation	6
0:0:1.50	6.957.650	CBUS LVL	HIGH		PACKET 5621 Packet A		Annotation		
0:0:1.50	6.957.650	PULSE	0		RXS+	0	RxSenset	RySenset (High or Low)	
0:0:1.50	6,958,660	CBUS LVL	LOW		RXS-	0	RxSense-	RxSense- (High or Low)	
0:0:1.50	6.958.660	PULSE	0	v v	BUS LVL	0	VBUS Lev	VBUS Level	
0:0:1.50	0:0:1.506.959.650 CBUS LVL HIGH				PASS	241	Test Pas	s Id	
0:0:1.50	6.959.650	PULSE	0		Other	0	All othe	er logged events.	
0:0:1.50	6.960.660	CBUS LVL	LOW						
0:0:1.50	6.960.660	PULSE	0		Select /	All 🔳 Se	lect None	🗸 Ok 🙆 Cancel	$\odot$
Events	🔯 Find	1							

The resulting view is shown on the screen example below.

🗄 Event Plot 🔂 CBUS Plot 🕴 📃 CT Results 🗧 🗖								
Data: MHL_CBUS_2.0_121105\6_3_11_2_01								
Rows Segment								
A Coom %: 0.003 🔍 🔍 Marker 1 🗲 💿 🄁 🖉 Marker 2 🗲 💿 🄁								
0:7:0.807.234.481								
								1
PASS	Pass 13							
PACKET								
CRUSIA							<mark></mark>	
PULSE		wake to	discover low					
CBUS DRV	DUT				DUT		DUT	
VBUS DRV	Tester							
VBUS LVL								
CBUS TRM	CBUS TRM 1000 ohms pulldown				100 k-ohms pullde		ldown	
TMDS TRM	1 high z			70 ohm pullup			up	
RXS+				^				
RXS-								
0:0:48.686.301.146 0:0:48.694.311.245 0:0:48.702.368.741 0:0:48.710.426.237 0:0:48.718 Time (H:M:S.ms.us.ns)							483.733	
TimeStamp Type			Туре	Description				
0:0:3.50	07.753.550	D	CBUS DRV	DUT is drivi	ng CBUS			(1)
0:0:3.507.757.180			CBUS DRV	Tester is driving CBUS				्
0:0:3.507.771.180			CBUS DRV	DUT is driving CBUS				
0:0:3.507.781.180 CBUS DE			CBUS DRV	Tester is driving CBUS				
0:0:3.507.781.480 PACKET			PACKET	Sink -> Source <msc get_msc_errorcode=""></msc>				
0:0:3.507.782.580 CBUS			CBUS DRV	DUT is driving CBUS				
0:0:3.507.786.210			CBUS DRV	Tester is driving CBUS				
0:0:3.507.800.210 CBUS DR			CBUS DRV	DUT is driving CBUS				
0:0:3.507.810.210 CBUS DRV			Tester is driving CBUS					
U:U:3.507.810.510 PACKET			Sink -> Source <msc get_msc_errorcode=""></msc>				$\odot$	
Events 🔁 Find								

### 6.5.3 Finding Events on the CBUS Log Plot

You can locate specific CBUS events in the **CBUS Log Plot** using the **Finnd** button and associated dialog box. Simply click on the **Find** button and check the event type and text string on the dialog box for the Event that you looking for on the **CBUS Log Plot**. Then click OK. The screen examples below depict an Event filter scenario.
January 30, 2012

🗄 Event Plot 🚰 CBUS Plot 🕱 📜 CT Results 📃 🗖													
Data: MHL_CBUS_2.0_121105\6_3_11_2_01													
Rows Egment													
	🖑 🔍 Zoom	n %: 0.003 🤇	🔾 🔍 📝 Marker	1 🗲 💿 🖡	Marker 2 🧲	• •							
0:0:9.468.597.806													
ſ				Find CBUS Event									
ſ				V Type(s):									
					CBUS LVL	CBUS DRV	CBUS V						
PASS			Pas	s 3	CBUS TRM	TMDS TRM	VBUS DRV						
PACKET					PULSE	<b>PACKET</b>	RXS+						
CBUS L/V					RXS-	VBUS LVL	PASS						
PULSE	w	ake to discover low		🔲 Other									
CBUS DRV	DUT				Description contains text:								
VBUS DRV			Te	ster	ABORT								
VBUS LVL													
CBUS TRM		1000 ohms pulldown			Nearest to Time (n	s):	Grab Selected						
TMDS TRM			0										
RXS+						Found							
RXS-						🕂 Find Next	💢 Close						
0:0:9.463.810.706 0:0:9.4		0:0:9.471.820.805	0:0:9.479 Time (H:M:S	9.878.301 S.ms.us.ns)	0:0:9.487.935.	797 0:0	:9.495.993.293						
TimeStamp		Туре	Description				•						
0:0:0.30	0.227.310	PASS	Pass 1				(2)						
0:0:0.300.227.310 CBUS LVL		CBUS LVL	HIGH (0:0:0.050.006.130)										
0:0:0.300.227.310 CBUS DRV		CBUS DRV	DUT is driving CBUS										
0:0:0.300.227.310 CBUS TRM		high z											
0:0:0.300.227.310 TMDS TRM		high z											
0:0:0.300.227.310 VBUS DRV			DUT 1s driving VBUS										
0:0:0.350.233.060 VB0S DRV			1000 ohma pulldorm										
0:0:0.350.233.440 CBUS LVL			LOW (0:0:0.648.013.690)										
0:0:0.998.247.130 CBUS LVL			HIGH (0:0:0.021.126.170)										
🗵 Events	🔯 Find												

The result is shown on the screen example below.

🗄 Event Plot 🔂 CBUS Plot 🕴 📘 CT Results 📃 🗖												
Data: MHL_CBUS_2.0_121105\6_3_11_2_01												
Rows Segment												
	- 🖑 🔍 Zoom %:	0.003	🔍 🔍 🛛 🛛 Marker 1		Marker 2 🗲	● ₽						
0:0:5.533.242	2.044											
			🙀 Find CBUS Event									
					V Type(s):							
PASS			Pase	:2	CBUS LVL	CBUS DRV	CBUS V					
					CBUS TRM	TMDS TRM	VBUS DRV					
PACKET					PULSE	<b>PACKET</b>	RXS+					
CBUS L/V					RXS-	VBUS LVL	PASS					
PULSE	wake to discover low				Other							
CBUS DRV	DUT				✓ Description contains text:							
VBUS DRV			Tes	ter	ABORT							
VBUS LVL					— Newcette Time (n	-).	[[]]					
CBUS TRM	1000	ohms pulldown			Nearest to Time (in	s).	GITT SELECTED					
TMDS TRM		high z										
RXS+						Found						
RXS-					A Find Previous	🖑 Find Next	💢 Close					
0.0.5 505	274 126 0.0	5 522 204 225	0.0.5 541	441 721	0.0.5 540 400		5 553 556 300					
0:0:5.525	.374.136 0:0	:5.533.384.235	0:0:5.541 Time (H:M:S	.441.731 .ms.us.ns)	0:0:5.549.499.	227 0:0	:5.557.556.723					
TimeStamp	)	Туре	Description				•					
0:0:5.541.458.690 PULSE		PULSE	bit-ack									
0:0:5.541.459.050 CB		CBUS LVL	LOW (0:0:0.000.000.490)									
0:0:5.541.459.540 CBUS LVL			HIGH (0:0:0.000.005.890)									
U:U:5.541.465.430 CBUS LVL			LOW (0:0:0.000.004.530)									
0:0:5.541.465.430 PULSE		PACKET	Source applicates (case 4)									
0:0:5.541.469.960 CBUS LVL			HIGH (0:0:0.000.001.210)									
0:0:5.541.471.170 CBUS LVL			LOW (0:0:0.000.001.660)									
0:0:5.541.471.170 PULSE			Sync pulse									
0:0:5.541.472.830 CBUS LVL			HIGH (0:0:0.000.000.610)									
Events G Find												

## 6.6 Working with Markers

and right arrows associated with each marker

The **CBUS Log Plot** panel enables you to view the events at a high level and identify points of interest for further analysis. You can set two cursors or "markers" in the **Plot** at particular points of interest. The **CBUS Log Plot** will show you the time difference between the two cursors. You can fine tune the position of the cursors with the left



center icon allows you to

center the particular marker on the **CBUS Log Plot** window. The screens below show the markers being set and the resulting markers placed in the **CBUS Log Plot** panel. Note that you can also set the markers using the right

click menu also shown below and this is the preferred method because the markers will appear exactly where you right click.

You can see the timestamp associated with each marker which are color coded (blue and red) just above the area where the data is shown. The dark text to the right shows the difference in microseconds and pixels between the two markers. Examples are shown in the following two screen shots.





