



980 HDMI 300MHZ PROTOCOL ANALYZER MODULE

NEW! Now supports HDMI 2.0 & HDCP 2.2 Compliance Tests



The 980 HDMI 300MHz Protocol Analyzer module can be equipped in any of the 980 Advanced Test Platforms: 1) 980, 2) 980B (shown above) or 3) 980R. It is equipped in the 980 platform as a standard feature and can optionally be equipped in the 980B or 980R.

The 980 HDMI Protocol Analyzer module is equipped with an HDMI Rx and an HDMI Tx port. The HDMI Rx analyzer port provides full visibility into the HDMI and MHL protocol, metadata, timing, control and auxiliary data at HDMI 1.4b speeds. The module offers analysis of HDMI and MHL source devices as well as compliance testing for HDMI and MHL source and sink devices. For HDMI, the 980 HDMI Protocol Analyzer module operates at TMDS clock rates up to 300MHz to support 4K-capable source devices.

“DEEP ANALYSIS” DIAGNOSING INTEROPERABILITY PROBLEMS

The 980 HDMI 300MHz Protocol Analyzer provides the deep analysis and compliance test features necessary to enable you to get your product to market more quickly and with reduced expense. Deep analysis enables you to identify and resolve interoperability problems early in the product life cycle. The 980 HDMI Protocol Analyzer captures and decodes encrypted or unencrypted metadata (protocol data, audio sample, infoframes and other data islands) as well as HDMI DDC and MHL C-Bus transactions and HDMI CEC messages. Unlike competing analyzers for HDMI and MHL protocol testing, the 980 captures all protocol data, data islands and control packets with accurate timestamps even when they are transmitted in rapid succession.

COMPLIANCE PRE-TESTING AND SELF-TESTING

The comprehensive suite of HDMI 1.4b, 2.0 and MHL 1.2, 1.3, 2.0 & 2.1 compliance test tools for sources, sinks, dongles (MHL). Compliance tests supported for HDMI 2.0 include 4:2:0 pixel encoding for sources and sinks and EDID and Read Request testing for HDMI 2.0 sinks. Compliance tests are ideal for pre-testing your product prior to submission to an Authorized Test Center (ATC) for approval. Pre-testing provides added assurance that your product will pass on the first submission to the ATC. Where permitted, the 980 HDMI Protocol Analyzer module can be used to self-test your product. Self-testing offers even greater benefits for time to market and cost reduction than pre-testing by avoiding submission to the ATC for approval. The module provides all the necessary raw data test results to demonstrate compliance. HDCP 1.4 source and HDCP 2.2 source, sink and repeater compliance test solutions are also offered as optional packages.

OPERATIONAL MODES

The 980 HDMI Protocol Analyzer module operates in one of two modes: Capture and Store or Real Time Monitoring. In the Capture and Store mode, the module captures and decodes either unencrypted or HDCP encrypted HDMI or MHL metadata. You can trigger a capture on a variety of conditions or events that occur in the various data types and on specific values of a data type. Once the data is captured, the 980 Manager presents the data in an easy to understand way through its GUI graphical user interface.

DATA PORTABILITY

Both the captured data as well as compliance test data can be stored permanently and disseminated to subject matter experts at other locations. The 980 test instrument is not required to view the test results. The results and logs can be viewed through the 980 GUI Manager which is free and available from the Quantum Data website.

REAL TIME MODE

The Real Time mode enables you to view the incoming video and select which type of data to view in real time. Infoframes and other data islands, control, timing data, HDCP and EDID transactions can all be viewed in real time. You can observe changes in these data as changes are made in the source device. Reference frames can be set for any data type to enable easy identification of changes. The 980s' built-in color touch screen provides a graphical user interface (GUI) to control the instrument and to view incoming video and data in the real time mode.

KEY FEATURES + BENEFITS

Data Island Decoding

Captures and decodes all metadata, control data, data islands, infoframes and auxiliary channel data, etc. Decodes audio sample packets—including the decoding of the Channel Status Bits and the control bits from HDMI and MHL streams up to 300MHz.

HDMI and MHL Protocol Decoding

Decodes protocol data such as guard bands and preambles. Enables diagnosing protocol compliance test failures. Operates up to 300MHz.

HDMI DDC Data Decoding

Decodes all DDC transactions including EDID reads and HDCP authentication. You can view HDCP registers in human readable text and pinpoint failures in authentication.

MHL C-Bus Data Monitoring

Enables monitoring of MHL C-Bus transactions either passively between an MHL source and an MHL sink or while emulating an MHL sink device.

Real Time Monitoring Mode

View and monitor the incoming video image and metadata using the new Real Time monitoring mode. You can monitor all the data island data including infoframes and the DDC transactions and MHL C-Bus transactions. Operates up to 300MHz.

Capture Playback

The Playback function enables you to make a capture from any HDMI or MHL source device and play it back to an HDMI or MHL sink device under test. Operates up to 300MHz pixel rate.

Passive Monitoring

Captures and decodes video, metadata, control data and protocol data passively between a source and a sink device up to 300MHz if the content from the source is not HDCP encrypted. If the source content is encrypted, only the DDC, CEC, MHL C-Bus and timing parameters are captured.

Encrypted Link Analyzer (Optional Feature)

Monitor or capture and analyze HDCP encrypted protocol data transmitted between a source device and sink device up to 300MHz. All metadata, audio and timing data can be monitored or captured even when the content from the source is encrypted with HDCP content protection.

HDMI Source Compliance Test (Optional Feature)

Supports testing of HDMI source devices for compliance to Sections 7.4 (Protocol), 7.5 (Video), 7.6 (Audio), 7.7 (DVI) and 7.8 (Advanced) of the HDMI CTS 1.4. The 980 source compliance test is an ideal solution for pre-testing and/or self testing and enables you to get your source product to market more quickly and to reduce the expense of testing at the ATC.

HDMI HDCP Source Compliance Test (Optional Feature)

Supports testing of HDCP compliance testing for source devices in accordance with HDCP CTS 1.2.

HDMI Sink Compliance Test (Optional Feature)

Supports testing of HDMI sinks for compliance to Sections 8.2 (EDID), 8.4 (Protocol), 8.5 (Video), 8.6 (Audio), 8.7 (Interoperability with DVI), 8.8 (Advanced) of the HDMI 1.4 Compliance Test Specification (CTS). The 980 sink compliance test is an ideal solution for pre-testing and/or self testing and enables you to get your sink product to market more quickly and to reduce the expense of testing at the ATC.

HDMI 2.0 Source Compliance Test for 4:2:0 Pixel Encoding (Optional Feature)

Supports compliance testing of HDMI 2.0 4K & 4:2:0-capable sources per HDMI 2.0 CTS.

HDMI 2.0 Sink Compliance Test for 4:2:0, EDID, Read Request (Optional Feature)

Supports compliance testing of HDMI 2.0 EDID, 4:2:0, Read Request tests for sinks per HDMI 2.0 CTS.

NEW! HDMI 2.0 Sink Compliance Test for Read Request (Optional Feature)

Supports compliance testing of HDMI 2.0 sinks supporting read request per HDMI 2.0 CTS.

MHL Source Compliance Test (Optional Feature)

Supports testing of MHL source devices for compliance to Section 3 of the MHL 1.2, 1.3, 1.4, 2.0, 2.1 and 2.2. Compliance Test Specification (approved by MHL consortium). The 980 MHL source compliance test is an ideal solution for pre-testing (and/or self testing where permitted) and enables you to get your MHL source device to market more quickly and to reduce the expense of testing at the ATC.

MHL Sink Compliance Test (Optional Feature)

Supports testing of MHL sink/dongle devices for compliance to Sections 4 and 5 of the MHL 1.2, 1.3, 1.4, 2.0, 2.1 and 2.2 Compliance Test Specification (approved by MHL consortium). The 980 MHL sink and dongle compliance test solution is ideal solution for pre-testing your MHL sink or dongle device prior to submitting to the MHL ATC for approval. **Note:** Quantum Data 882 required.

HDCP 2.2 Source and Sink Functional Test

Verify an HDMI source and sink's HDCP 2.2 authentication capabilities.

NEW! HDCP 2.2 Source, Sink Repeater Compliance Test

Test HDMI sources, sinks and repeaters for compliance to HDCP 2.2 CTS.

Data Portability

Data portability enables you to share capture data and compliance test results with colleagues, subject matter experts at other corporate locations and other experts for analysis and for verifying compliance. The 980 test instrument is not required to view the test results. The data can be viewed through the 980 GUI Manager which is free and available from the Quantum Data website.

Triggering and Pre-capture Filtering

Set up triggers on specific data island values and set pre-capture filtering to capture specific data.

Filtering of Data Transactions

Check box filtering allows you to remove data types you are not interested in. For example you can filter out all data islands except audio sample packets and audio infoframes to compare the respective values for sampling rate.

Searching Through Data

Search through the captured data to locate the specific occurrence of the data you are interested in.

Special Analysis Tests

Run special analysis tests to verify timing, video, audio sampling and AVmute at the touch of a button.

Pixel Error Test

Test HDMI sources and HDMI distribution networks at the sink (downstream) with Pixel Error Test. Verify HDMI networks comprised of cables, audio/video processors, extenders, switches, repeaters, etc. once installed. Test for pixel errors on the TMDS video.

Pseudo-Random Noise Test

Test HDMI cables and distribution networks comprised of cables, audio/video processors, extenders, switches, repeaters, etc. using loopback configuration with Pseudo-Random Noise Test pattern.

HDMI CEC Data Decoding

View CEC messages for addressing, routing, one touch play, etc.

PRODUCT OPTIONS

HDMI Source Compliance

Specification	HDMI CTS 1.4b
Test Sections	Section 7.4 (Protocol) Section 7.5 (Video) Section 7.6 (Audio) Section 7.7 (DVI) Section 7.8 (Advanced Features)

HDMI Sink Compliance

Specification	HDMI CTS 1.4b
Test Sections	Section 8.2 (EDID / E-DDC) Section 8.4 (Protocol) Section 8.5 (Video) Section 8.6 (Audio) Section 8.7 (Interoperability with DVI) Section 8.8 (Advanced Features)

HDMI 2.0 Compliance

Specification	HDMI CTS 2.0 MOIs
Package #1	4:2:0 Pixel Encoding (source & sink)
Package #2	EDID & Read Request (sink)

HDMI HDCP Source Compliance

Specification	HDCP CTS 1.2 (source) & HDCP 2.2 (source, sink and repeaters)
Test Sections	Sections 1A & 1B.(Source Testing)

MHL Source Compliance

Specification	MHL CTS 1.2 & (1.3 approved) MHL CTS 2.0 & 2.1 approved
Test Sections	Sections 3 & 6

MHL Sink/Dongle Compliance

Specification	MHL CTS 1.2 & (1.3, 1.4 approved) MHL CTS 2.0, 2.1 & 2.2 approved
Test Sections	Section 4, 5 & 6

Encrypted Link Analyzer

Monitor or capture and analyze HDCP encrypted protocol data transmitted between a source device and sink device.

HDCP 2.x Functional Tests for sources and sinks

Verify a sources or a sinks HDCP 2.2 authentication on HDMI 1.4x devices.

PROTOCOL ANALYZER MODULE CONNECTORS

HDMI Rx

Function	HDMI input (analyzer)
Connector	One (1) HDMI Type A
Pixel/TMDS Rate	300 MHz; 3.00 Gb/s (per pair)
Minimum Time Resolution	2.5x10 ⁻⁹

Video

Encoding	RGB, YCbCr
Sampling modes	4:4:4, 4:2:2, 4:2:0 (per HDMI 2.0)
Bits/component	24/30/36-bit RGB or YCbCr 16/20/24-bit 4:2:2 YCbCr

Note: 30 and 36 bit Deep Color is supported at TMDS rates up to 3.00Gb/s.

HDMI / MHL Tx

Function	HDMI / MHL output (pass-through)
Connector	One (1) HDMI Type A
TMDS max rate	300MHz; 3.00 Gb/s

Video

Encoding	RGB, YCbCr
Sampling modes	4:4:4 or 4:2:2
Bits/component	24/30/36-bit RGB or YCbCr 16/20/24-bit 4:2:2 YCbCr

Ethernet (2)

Function	HDMI Ethernet Channel
Connector	RJ-45

980/980B PLATFORM CONNECTORS/SPECIFICATIONS

SPDIF IN

Function	Audio Return Channel receive for HDMI source
Connector	RCA

SPDIF OUT

Function	Audio Return Channel transmit for HDMI sink
Connector	RCA

TRIG IN

Function	External Trigger input C-Bus pass-through monitoring
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Memory

Size	4 GB
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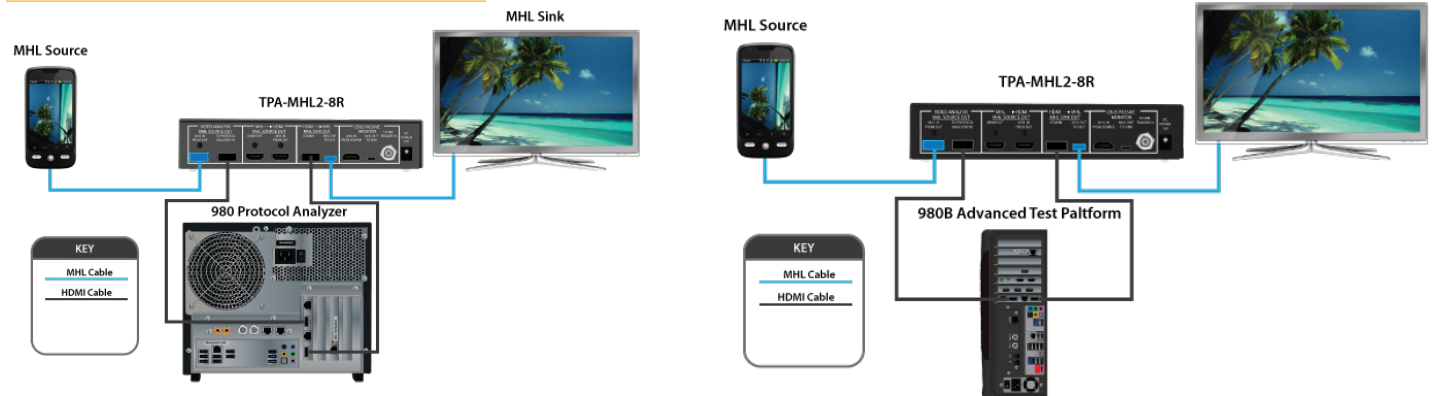
Administration

Ethernet (RJ-45) for external GUI Manager
800 pixels by 600 lines color touch screen display for embedded GUI Manager

HDMI Setups - Source Analysis & Pass-through



MHL Setups - Source Analysis & Pass-through (1.2, 1.3, 2.0, 2.1)



Data Monitoring in Real Time

Operation is simple:

1. Select the Real Time Mode.
2. Enable real time monitoring
3. Select which metadata to view.
4. Configure image viewing parameters

HDMI & MHL Video

- View incoming video
- View video timing data

HDMI & MHL Metadata

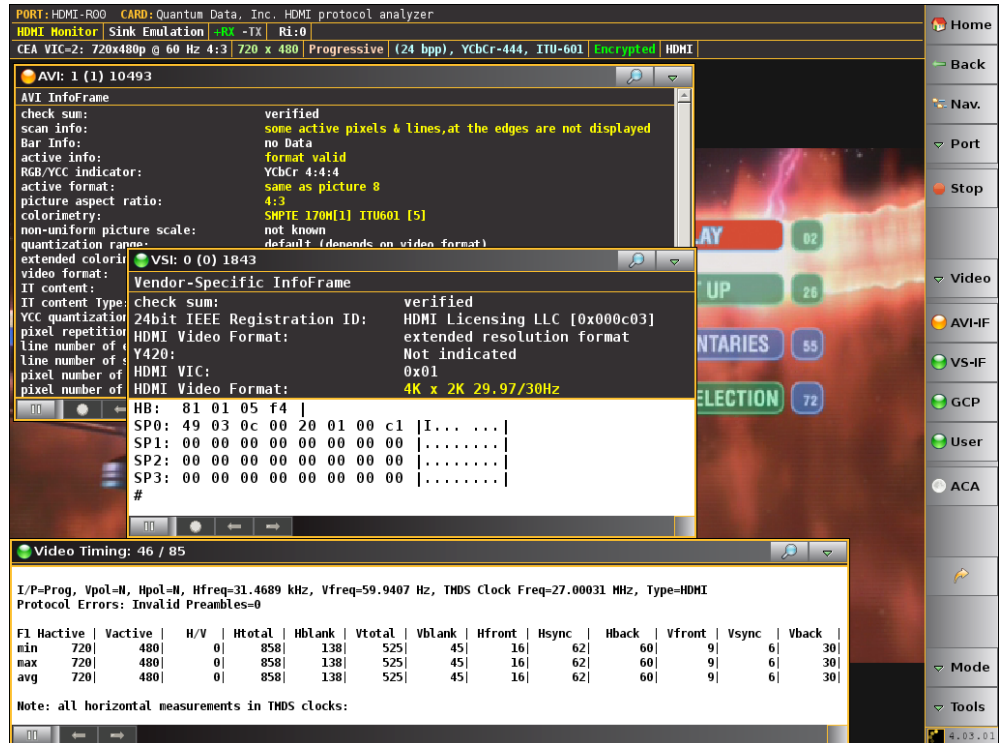
- AVI Infoframes
- Audio Infoframes
- Vendor Specific Infoframes
- Source Product Descriptor
- General Control Packets

HDMI DDC Traffic

- EDID transactions
- HDCP transactions

MHL C-Bus

- EDID transactions
- HDCP transaction



HDMI and MHL Source Analysis

Operation is simple:

1. Define the trigger and precapture filter criteria or start and stop capture under manual control.
2. Initiate the capture. When the trigger criteria is met the data is decoded and presented.
3. Navigate to specific data packets of interest in the Event Plot, Data Decode windows (shown below) or the Timing Analyzer or Video Analyzer windows (not shown below). The decoded data is presented in human readable text to facilitate rapid examination of data.

The screenshot displays the Capture Viewer software interface. The top section shows the Event Plot with a timeline of captured data. The Data Decode window below it provides a detailed view of the captured packets.

Packet	Time (H:M:S.ms.us.ns.ps)	Frame	Line	Pixel	Type	SubType	Info
12955	1:47:10.723.578.830.000	2	8	0	TMDS	HSYNC	HSYNC 88 clocks
12956	1:47:10.723.578.830.000	2	8	0	TMDS	VSYNC	VSYNC 55000 clocks
12957	1:47:10.723.578.870.000	2	8	11	TMDS	GCP	General Control Packet (GCP)
12958	1:47:10.723.578.977.742	2	8	43	TMDS	AVI IF	AVI InfoFrame
12959	1:47:10.723.579.085.485	2	8	75	TMDS	AUD IF	Audio InfoFrame
12960	1:47:10.723.579.193.226	2	8	107	TMDS	VEN	Vendor-Specific InfoFrame
12961	1:47:10.723.590.900.000	2	8	3584	TMDS	AUDSAM	Audio Sample Packet(L-PCM and IEC 61937 compressed formats)
12962	1:47:10.723.597.350.000	2	9	0	TMDS	HSYNC	HSYNC 88 clocks

Below the table, the following metadata is displayed:

```

RGB/YCC indicator:      RGB
active format:         not defined
picture aspect ratio:  16:9
colorimetry:          No Data
non-uniform picture scale: no known
quantization range:   default (depends on video format)
IT content:           no data
video format:         VIC=0 (No Video Identification Code Available)
pixel repetition:     none
line number of end of top bar: 0
line number of start of bottom bar: 2161
pixel number of end of left bar: 0

```



HDMI 1.4 Source Compliance Tests

Operation is simple:

1. Define the capabilities of the source device under test using the CDF forms.
2. Select the HDMI 1.4 Compliance Tests you wish to run.
3. Initiate the test suite.
4. View the test results, detail and summary.

HDMI 1.4 CTS Tests supported:

Section 7.4: Source Protocol Tests

- Test ID 7-16: Legal Codes
- Test ID 7-17: Basic Protocol
- Test ID 7-18: Extended Control Period
- Test ID 7-19: Packet Types

Section 7.5: Source Video Tests

- Test ID 7-21: Minimum Format Support
- Test ID 7-22: Additional Format Support
- Test ID 7-23: Pixel Encoding – RGB to RGB-only Sink
- Test ID 7-24: Pixel Encoding – YCbCr to YCbCr Sink
- Test ID 7-25: Video Format Timing
- Test ID 7-26: Pixel Repetition
- Test ID 7-27: AVI InfoFrame

Section 7.6: Source Audio Tests

- Test ID 7-28: IEC 60958/IEC 61937
- Test ID 7-29: ACR
- Test ID 7-30: Audio Sample Packet Jitter
- Test ID 7-31: Audio InfoFrame
- Test ID 7-32: Audio Sample Packet Layout

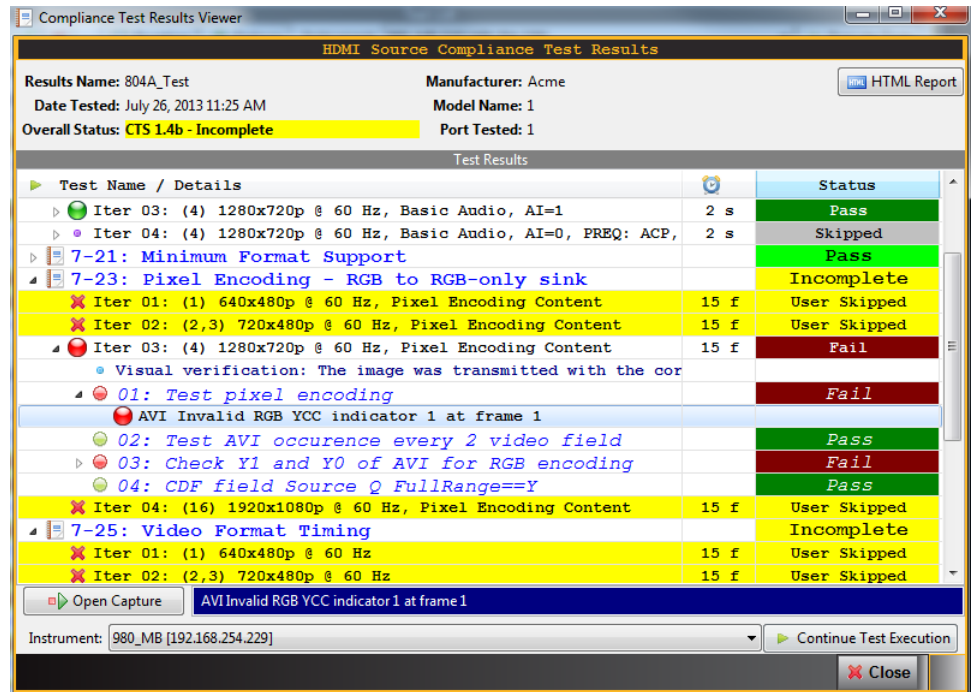
Section 7.7: Source Interoperability with DVI

- Test ID 7-33: Interoperability with DVI

Section 7.8: Source Advanced Features

- Test ID 7-34: Deep Color
- Test ID 7-35: Gamut Metadata Transmission
- Test ID 7-36: High-Bitrate Audio
- Test ID 7-37: One Bit Audio
- Test ID 7-38: Video Format Timing
- Test ID 7-39: 4K x 2K Video Format*
- Test ID 7-40: Extended Colorimetry Transmission (without xvYCC)

*Approved for use in ATC per CTS version 1.4



HDMI Sink Compliance Tests for HDMI 1.4

Operation is simple:

1. Define the capabilities of the source device under test using the CDF forms.
2. Select the HDMI 1.4 Compliance Tests you wish to run.
3. Initiate the test suite.
4. View the test results, detail and summary.

HDMI 1.4 CTS Tests supported:

Section 8.2: Sink – EDID / E-DDC

- Test ID 8-1: EDID Readable
- Test ID 8-2: EDID VESA Structure
- Test ID 8-3: EDID CEA Timing Extension Structure

Section 8.4: Sink - Protocol

- Test ID 8-15: Character Synchronization
- Test ID 8-16: Acceptance of Valid Packet Types

Section 8.5: Sink - Video

- Test ID 8-17: Basic Format Support Requirements
- Test ID 8-18: HDMI Format Support Requirements
- Test ID 8-19: Pixel Encoding Requirements
- Test ID 8-20: Video Format Timing

Section 8.6: Sink - Audio

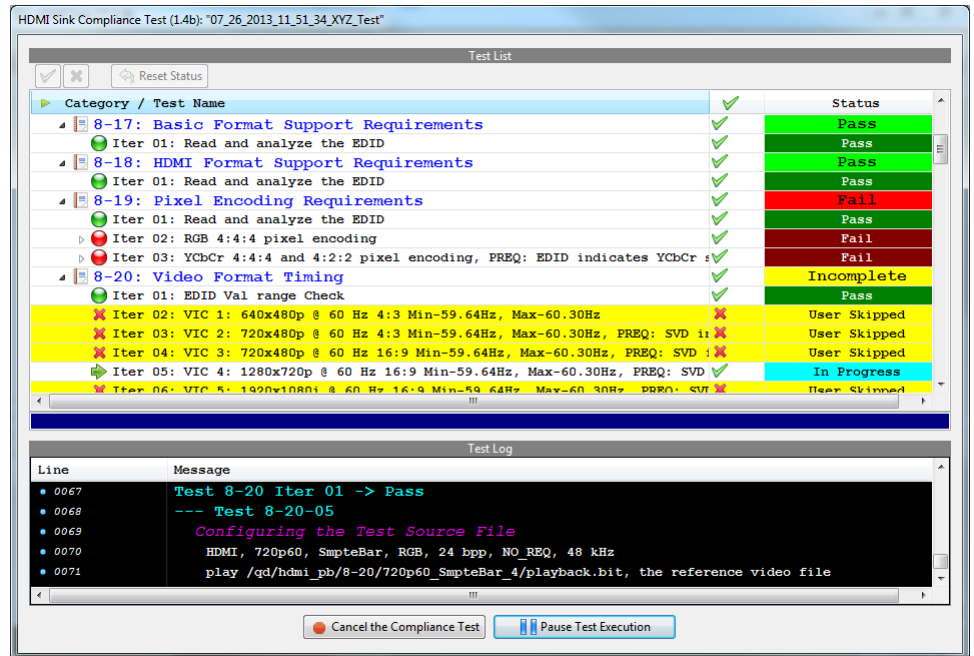
- Test ID 8-21: Audio Clock Regeneration
- Test ID 8-23: Audio Formats

Section 8.7: Sink - Interoperability with DVI

- Test ID 8-24: Interoperability with DVI

Section 8.8: Sink - Advanced Features

- Test ID 8-25: Deep Color
- Test ID 8-27: High Bitrate Audio (requires 882E/EA)
- Test ID 8-29: 3D Video Format Timing
- Test ID 8-30: 4K by 2K Video Format Timing
- Test ID 8-31: AVI Infocode, YCC Quantization Range



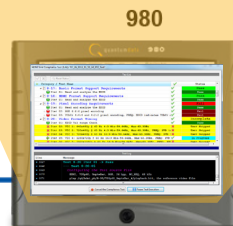
PC
w/ 980 GUI Manager



Ethernet Cable



Ethernet Cable



HDMI Cable



Sink

HDMI Compliance MOIs for HDMI 2.0

Operation is simple:

1. Define the capabilities of the source device under test using the CDF forms.
2. Select the HDMI 1.4 Compliance Tests you wish to run.
3. Initiate the test suite.
4. View the test results, detail and summary.

HDMI 2.0 CTS Test MOIs supported - Package 1:

Source Tests:

- Test ID HF1-31: Source Pixel Encoding YCbCr 4:2:0
- Test ID HF1-33: Source Video Timing - YCbCr 4:2:0
- Test ID HF1-51: Source AVI Infoframe - YCbCr 4:2:0

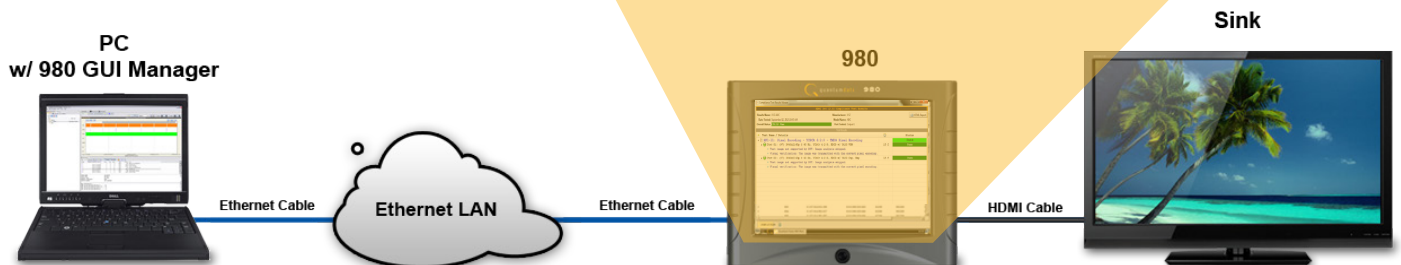
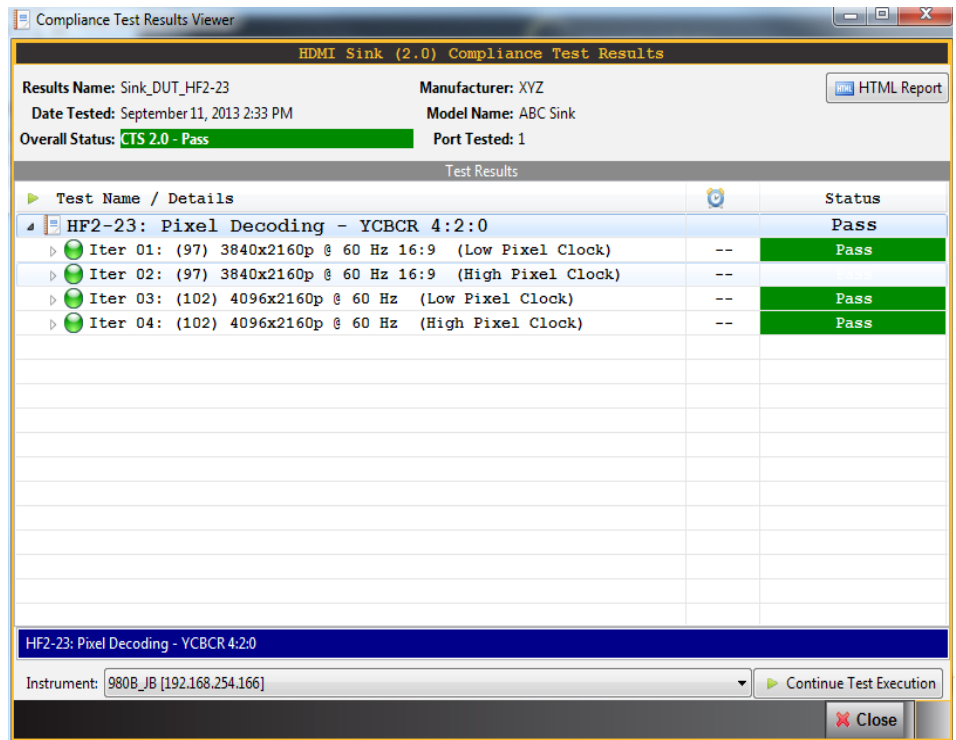
Sink Tests:

- Test ID HF2-23: Sink Pixel Decoding - YCbCr 4:2:0
- Test ID HF2-31: Sink EDID - YCbCr 4:2:0

HDMI 2.0 CTS Test MOIs supported - Package 2:

Sink Tests:

- Test ID HF2-10: Sink Video Timing – 6G – HF-VSDB
- Test ID HF2-12: E-DDC - Read Request Enable Verify
- Test ID HF2-16: E-DDC - Read Request Test Config Register Reset
- Test ID HF2-26: Sink EDID – Video Format Declaration
- Test ID HF2-34: E-DDC - Read Request SCDC Update Flag Response
- Test ID HF2-35: Sink EDID YCBCR 4:2:0 Deep Color HF-VSDB
- Test ID HF2-44: E-DDC - Read Request SCDC Wait for Bus Free
- Test ID HF2-32: Sink EDID – YCBCR 4:2:0 BT.2020 – Data Block
- Test ID HF2-39: Sink EDID 3D and Multi-stream Audio Data Blocks
- Test ID HF2-41: Sink HDMI-VSDBs – Independent-View
- Test ID HF2-50: E-DDC - Read Request TestReadRequest and TestReadResponse
- Test ID HF2-53: Sink EDID HF-VSDB



HDMI HDCP 1.2 Source Compliance Tests

Operation is simple:

1. Define the capabilities of the source device under test using the CDF forms.
2. Select the HDMI HDCP 1.2 Compliance Tests you wish to run.
3. Initiate the test suite.
4. View the test results, detail and summary.

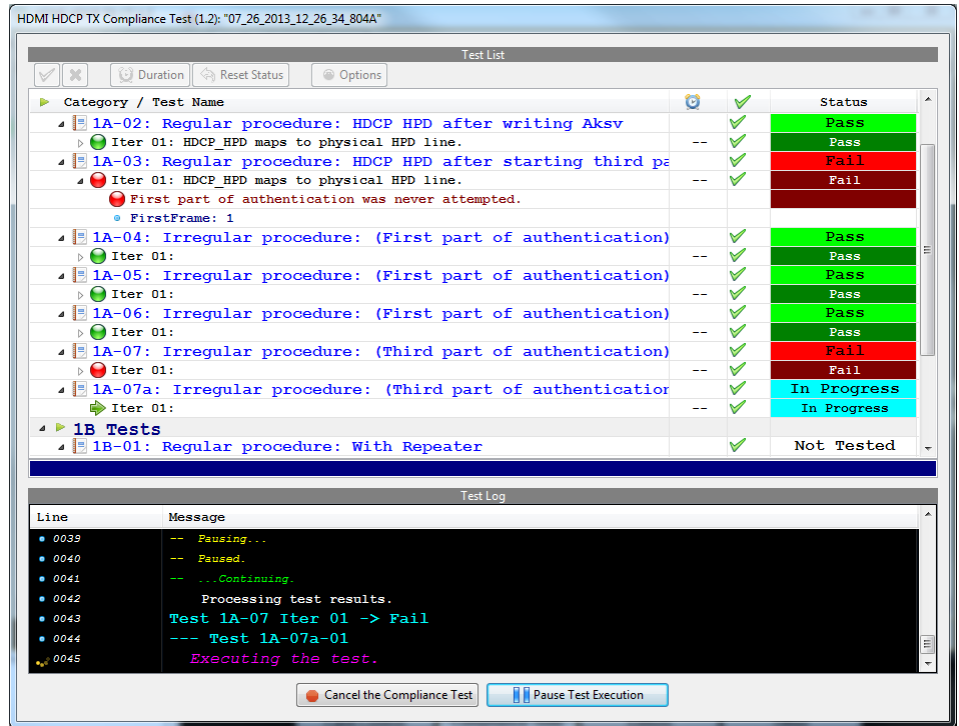
HDMI HDCP 1.2 CTS Tests supported:

Section 1A: Source Transmitter Downstream with HDMI Capable Receiver

- 1A-01: Regular Procedure: w/ HDMI Capable Receiver.
- 1A-02: Regular Procedure: HDCP_HPD After Writing Aksv.
- 1A-03: Regular Procedure: HDCP_HPD After Starting Third Part of Authentication.
- 1A-04: Irregular Procedure: (First Part Authentication) HDPC Port Access'.
- 1A-05: Irregular Procedure: (First Part Authentication) Verify Bksv.
- 1A-06: Irregular Procedure: (First Part Authentication) Verify R0'.
- 1A-07: Irregular Procedure: (Third Part Authentication) Verify Ri' (invalid Ri).
- 1A-07a: Irregular Procedure: (Third Part Authentication) Verify Ri' (Ri' not returned).
- 1A-08: Irregular Procedure: SRM. Requires SRM DVD disc.
- 1A-09: Regular Procedure: With DVI Receiver.

Section 1B: Source Transmitter Downstream with HDMI Capable Repeater

- 1B-01: Regular Procedure: w/ HDMI Capable Repeater
- 1B-02: Regular Procedure: HPD After Reading R0'
- 1B-03: Irregular Procedure: (Second Part of Authentication) Timeout of KSV List READY
- 1B-04: Irregular Procedure: (Second Part of Authentication) Verify V'
- 1B-05: Irregular Procedure: (Second Part of Authentication) MAX_DEVS_EXCEEDED
- 1B-06: Irregular Procedure: (Second Part of Authentication) MAX_CASCADE_EXCEEDED



HDMI HDCP 2.2 Source, Sink & Repeater Compliance Tests

Operation is simple:

1. Define the capabilities of the device under test using the CDF forms.
2. Select the HDMI HDCP 2.2 Compliance Tests you wish to run.
3. Initiate the test suite.
4. View the test results, detail and summary.

HDMI HDCP 2.2 CTS Transmitter (Source) Test Sections supported:

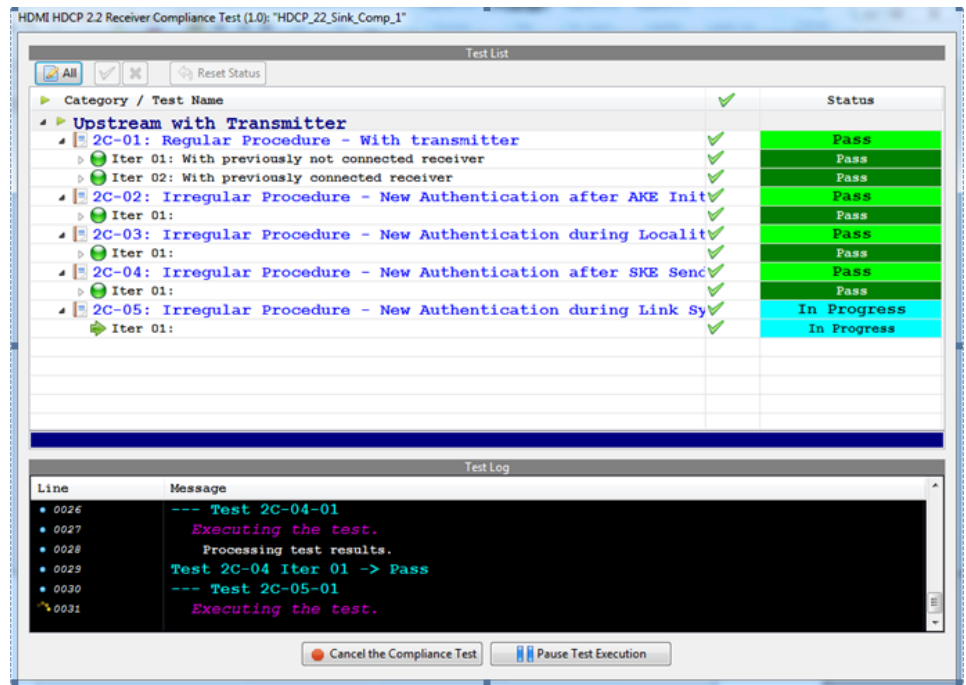
- Section 1A: Transmitter Downstream with Receiver with HDMI Capable Receiver (all tests supported)
- Section 1B: Transmitter with Downstream Repeater (all tests supported)

HDMI HDCP 2.2 CTS Receiver (Sink) Test Sections supported:

- Section 2C: Receiver Upstream with Transmitter (all tests supported)

HDMI HDCP 2.2 CTS Repeater Test Sections supported:

- Section 3A: Downstream Procedure with Receiver (all tests supported)
- Section 3B: Downstream Procedure with Repeater (all tests supported)
- Section 3C: Upstream Procedure with Transmitter (all tests supported)



HDMI 1.4 EDID Compliance Tests for HDMI 1.4

Operation is simple:

1. Define the capabilities of the sink device under test using the CDF forms.
2. Initiate the test suite.
3. View the test results, detail and summary.

HDMI CTS 1.4 Tests supported:

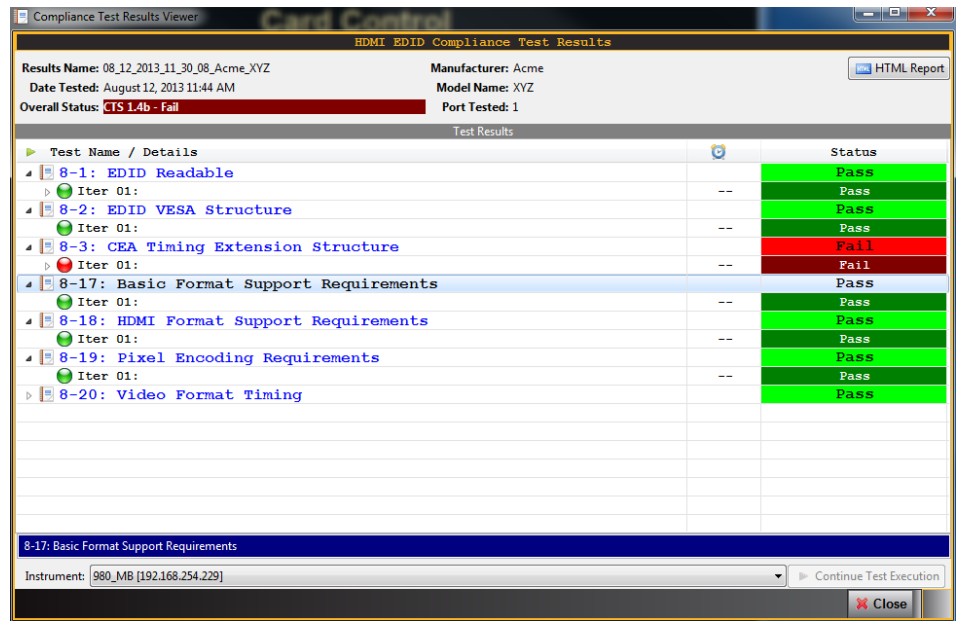
Section 8.2: Sink – EDID / E-DDC

- Test ID 8-1: EDID Readable
- Test ID 8-2: EDID VESA Structure
- Test ID 8-3: EDID CEA Timing Extension Structure

Section 8.5: Sink - Video

- Test ID 8-17: Basic Format Support Requirements
- Test ID 8-18: HDMI Format Support Requirements
- Test ID 8-19: Pixel Encoding Requirements*
- Test ID 8-20: Video Format Timing*

* Tests for Section 8.5 Sink - HDMI Sink Compliance Test option is required to fully cover 8-19 and 8-20 tests..



MHL CTS 1.2, 1.3, 2.0, 2.1 Source Compliance Tests Approved by MHL Consortium

Operation is simple:

1. Define the capabilities of the source device under test using the CDF forms.
2. Select the MHL Compliance Tests you wish to run: 1.2, 1.3, 2.0, 2.1.
3. Initiate the test suite.
4. View the test results, detail and summary.

MHL CTS 1.2, 1.3, 2.0 & 2.1 Source tests supported (unless otherwise indicated):

Section 3.2.2: TMDS Coding

- Test 3.2.2.1: Legal Codes Normal mode
- Test 3.2.2.2: Basic Protocol Normal mode
- Test 3.2.2.3: Packet Types Normal mode
- Test 3.2.2.4: Legal Codes PackedPixel mode (1.3, 2.0, 2.1)
- Test 3.2.2.5: Basic Protocol PackedPixel mode (1.3, 2.0, 2.1)
- Test 3.2.2.6: Packet Types PackedPixel mode (1.3, 2.0, 2.1)

Section 3.2.3: Video Modes

- Test 3.2.3.1: Video Formats Normal mode
- Test 3.2.3.2: Required Pixel Encoding Normal mode
- Test 3.2.3.3: AVI InfoFrame Normal mode
- Test 3.2.3.4: Video Quantization Ranges
- Test 3.2.3.5: Video Formats PackedPixel mode (1.3, 2.0, 2.1)
- Test 3.2.3.6: Pixel Encoding PackedPixel mode (1.3, 2.0, 2.1)
- Test 3.2.3.7: AVI InfoFrame PackedPixel mode (1.3, 2.0, 2.1)

Section 3.2.4: Audio Tests

- Test 3.2.4.1: IEC 60958 / IEC 61937
- Test 3.2.4.2: Audio Clock Regeneration
- Test 3.2.4.4: Audio InfoFrame

Section 3.2.6: EDID and Device Capability Register Test

- Test 3.2.6.3: Device Status Regs Normal mode (1.3, 2.0, 2.1)
- Test 3.2.6.4: Device Status Regs PackedPixel (1.3, 2.0, 2.1)

Section 3.2.8: RAP Sub-Command (All Tests) (1.3, 2.0, 2.1)

Section 3.2.9: 3D Tests

- Test 3.2.9.2: 3D Video Format Timings (2.0, 2.1)
- Test 3.2.9.3: 3D Video Mode Indicator (2.0, 2.1)

Section 3.2.10: UCP Sub-Command Tests (All Tests)

MHL Source CTS 1.2, 1.3, 2.0, 2.1 tests supported by 980 MHL CBUS Module (excepted where noted):

Section 3.1.1: Electrical Tests

- Test 3.1.1.13: Rx Sense Impedance

Section 3.2.6: EDID and Device Capability Register Test

- Test 3.2.6.1: EDID Reading Test
- Test 3.2.6.2: Device Capability Registers Test

Section 3.2.7: RCP Sub-command Test

Section 3.3: CBUS Tests (All tests in Sections 3.3.2 thru 3.3.23)

Section 3.2.9: 3D Tests

- Test 3.2.9.1: 3D Video Mode Support (3D Req) (2.0, 2.1)

Section 3.2.10: UCP Sub-Command Tests (2.0, 2.1)

Section 6: Common Tests (All tests in section 6.3.1 - 6.3.22)

MHL Source tests supported by 882EA:

Section 3.2.5: HDCP Test

Source
MHL DUT

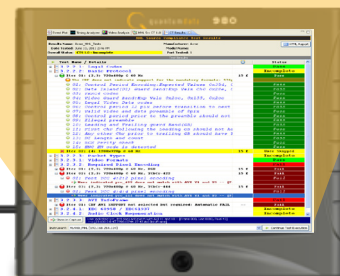


MHL Cable

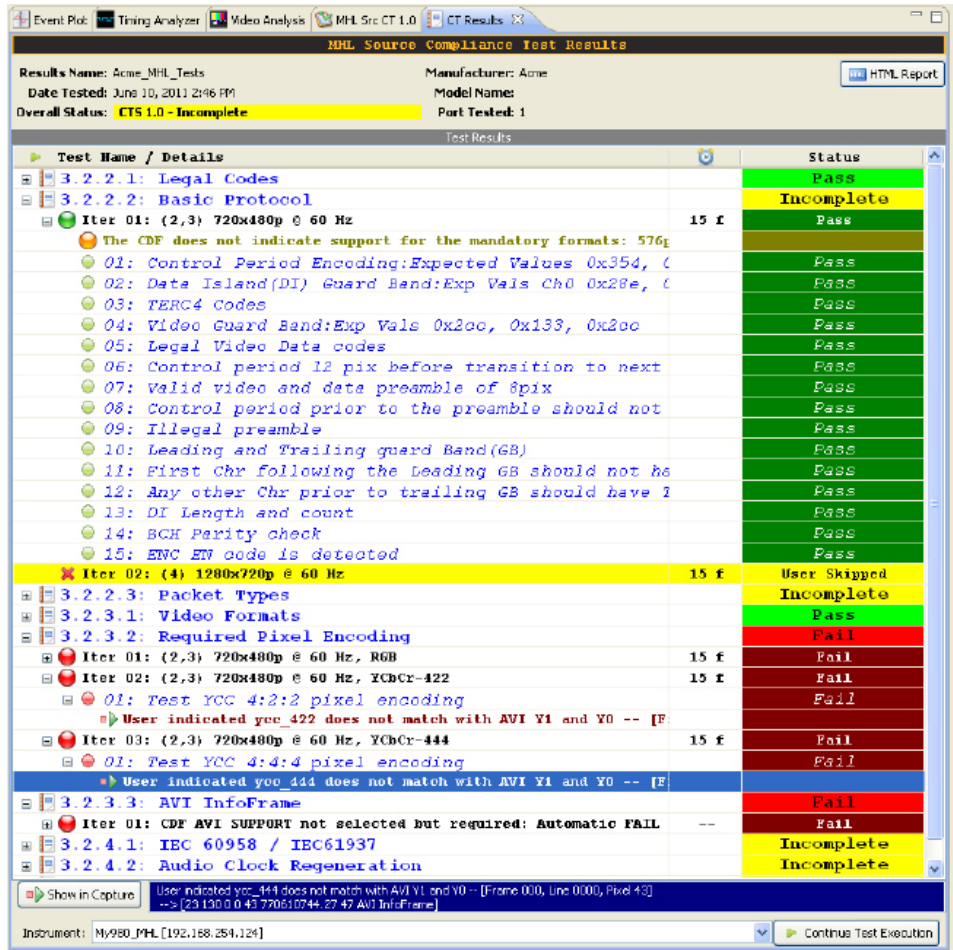
TPA-MHL-8R



HDMI Cable



980 Protocol Analyzer
and Compliance Tester



MHL CTS 1.2, 1.3, 2.0, 2.1 Sink Compliance Tests

Operation is simple:

1. Define the capabilities of the sink device under test using the CDF forms.
2. Select the MHL Compliance Tests you wish to run.
3. Initiate the test suite.
4. View the test results, detail and summary.

MHL CTS 1.2, 1.3, 2.0, 2.1 Sink tests supported (except where noted) (882EA required):

Section 4.2.1: System

- Test 4.2.1.1: Character Sync Normal mode
- Test 4.2.1.2: Packet Types Normal mode
- Test 4.2.1.3: Character Sync PackedPixel (1.3, 2.0, 2.1)
- Test 4.2.1.4: Packet Types PackedPixel mode (1.3, 2.0, 2.1)

Section 4.2.2: Video

- Test 4.2.2.1: Video Formats Normal mode
- Test 4.2.2.2: Pixel Encoding Normal mode
- Test 4.2.2.3: Video Quantization Ranges
- Test 4.2.2.4: Video Formats PackedPixel (1.3, 2.0, 2.1)
- Test 4.2.2.5: Pixel Encoding PackedPixel (1.3, 2.0, 2.1)

Section 4.2.3: Audio

- Test 4.2.3.1: IEC 60958 / IEC 61937
- Test 4.2.3.2: Audio Clock Regeneration

Section 4.2.7: RAP Sub-command tests (1.3, 2.0, 2.1)

Section 4.2.8: 3D Video Formats

- Test 4.2.8.2: 3D Video Formats Normal mode (2.0, 2.1)
- Test 4.2.8.3: 3D Video Formats PackedPixel (2.0, 2.1)

MHL CTS 1.2, 1.3, 2.0, 2.1 Sink tests supported by 980 MHL CBUS Module (except where noted):

Section 4.1.1: Electrical Tests

- Test 4.1.1.7: Rx Sense Impedance

Section 4.2.5: EDID and Device Capability Register Test

- Test 4.2.5.1: EDID Reading Test
- Test 4.2.5.2: Device Capability Registers Test
- Test 4.2.5.3: Device Status Registers Test (1.3, 2.0, 2.1)

Section 4.2.6: RCP Sub-command Tests

Section 4.2.8: 3D Video

- Test 4.2.8.1: 3D Mode Support (2.0, 2.1)

Section 4.2.9: UCP Sub-command Tests (2.0, 2.1)

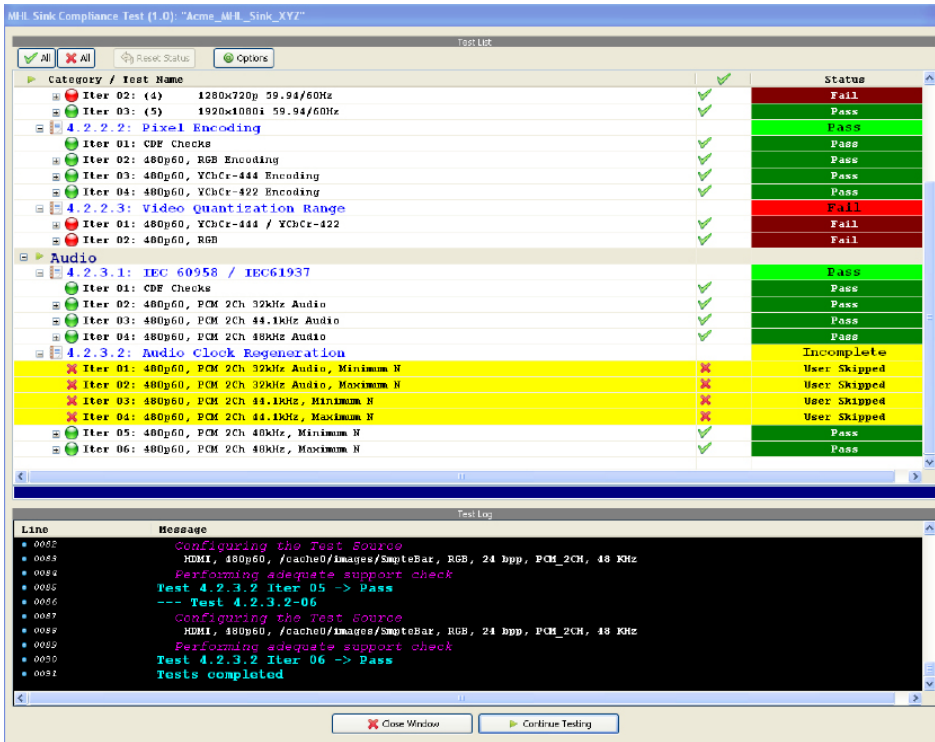
Section 4.3: CBUS Tests

(All tests in Sections 4.3.2 through 4.3.25)

Section 6: Common Tests (All tests in section 6.3.1 - 6.3.22)

MHL Sink tests supported by 882EA:

Section 4.2.4: HDCP Test



PC
w/ 980 GUI Manager



882EA

TPA-MHL-8R

MHL Sink DUT



MHL CTS 1.2, 1.3, 2.0, 2.1 Dongle Compliance Tests

Operation is simple:

1. Define the capabilities of the sink device under test using the CDF forms.
2. Select the MHL Compliance Tests you wish to run.
3. Initiate the test suite.
4. View the test results, detail and summary.

MHL CTS 1.2, 1.3, 2.0, 2.1 Dongle tests supported (except where noted) (882EA required):

Section 5.2.1: System

- Test 5.2.1.1: Character Sync Normal mode
- Test 5.2.1.2: Packet Types Normal mode
- Test 5.2.1.3: Character Sync PackedPixel mode (1.3, 2.0, 2.1)
- Test 5.2.1.4: Packet Types PackedPixel mode (1.3, 2.0, 2.1)

Section 5.2.2: Video

- Test 5.2.2.1: Video Formats Normal mode
- Test 5.2.2.2: Pixel Encoding Normal mode
- Test 5.2.2.3: Video Quantization Ranges
- Test 5.2.2.4: Video Formats PackedPixel mode (1.3, 2.0, 2.1)
- Test 5.2.2.5: Pixel Encoding PackedPixel mode (1.3, 2.0, 2.1)

Section 5.2.3: Audio

- Test 5.2.3.1: IEC 60958 / IEC 61937
- Test 5.2.3.2: Audio Clock Regeneration

Section 5.2.7: RAP Sub-command tests (1.3, 2.0, 2.1)

Section 5.2.8: 3D Video

- Test 5.2.8.2: 3D Video Formats (2.0, 2.1)
- Test 5.2.8.3: 3D Video Formats PackedPixel (2.0, 2.1)

MHL CTS 1.2, 1.3, 2.0, 2.1 Dongle tests supported by 980 MHL CBUS Compliance Test Module (except where noted):

Section 5.1.1: Electrical Tests

- Test 5.1.1.7: Rx Sense Impedance (Powered)
- Test 5.1.1.8: Rx Sense Impedance (Unpowered)

Section 5.2.5: EDID and Device Capability Register Test

- Test 5.2.5.1: EDID Reading Test
- Test 5.2.5.2: Device Capability Registers Test
- Test 5.2.5.3: Device Status Registers Test (1.3, 2.0, 2.1)

Section 5.2.6: RCP Sub-command Tests

Section 5.2.8: 3D Video

- Test 5.2.8.1: 3D Video Mode Support Data (2.0, 2.1)

Section 5.2.9: UCP Sub-command Test (2.0, 2.1)

Section 5.3: CBUS Tests (All tests in Sections 4.3.2 through 4.3.25)

Section 6: Common Tests (All tests in section 6.3.1 - 6.3.22)

MHL Dongle tests supported by Quantum Data 882EA:

Section 5.2.4: HDCP Test

