

# **High-Definition Multimedia Interface**

**Version 2.0**

**Quantum Data MOI v1.0**

**Test ID: HF1-25**

April 22, 2015

# Preface

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## Document Revision History

1.0 April 22, 2015 - Initial Release.

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## Contact Information

The URL for the HDMI Forum web site is: <http://www.hdmiforum.org/>

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# Introduction

This document provides a set of Method of Implementation for test method described in HDMI Compliance Test Specification Version 2.0 (HDMI CTS 2.0). HDMI Forum created HDMI CTS 2.0 to specify a set of tests that should be performed to verify features described in HDMI Specification Version 2.0.

## Scope

This document provides testing procedures for HDMI CTS 2.0 Test ID HF1-25: Source Video Timing – 6G – Non-2160p Deep Color.” The procedure below deals with single resolution and only one Test ID is considered at a time.

## References

### Normative References

High-Definition Multimedia Interface Specification Version 1.4b, October 11, 2011.  
HDMI Compliance Test Specification Version 1.4b, October 11, 2011.  
High-Definition Multimedia Interface Specification Version 2.0, August, 2013.  
HDMI Compliance Test Specification Version 2.0.

### Informative Reference

No additional informative references.

## Test ID HF1-25: Source Video Timing – 6G – Non-2160p Deep Color

### Objective

Confirm that the Source outputs the correct Deep Color non-2160p Video Timing with a TMDS Character Rate that is greater than 340Mcsc.

Table 7-52 Source Video Timing – 6G – Non-2160p Deep Color Requirements

Reference	Requirement
HDMI 2.0: 10.1] Use of the AVI InfoFrame in This Specification	<See reference for details>

### Capability(s)

The Source supports the transmission of any non-2160p Video Timing at 36 bits/Pixel or 30 bits/Pixel.

### Test Equipment

Item	Generic Equipment	Vendor Specific Equipment	Quantity
1	HDMI 2.0 Protocol Analyzer	980 Advanced Test Platform series: 980 HDMI 2.0 Protocol Analyzer module HDMI CTS 2.0 Compliance Test Package #3	1
2	Frequency Counter		1

### Generic Procedure

- 1 If the CDF field Source\_non\_2160p\_Video\_Formats\_Above\_340\_DC is empty, then SKIP this test.

Setup:

- 2 Connect the Source DUT to the Protocol Analyzer.
- 3 Configure the EDID, which indicates all of the Video Timings necessary for this test.

Measure:

- 4 For each Video Timing at 36 bits/Pixel listed in the CDF fieldSource\_non\_2160p\_Video\_Formats\_Above\_340\_DC, perform the following:
  - 4.1 Operate the Source DUT to output the tested format.
  - 4.2 Measure the TMDS Clock Rate with a frequency counter.
  - 4.3 If the TMDS Clock Rate is outside the allowable range, then FAIL.

4.3.1 The nominal TMDS Clock Rate is  $1.5 \times \frac{1}{4}$  of the nominal TMDS Character Rate of the Video Timing (at 24 bit/Pixel) being tested.

4.3.2 For video frame rates of 24, 30 Hz and multiples thereof, 1834 the allowed variation is  $\pm 0.5\%$ ; for non-2160p video frame rates, the allowed variation is  $\pm 0.5\%$ .

4.4 Capture and descramble the data (except for the one unscrambled Control Period per field) and verify the tested Video Timing as follows:

[Verify the General Control Packet for each tested format]

4.5 For every packet with Packet Type equal to 0x03 (General Control Packet), verify the following:

4.5.1 If either byte HB1 or HB2 does not equal 0x00, then FAIL.

4.5.2 Compare SB0...SB6 of subpacket 0 with SB0...SB6 of subpackets 1, 2 and 3. Likewise, compare subpacket 1 with subpacket 2 and 3 and compare subpacket 2 with subpacket 3.

4.5.3 If any subpacket differs from any other, then FAIL.

4.5.4 If SB0 of subpacket 0 does not equal 0x00, 0x01, or 0x10, then FAIL.

4.5.5 If any of the bytes SB3...SB6 of subpacket 0 does not equal 0x00, then FAIL.

4.5.6 If SB1[CD] does not indicate 36-bit (0110), then FAIL.

4.6 Track the video timing across several fields. For each General Control Packet received during that period with SB1[CD] not equal to 0:

4.6.1 Verify that SB1[PP] is updated correctly to indicate the packing phase of the last Pixel in the most recent Video Data Period.

4.6.2 If the Default\_Phase bit is set (=1), verify that:

- The first Pixel of each Video Data Period has a Pixel packing phase of 0 (10P0, 12P0, 16P0).
- The first Pixel following each Video Data Period has a Pixel packing phase of 0 (10C0, 12C0, 16C0).
- The PP bits are constant for all General Control Packets and equal to the last packing phase (10P4, 12P2, 16P1).
- The first Pixel following every transition of HSYNC or VSYNC has a Pixel packing phase of 0 (10C0, 12C0, 16C0).

4.6.3 If any of these conditions is not true, the FAIL, “Default\_Phase 1865 is incorrectly set”.

4.7 Verify that for all of the Video Data Periods, after unpacking (per the Pixel packing indicated by the PP field), have the correct length and that all HSYNC and VSYNC positions and lengths are accurate. If any of the values for the tested Video Timing are incorrect, then FAIL.

4.8 If the Source DUT does not support 36 bits/Pixel for that Video Timing but it supports 30/Pixel, then the above test is performed for 30 bits/Pixel using the same PASS/FAIL criteria for 30 bits/Pixel.

4.8.1 For step 4.3.1, the nominal TMDS Clock Rate is  $1.25 * \frac{1}{4}$  of the nominal TMDS Character Rate of the Video Timing (at 24 bits per Pixel) being tested.

[Verify the “Max\_TMDS\_Character\_Rate”]

- 5 Configure the EDID to include that the Max\_TMDS\_Character\_Rate equal to 0 (indicating below 340 Mcsc).
- 6 Operate the Source DUT to output the same signal.
- 7 If the Source DUT outputs the Video Timing above 340Mcsc, then FAIL.

Vendor Specific Test Procedure

Test Equipment

A variety of equipment is needed for testing HDMI products. Each piece is authorized and included by name in this Compliance Test Specification. This section describes the Quantum Data test equipment.

HDMI 2.0 Protocol Analyzer module

The Quantum Data 980 HDMI 2.0 Protocol Analyzer module can be installed in the 980B or 980R series Advanced Test Platforms. This 980 HDMI 2.0 Protocol Analyzer module serves the generic test functions called out in the HDMI 2.0 Generic CTS. Refer to the table below:

Item	Quantum Data Equipment	
1	980 Advanced Test Platform series:	
	Equipped with:	980 HDMI 2.0 Protocol Analyzer module
		HDMI CTS 2.0 Compliance Test Package #3

980 HDMI 2.0 Protocol Analyzer Module with 980 Series Platform Configurations

The figures below show depictions of the 980 HDMI 2.0 Protocol Analyzer module equipped in various 980 series platforms. **Note:** Card positioning may vary depending on configuration.



Source Video Timing – 6G – Non-2160p Deep Color

Test ID HF1-25: Source Video Timing – 6G – Non-2160p Deep Color



### 1. Objective

Confirm that the Source outputs the correct Deep Color non-2160p Video Timing with a TMDS Character Rate that is greater than 340Mcsc.

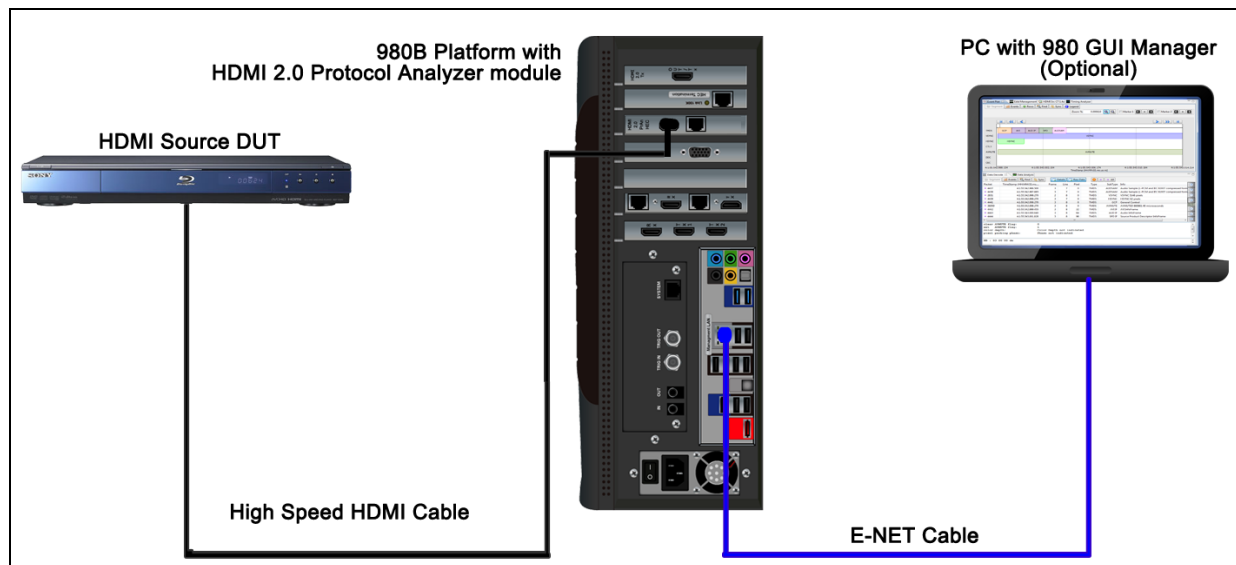
### 2. Test Overview

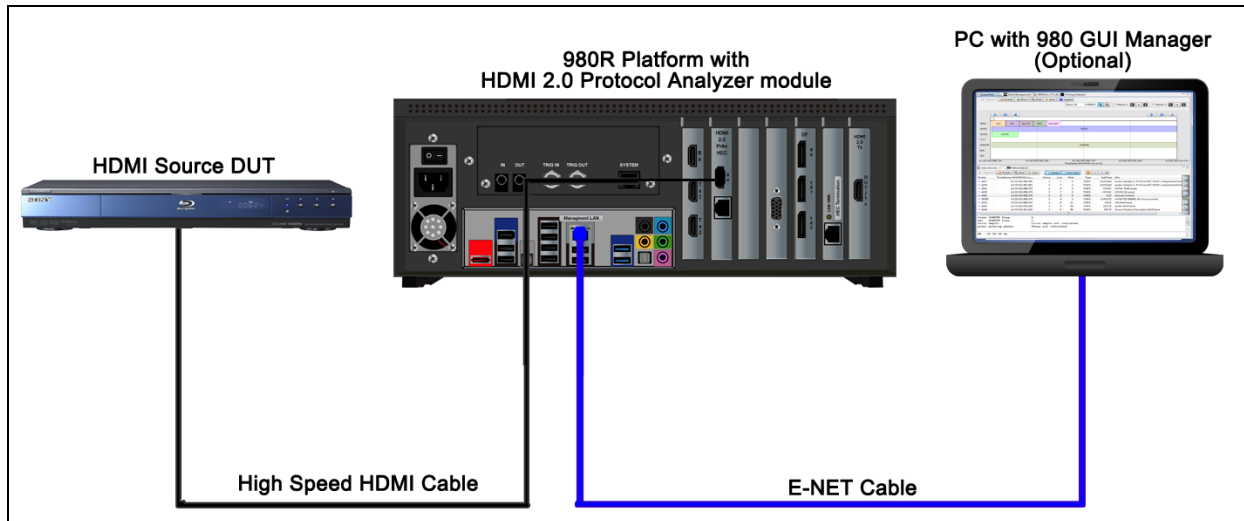
The Pass/Fail criteria is assessed by the application with no human examination required.

### 3. Procedure

Use the following procedure to conduct this test.

1. Connect Source DUT to the Quantum Data 980 HDMI 2.0 Protocol Analyzer at the module's port labeled Rx. Use a High Speed HDMI cable. The figures below show depictions of connections to the 980 HDMI 2.0 Protocol Analyzer module residing in the 980 series chassis.

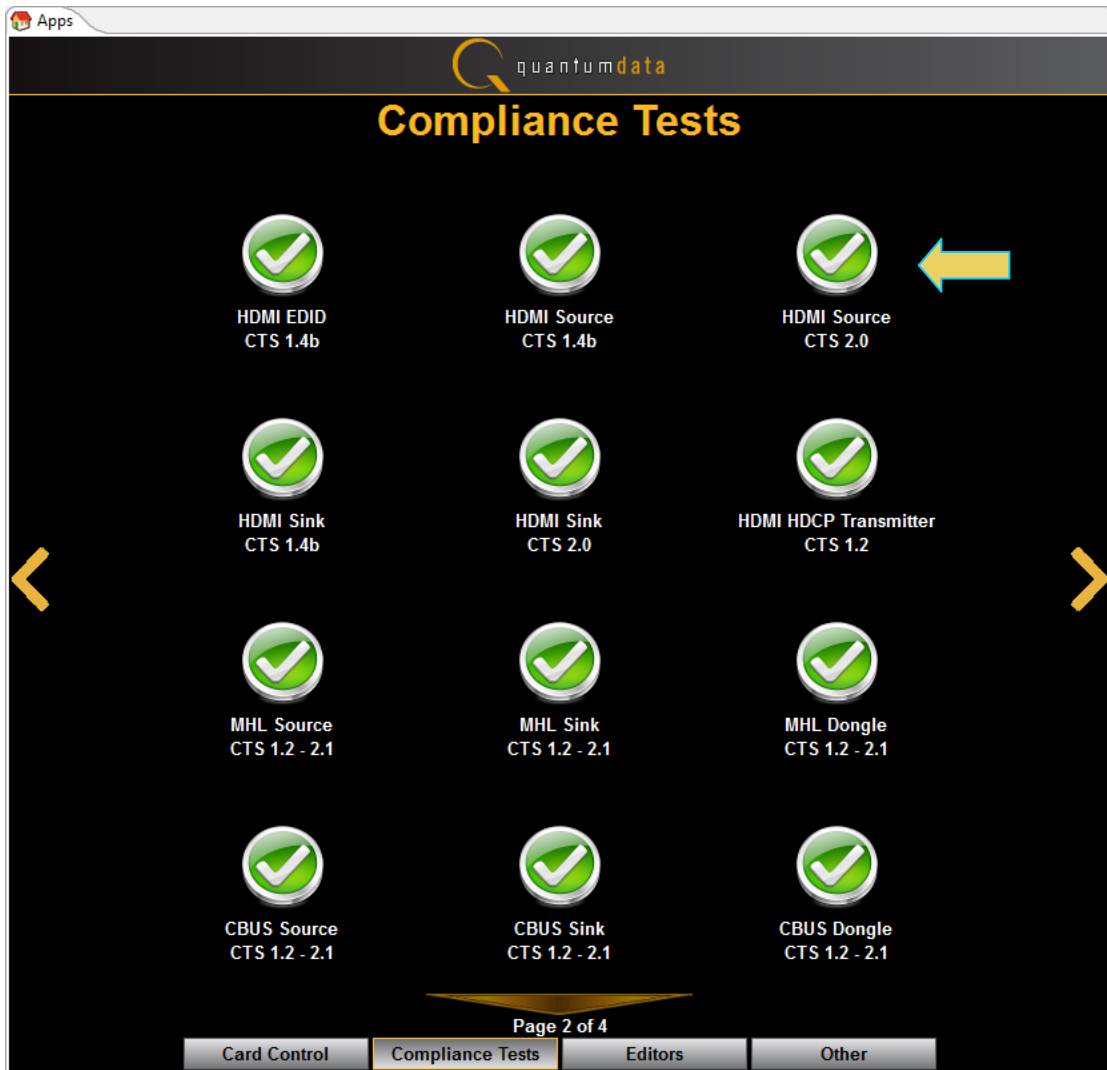




- 2 Operate the Source DUT to output the tested formats.
- 3 Use Quantum Data 980 Embedded Manager GUI (touchscreen) or invoke Quantum Data 980 External Manager GUI (Windows application).

**Note:** You will not need to connect the PC shown in the figures above if you are running the compliance test through the 980's embedded display. The PC running the 980 HDMI Protocol Analyzer module's compliance test application is connected to the 980 through a standard Ethernet cable.

- 4 Complete the following steps:
  - 4.1 Click on the HDMI Source CTS 2.0 icon in the Compliance Tests page of the Apps panel.



- 4.2 Navigate to the CDF tab if not already there. If there is a saved CDF file, then click on Open and select it. Otherwise, enter the DUT's CDF information for each tab and optionally click on Save to save the CDF.

HDMI 2.0 Src CT 2.0

CDF Entry Test Selection Test Options / Preview

Open New Save CDF File: /CDF/XYZ\_Source

General Y420 Video 21:9 (64:27) Video 6G Video 50p Timings

Source\_ITURBT\_2020\_101 Does the DUT support ITU-R BT.2020 Y'CC'BCC'RC Colorimetry?  
☐ Yes ☒ No

Source\_ITURBT\_2020\_110 Does the DUT support ITU-R BT.2020 Y'C'BC'R Colorimetry?  
☐ Yes ☒ No

Source\_LTE\_340Mscsc\_Scrambling Does the product support scrambling for TMDS Character Rates at or below 340Mscsc?  
☐ Yes ☒ No

Source\_Above\_340 Does the product support any Video Format/color mode for TMDS Character Rate above 340Mscsc up to 600Mscsc?  
☒ Yes ☐ No

**Source\_2160p\_Video\_Formats\_Above\_340**

(96) 3840x2160p @ 50 Hz 16:9	<input checked="" type="radio"/> Yes <input type="radio"/> No
(97) 3840x2160p @ 60 Hz 16:9	<input checked="" type="radio"/> Yes <input type="radio"/> No
(101) 4096x2160p @ 50 Hz 256:135	<input type="radio"/> Yes <input checked="" type="radio"/> No
(102) 4096x2160p @ 60 Hz 256:135	<input type="radio"/> Yes <input checked="" type="radio"/> No
(106) 3840x2160p @ 50 Hz 64:27	<input checked="" type="radio"/> Yes <input type="radio"/> No
(107) 3840x2160p @ 60 Hz 64:27	<input checked="" type="radio"/> Yes <input type="radio"/> No

**Source\_2160p\_DC\_Video\_Formats\_Above\_340**

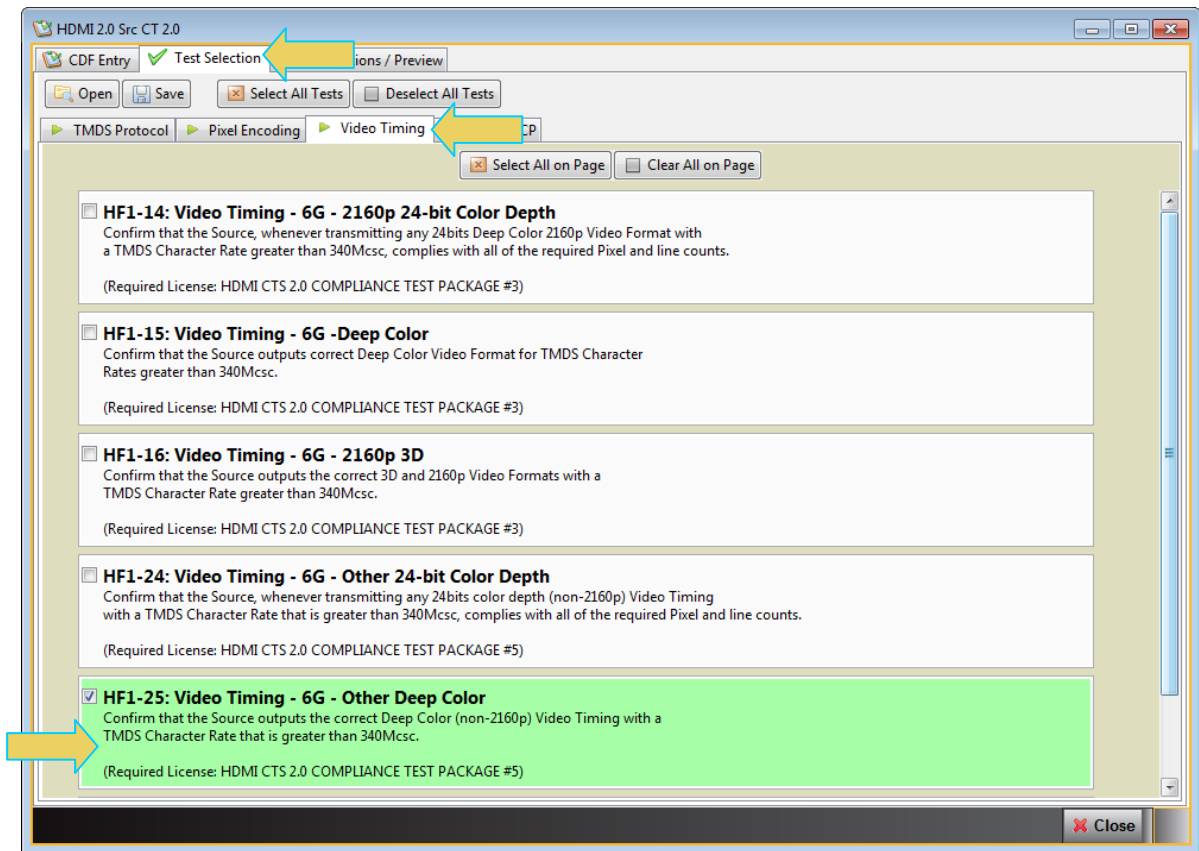
Format	30	36	48	(bits per pixel)
(93) 3840x2160p @ 24 Hz 16:9	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	(bits per pixel)
(94) 3840x2160p @ 25 Hz 16:9	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	(bits per pixel)
(95) 3840x2160p @ 30 Hz 16:9	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	(bits per pixel)
(98) 4096x2160p @ 24 Hz 256:135	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	(bits per pixel)
(99) 4096x2160p @ 25 Hz 256:135	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	(bits per pixel)
(100) 4096x2160p @ 30 Hz 256:135	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	(bits per pixel)
(103) 3840x2160p @ 24 Hz 64:27	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	(bits per pixel)
(104) 3840x2160p @ 25 Hz 64:27	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	(bits per pixel)
(105) 3840x2160p @ 30 Hz 64:27	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	(bits per pixel)

**Source\_2160p\_3D\_Video\_Formats\_Above\_340**

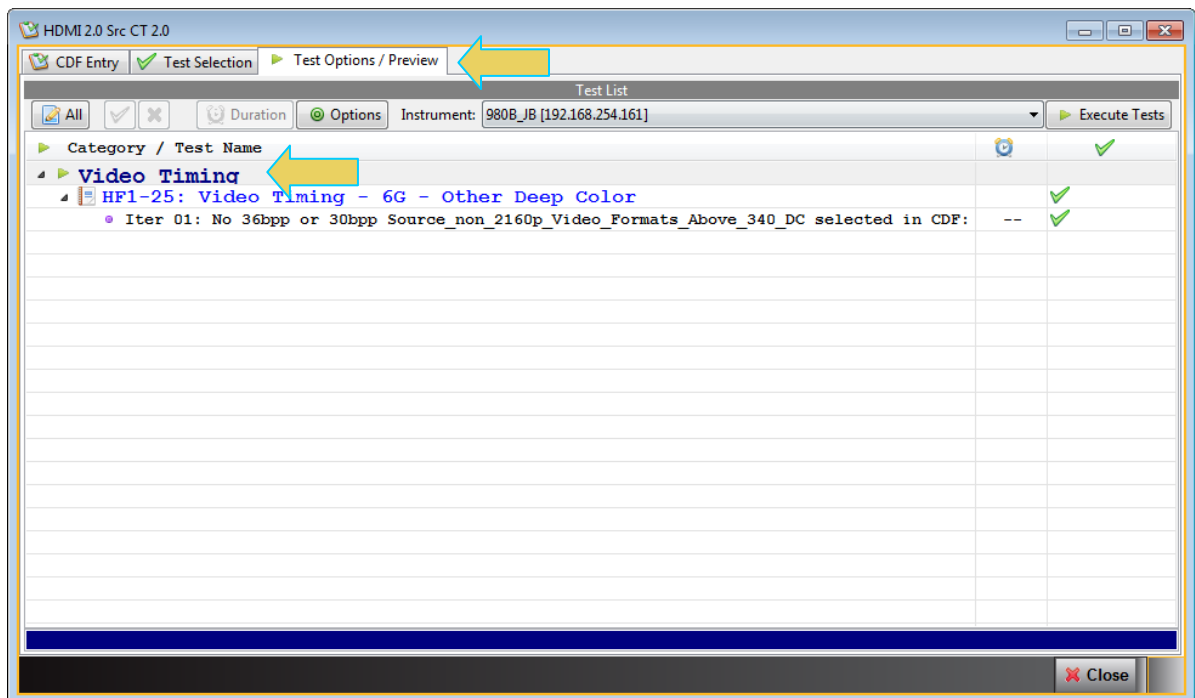
(95) 3840x2160p @ 30 Hz 16:9 - Frame Packing	<input type="radio"/> Yes <input checked="" type="radio"/> No
(94) 3840x2160p @ 25 Hz 16:9 - Frame Packing	<input type="radio"/> Yes <input checked="" type="radio"/> No
(93) 3840x2160p @ 24 Hz 16:9 - Frame Packing	<input type="radio"/> Yes <input checked="" type="radio"/> No
(98) 4096x2160p @ 24 Hz 256:135 - Frame Packing	<input type="radio"/> Yes <input checked="" type="radio"/> No
(100) 4096x2160p @ 30 Hz 256:135 - Frame Packing	<input type="radio"/> Yes <input checked="" type="radio"/> No
(99) 4096x2160p @ 25 Hz 256:135 - Frame Packing	<input type="radio"/> Yes <input checked="" type="radio"/> No
(97) 3840x2160p @ 60 Hz 16:9 - Side-by-Side (Half)	<input checked="" type="radio"/> Yes <input type="radio"/> No
(96) 3840x2160p @ 50 Hz 16:9 - Side-by-Side (Half)	<input checked="" type="radio"/> Yes <input type="radio"/> No

Close

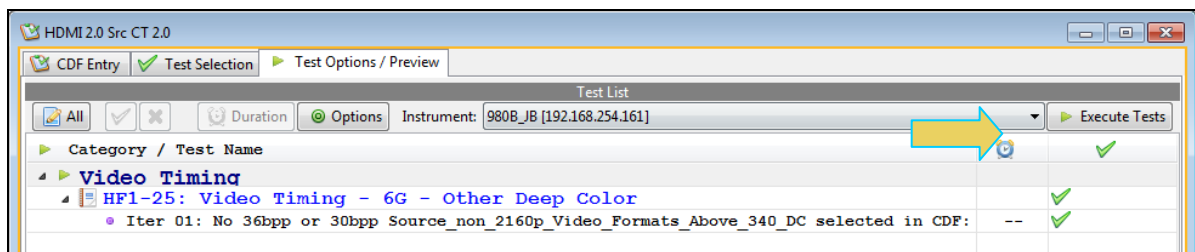
- 4.3 Click on the Test Selection tab and the Video Timing sub tab and select the Test ID HF1-25: Source Video Timing – 6G – Non-2160p Deep Color Test. Refer to the sample screen below.



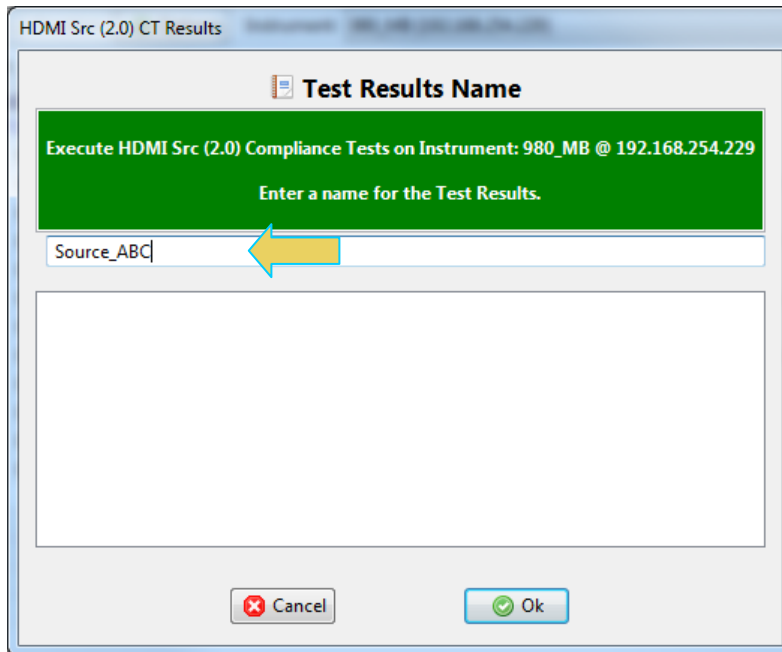
- 4.4 Click on Test Options / Preview tab and review the list of tests. Refer to the sample screen below.



4.5 Click on Execute tests activation button to initiate the test. Refer to the sample screen below.



**Note:** You will be prompted with a dialog box to assign a name to the test results. Refer to the screen example below:



Enter a name, click OK and the test will begin.

A Test Window will appear (below) indicating the progress of the test.

You will be prompted with a dialog box informing you of the requirements of the source DUT. Verify that the source is outputting the required HDMI format and pixel encoding and press Continue to run the test.

- 5 If the 980 HDMI Protocol Analyzer's compliance test application reports PASS, then PASS.  
If the 980 HDMI Protocol Analyzer's compliance test application reports FAIL, then FAIL.

