

High-Definition Multimedia Interface

Version 2.0

Quantum Data MOI v1.2

Test ID: HF1-16

July 24, 2015

Preface

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Document Revision History

- 1.2 July 24, 2015 – Removed limited scope statement pertaining to restricted set of 3D formats.

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Contact Information

The URL for the HDMI Forum web site is: <http://www.hdmiforum.org/>

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Introduction

This document provides a set of Method of Implementation for test method described in HDMI Compliance Test Specification Version 2.0 (HDMI CTS 2.0). HDMI Forum created HDMI CTS 2.0 to specify a set of tests that should be performed to verify features described in HDMI Specification Version 2.0.

Scope

This document provides testing procedures for HDMI CTS 2.0 Test ID HF1-16: “Source Video Timing – 6G – 2160p 3D.” The procedure below deals with single resolution and only one Test ID is considered at a time.

References

Normative References

High-Definition Multimedia Interface Specification Version 1.4b, October 11, 2011.
HDMI Compliance Test Specification Version 1.4b, October 11, 2011.
High-Definition Multimedia Interface Specification Version 2.0, August, 2013.
HDMI Compliance Test Specification Version 2.0.

Informative Reference

No additional informative references.

Test ID HF1-16: Source Video Timing – 6G – 2160p 3D

Objective

Confirm that the Source outputs the correct 2160p 3D Video Formats for TMDS Character Rate above 340Mcsc up to 600Mcsc.

Table 7-42 Source Video Timing - 6G – 2160p 3D Requirements

Reference	Requirement
[HDMI: 2.0: 10.1] Use of the AVI InfoFrame in This Specification	<See reference for details>
[HDMI: 2.0: 10.1.1] Signaling of 3D Video Formats	<See reference for details>
[HDMI 2.0: Appendix E] Signaling in AVI InfoFrame and VSIF for various Video Formats	<See reference for details>

Capability(s)

The Source DUT supports the transmission of any 2160p 3D Video Format for TMDS Character Rate above 340Mcsc up to 600Mcsc.

Test Equipment

Item	Generic Equipment	Vendor Specific Equipment	Quantity
1	HDMI 2.0 Protocol Analyzer	980 Advanced Test Platform series: 980 HDMI 2.0 Protocol Analyzer module HDMI CTS 2.0 Compliance Test Package #3	1
1	Frequency Counter		1

Generic Procedure

- 1 If no CDF field Source_2160p_3D_Video_Formats_Above_340 is declared, then SKIP this test.
Setup:
- 2 Connect the DUT to the Protocol Analyzer.
Measure:
- 3 For each Video Timing listed in CDF field Source_2160p_3D_Video_Formats_Above_340, perform the following:
 - 3.1 Operate the Source DUT to output the tested format. For all of the following, refer to the values listed in Table 7-44 through Table 7-49.
 - 3.2 Measure the TMDS Clock Rate with a frequency counter.

- 3.3 If the TMDS Clock Rate is outside the allowable range, then FAIL.
- 3.4 Capture and descramble the data (except for one unscrambled 1632 Control Period per field) and verify the tested format as follows:
[Verify H14b-VSIF Packet]
- 3.5 If the H14b-VSIF does not occur at least once per two Video Fields, then FAIL.
- 3.6 If an H14b-VSIF is transmitted:
 - 3.6.1 If PB5 equals 0b0000X000 or 0b0110X000 and byte HB2 (InfoFrame_Length) is less than 0x05, then FAIL.
 - 3.6.2 If PB5 equals 0b1000X000 and byte HB2 (InfoFrame_Length) is less than 0x06, then FAIL.
 - 3.6.3 If PB4, bit7, bit6 and bit5 (HDMI_Video_Format field) do not equal 0, 1, 0, then FAIL.
 - 3.6.4 If PB4, bit4...0 are not equal to 0 (reserved), then FAIL.
 - 3.6.5 If the Source DUT is outputting a 3D Video Format in Frame Packing as 3D Structure:
 - 3.6.5.1 If PB5 does not equal 0b0000X000, then FAIL.
 - 3.6.5.2 If byte HB2 (InfoFrame_Length) is more than 0x05:
 - 3.6.5.2.1 If byte PB5 equals 0x00 and bytes PB6 through InfoFrame_Length do not equal 0x00, then FAIL.
 - 3.6.5.2.2 If byte PB5 equals 0x08 and bytes PB7+M (where M is the value of bit4...0 of PB6) through InfoFrame_Length do not equal 0x00, then FAIL.
 - 3.6.6 If the Source DUT is outputting a 3D Video Format in Side-by-Side (Half) as 3D Structure:
 - 3.6.6.1 If PB5 does not equal 0b1000X000, then FAIL.
 - 3.6.6.2 If PB6 does not equal 0x00, 0x10, 0x20 or 0x30, then FAIL.
 - 3.6.6.3 If byte HB2 (InfoFrame_Length) is greater than 0x06:
 - 3.6.6.3.1 If byte PB5 equals 0x80 and bytes PB7 through InfoFrame_Length do not equal 0x00, then FAIL.
 - 3.6.6.3.2 If byte PB5 equals 0x88 and bytes PB8+1660 M (where M is the value of bit4...0 of PB7) through InfoFrame_Length do not equal 0x00, then FAIL.
 - 3.6.7 If the Source DUT is outputting a 3D Video Format in Top-and-Bottom as 3D Structure:

3.6.7.1 If PB5 does not equal 0b0110X000, then FAIL.

3.6.7.2 If byte HB2 (InfoFrame_Length) is greater than 0x05:

3.6.7.2.1 If byte PB5 equals 0x60 and bytes PB6 through InfoFrame_Length do not equal 0x00, then FAIL.

3.6.7.2.2 If byte PB5 equals 0x68 and bytes PB7+M (where M is the value of bit4...0 of PB6) through InfoFrame_Length do not equal 0x00, then FAIL.

3.6.8 Calculate the byte wide sum of HB0,HB1,HB2, PB0, PB1, PB2,...,PB5,...,PB [InfoFrame_Length].

3.6.9 If this byte wide sum is not equal to 0x00, then FAIL.

[Verify the Video Timing]

3.7 If an HF-VSIF is transmitted in any Video Frame during this test, then FAIL.

3.8 From the beginning of the captured data, scan for the first Video Data Period.

3.9 For each horizontal line, measure the following values:

- HS_POLARITY = HSYNC active value.
- HS_LEN = number of Pixels that HSYNC remains active.
- VIDEO_TO_HS = number of Pixels from the end of the Video Data Period to the HSYNC active edge.
- H_ACTIVE = number of Pixels in the Video Data Period minus 2 (for Guard Band).
- H_TOTAL = number of Pixels between two HSYNC active edges.

3.10 If any of the values of HS_POLARITY, HS_LEN, VIDEO_TO_HS, H_ACTIVE and H_TOTAL do not equal the correct value for the selected Video Format, then FAIL.

3.11 For each field, measure the following values:

- VS_POLARITY = VSYNC active value. VS_LEN = number of Pixels that VSYNC remains active divided by H_1690 TOTAL, rounded to the nearest integer
- V_ACTIVE = number of Video Data Periods between two consecutive VSYNC active edges.
- V_TOTAL = number of Pixels between the VSYNC active edges divided by H_TOTAL, rounded to the nearest half-integer.

3.12 Measure the following value:

- VS_TO_VIDEO = number of HSYNC pulses between the VSYNC active edge and the first subsequent Video Data Period, not including the HSYNC pulse that is coincident (or nearly so) with the VSYNC active edge.

- 3.13 If any of the values of VS_POLARITY, VS_LEN, VS_TO_VIDEO, V_ACTIVE and V_TOTAL does not equal the correct value for the selected Video Format, then FAIL.
- 3.14 If the Source DUT is outputting a 3D Video Format in Frame Packing as 3D structure, examine the area inserted between the two Active video regions, the "Active space".
 - 3.14.1 Examine the first Pixel value in the "Active space".
 - 3.14.2 Compare this first Pixel value with the other Pixel values in the "Active space".
 - 3.14.3 If any Pixel value differs from the first Pixel value in the "Active space", then FAIL.

Vendor Specific Test Procedure

Test Equipment

A variety of equipment is needed for testing HDMI products. Each piece is authorized and included by name in this Compliance Test Specification. This section describes the Quantum Data test equipment.

HDMI 2.0 Protocol Analyzer module

The Quantum Data 980 HDMI 2.0 Protocol Analyzer module can be installed in the 980B or 980R series Advanced Test Platforms. This 980 HDMI 2.0 Protocol Analyzer module serves the generic test functions called out in the HDMI 2.0 Generic CTS. Refer to the table below:

Item	Quantum Data Equipment	
1	980 Advanced Test Platform series:	
	Equipped with:	980 HDMI 2.0 Protocol Analyzer module
		HDMI CTS 2.0 Compliance Test Package #3

980 HDMI 2.0 Protocol Analyzer Module with 980 Series Platform Configurations

The figures below show depictions of the 980 HDMI 2.0 Protocol Analyzer module equipped in various 980 series platforms. **Note:** Card positioning may vary depending on configuration.



Source TMDS Video Timing

Test ID HF1-16 - Source Video Timing – 6G – 2160p 3D

1. Objective

Confirm that the Source outputs the correct 2160p 3D Video Formats for TMDS Character Rate above 340Mcsc up to 600Mcsc.

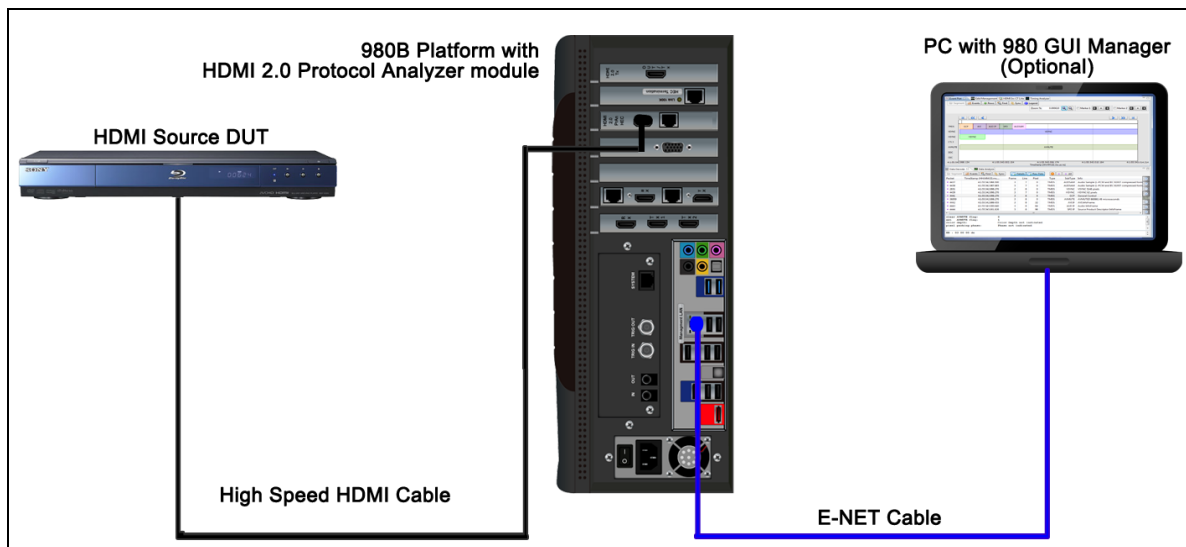
2. Test Overview

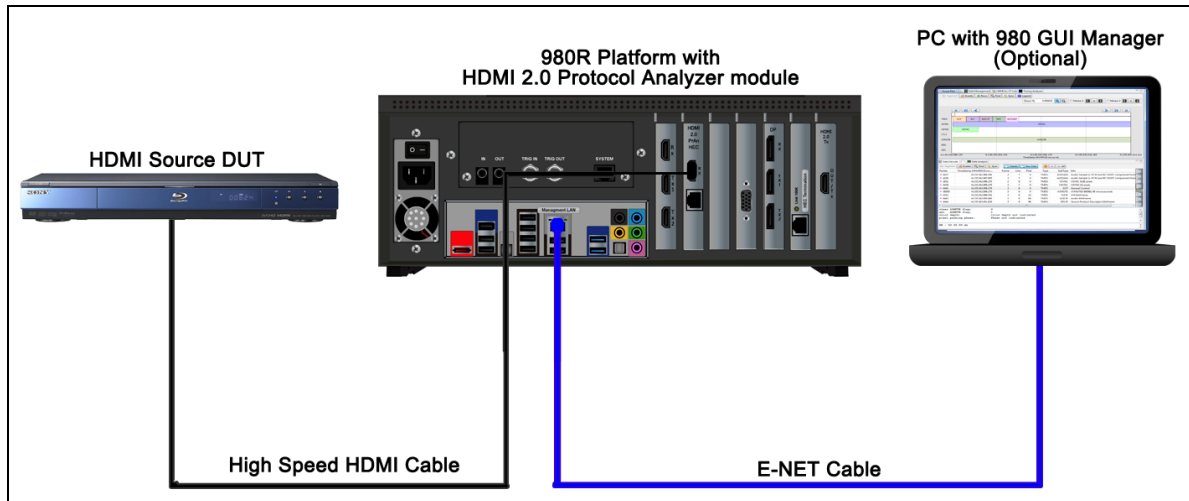
The Pass/Fail criteria is assessed by the application with no human examination required.

3. Procedure

Use the following procedure to conduct this test.

- 1 Connect Source DUT to the Quantum Data 980 HDMI 2.0 Protocol Analyzer at the module's port labeled Rx. Use a High Speed HDMI cable. The figures below show depictions of connections to the 980 HDMI 2.0 Protocol Analyzer module residing in the 980 series chassis.

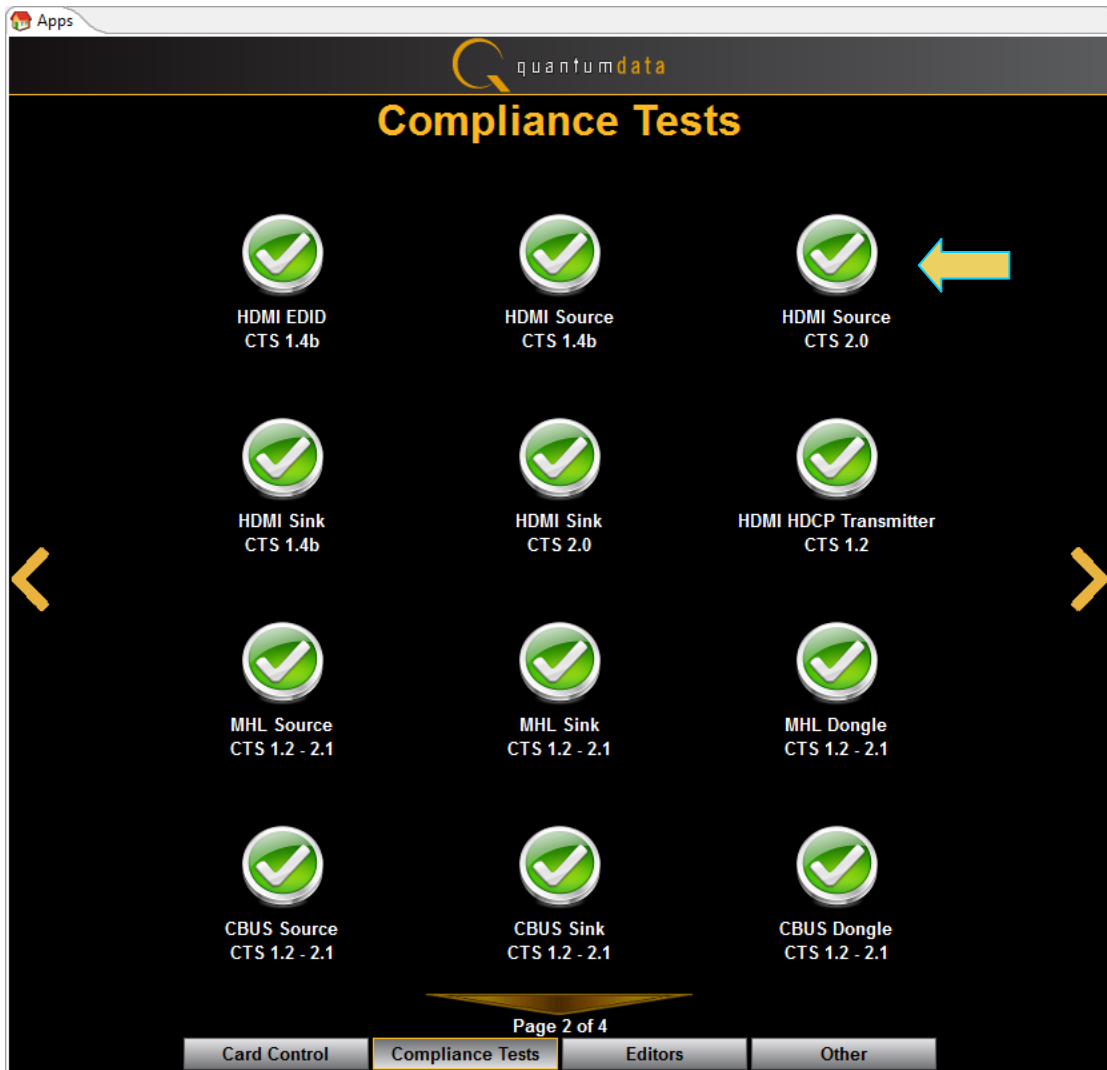




- 2 Operate the Source DUT to output the supported 3D formats.
- 3 Use Quantum Data 980 Embedded Manager GUI (touchscreen) or invoke Quantum Data 980 External Manager GUI (Windows application).

Note: You will not need to connect the PC shown in the figures above if you are running the compliance test through the 980's embedded display. The PC running the 980 HDMI Protocol Analyzer module's compliance test application is connected to the 980 through a standard Ethernet cable.

- 4 Complete the following steps:
 - 4.1 Click on the HDMI Source CTS 2.0 icon in the Compliance Tests page of the Apps panel.



- 4.2 Navigate to the CDF tab if not already there. If there is a saved CDF file, then click on Open and select it. Otherwise, enter the DUT's CDF information for each tab and optionally click on Save to save the CDF.

HDMI 2.0 Src CT 2.0

CDF Entry

Open New Save CDF File: <not saved>

General Y420 Video 21:9 (64:27) Video 6G Video

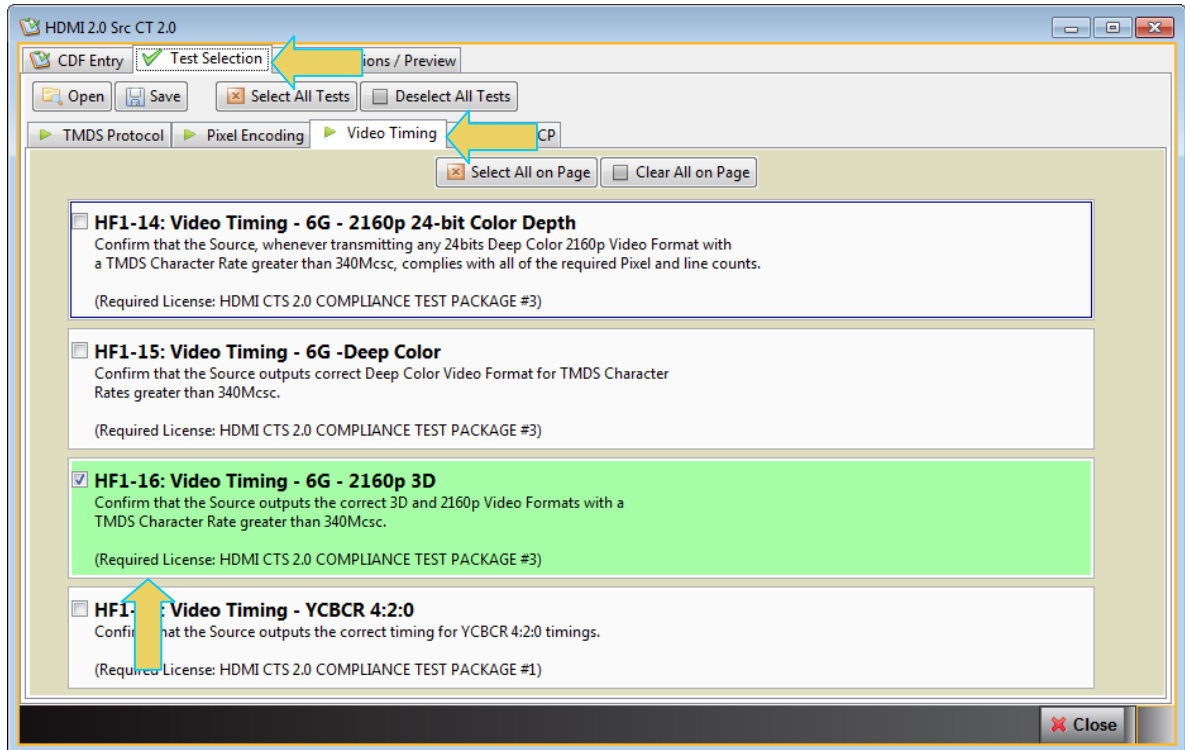
	30	36	48	(bits per pixel)
(94) 3840x2160p @ 25 Hz 16:9	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	(bits per pixel)
(95) 3840x2160p @ 30 Hz 16:9	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	(bits per pixel)
(98) 4096x2160p @ 24 Hz 256:135	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	(bits per pixel)
(99) 4096x2160p @ 25 Hz 256:135	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	(bits per pixel)
(100) 4096x2160p @ 30 Hz 256:135	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	(bits per pixel)
(103) 3840x2160p @ 24 Hz 64:27	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	(bits per pixel)
(104) 3840x2160p @ 25 Hz 64:27	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	(bits per pixel)
(105) 3840x2160p @ 30 Hz 64:27	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	(bits per pixel)

Source 2160p 3D Video Formats Above 340

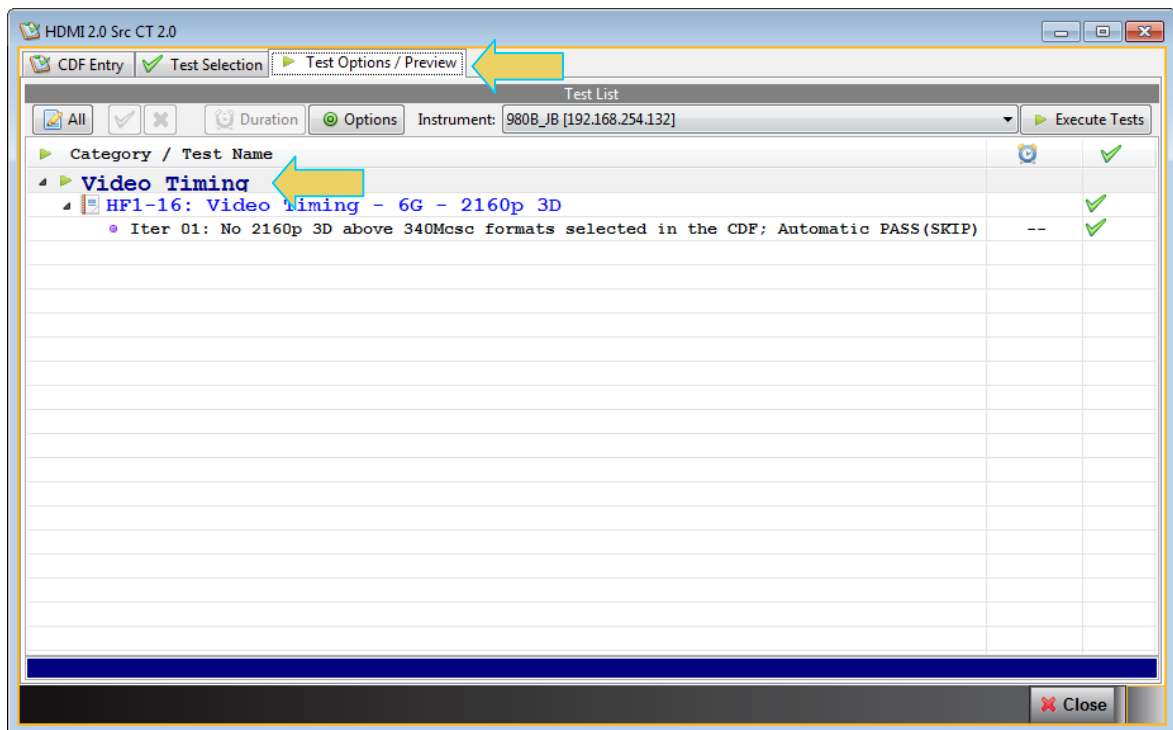
(95) 3840x2160p @ 30 Hz 16:9 - Frame Packing	<input checked="" type="radio"/> Yes <input type="radio"/> No
(94) 3840x2160p @ 25 Hz 16:9 - Frame Packing	<input checked="" type="radio"/> Yes <input type="radio"/> No
(93) 3840x2160p @ 24 Hz 16:9 - Frame Packing	<input checked="" type="radio"/> Yes <input type="radio"/> No
(98) 4096x2160p @ 24 Hz 256:135 - Frame Packing	<input checked="" type="radio"/> Yes <input type="radio"/> No
(100) 4096x2160p @ 30 Hz 256:135 - Frame Packing	<input checked="" type="radio"/> Yes <input type="radio"/> No
(99) 4096x2160p @ 25 Hz 256:135 - Frame Packing	<input checked="" type="radio"/> Yes <input type="radio"/> No
(97) 3840x2160p @ 60 Hz 16:9 - Side-by-Side (Half)	<input checked="" type="radio"/> Yes <input type="radio"/> No
(96) 3840x2160p @ 50 Hz 16:9 - Side-by-Side (Half)	<input checked="" type="radio"/> Yes <input type="radio"/> No
(102) 4096x2160p @ 60 Hz 256:135 - Side-by-Side (Half)	<input checked="" type="radio"/> Yes <input type="radio"/> No
(101) 4096x2160p @ 50 Hz 256:135 - Side-by-Side (Half)	<input checked="" type="radio"/> Yes <input type="radio"/> No
(97) 3840x2160p @ 60 Hz 16:9 - Top-and-Bottom	<input checked="" type="radio"/> Yes <input type="radio"/> No
(96) 3840x2160p @ 50 Hz 16:9 - Top-and-Bottom	<input checked="" type="radio"/> Yes <input type="radio"/> No
(102) 4096x2160p @ 60 Hz 256:135 - Top-and-Bottom	<input checked="" type="radio"/> Yes <input type="radio"/> No
(101) 4096x2160p @ 50 Hz 256:135 - Top-and-Bottom	<input checked="" type="radio"/> Yes <input type="radio"/> No

Close

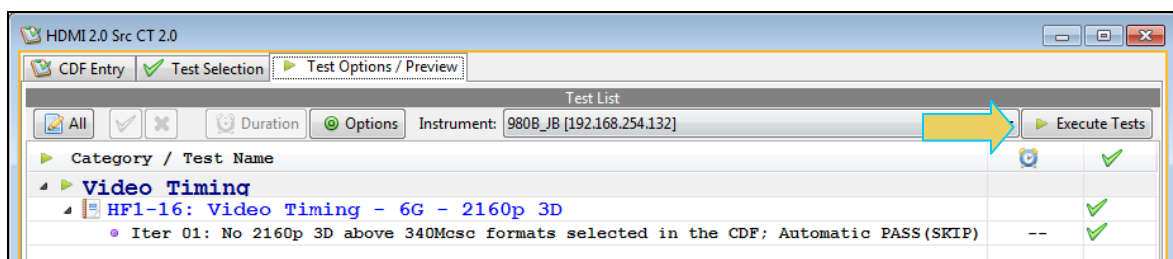
- 4.3 Click on the Test Selection tab and the Video Timing sub tab and select the HF1-16 Video Timing – 6G – 2160p 3D Test. Refer to the sample screen below.



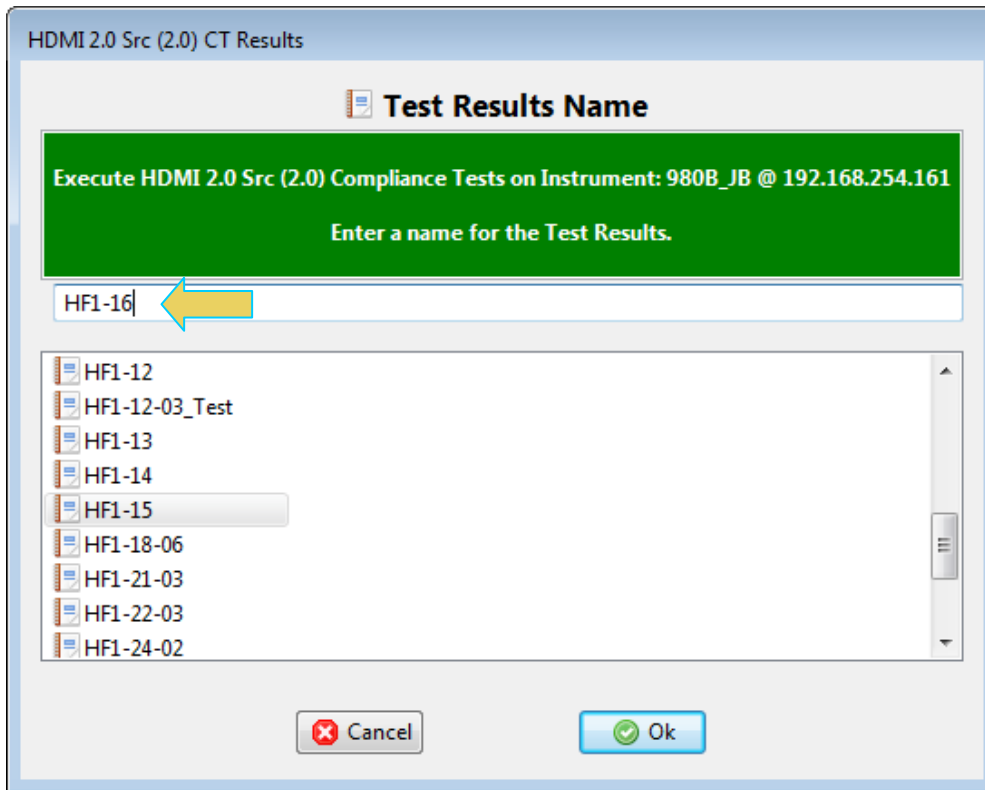
- 4.4 Click on Test Options / Preview tab and review the list of tests. Refer to the sample screen below.



- 4.5 Click on Execute tests activation button to initiate the test. Refer to the sample screen below.

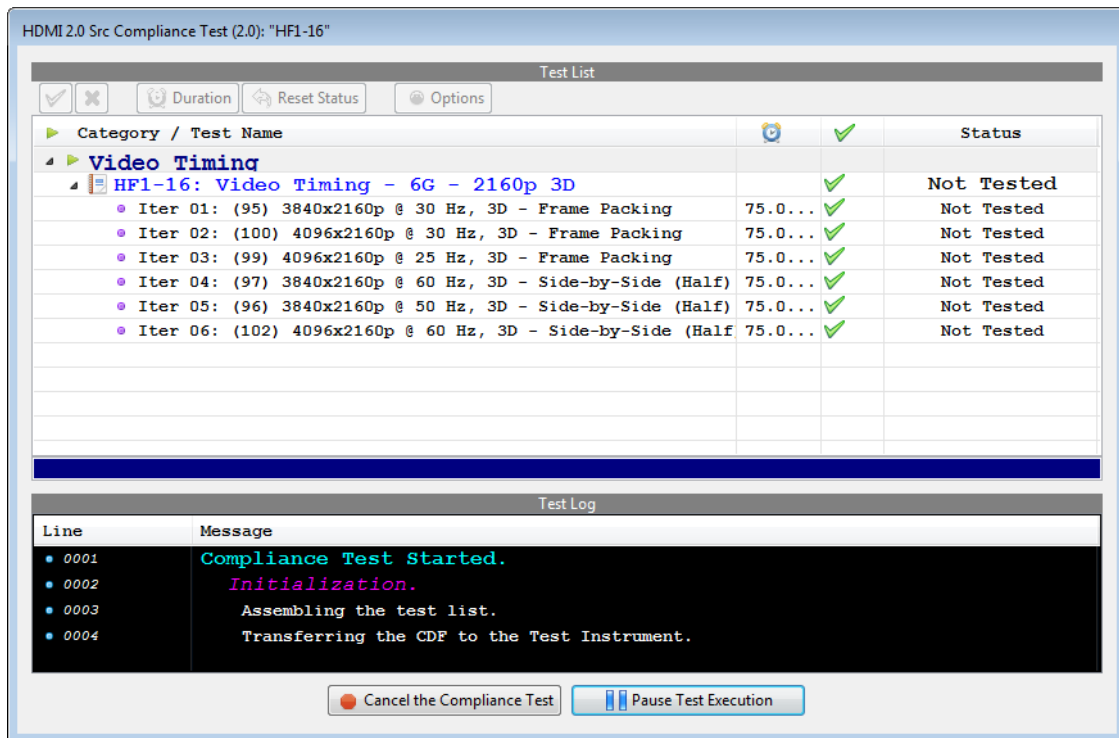


Note: You will be prompted with a dialog box to assign a name to the test results. Refer to the screen example below:

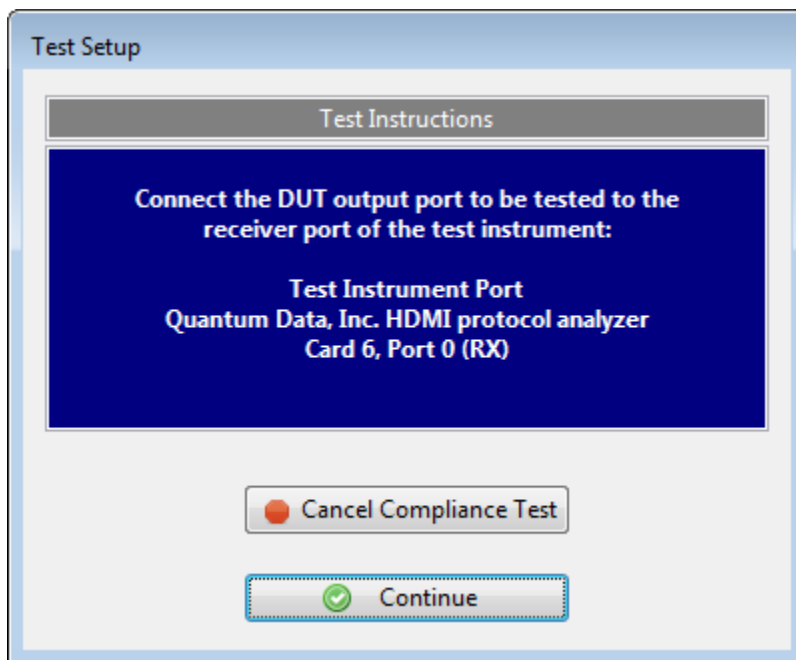


Enter a name, click OK and the test will begin.

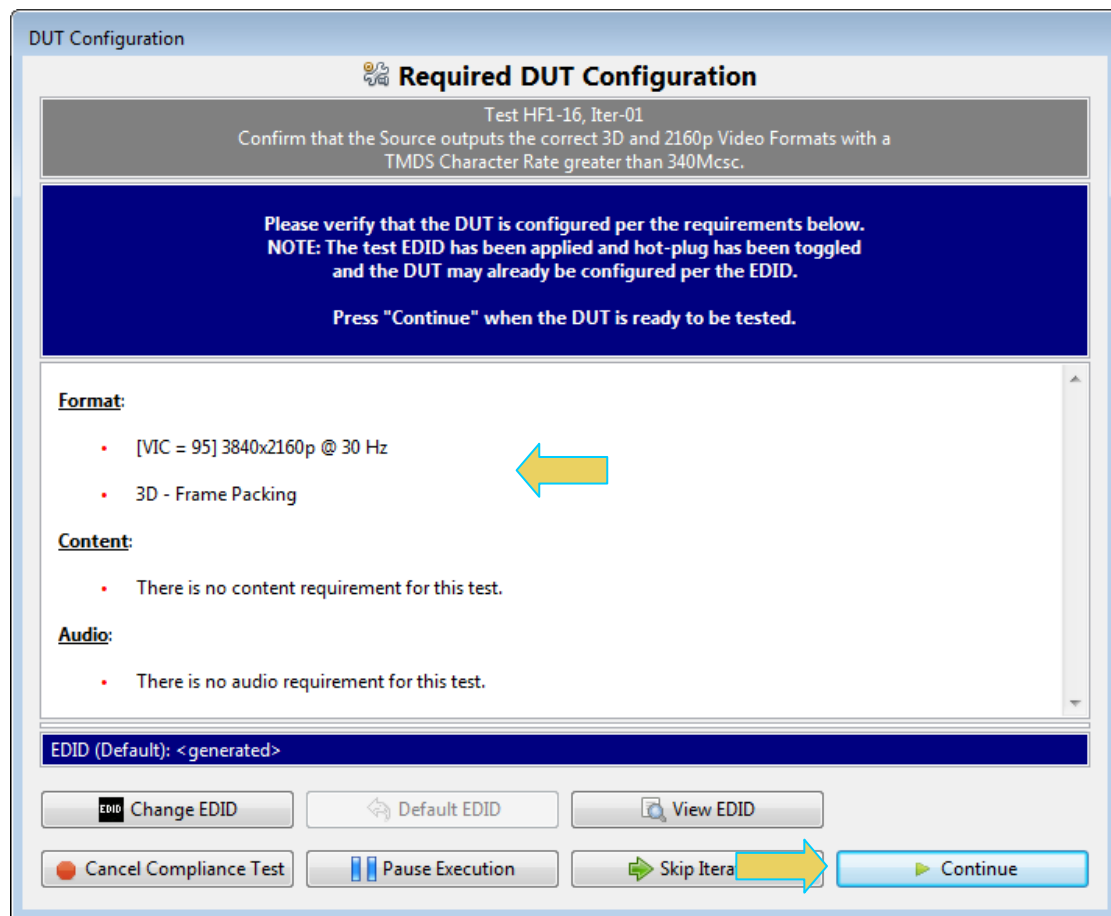
A Test Window will appear (below) indicating the progress of the test.



A Test Window will appear (below) indicating the test setup.



You will be prompted with a dialog box informing you of the requirements of the source DUT. Verify that the source is outputting the required HDMI format and pixel encoding and press Continue to run the test.



- 5 If the 980 HDMI Protocol Analyzer's compliance test application reports PASS, then PASS.
If the 980 HDMI Protocol Analyzer's compliance test application reports FAIL, then FAIL.

