

High-Definition Multimedia Interface

Version 2.0

Quantum Data MOI v1.0a

Test ID: HF1-34

December 3, 2015

Preface

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Document Revision History

1.0a December 3, 2015 – Added limited scope statement to Vendor Procedure.

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Contact Information

The URL for the HDMI Forum web site is: <http://www.hdmiforum.org/>

The URL for the Quantum Data website is: <http://www.quantumdata.com>.

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Introduction

This document provides a set of Method of Implementation for test method described in HDMI Compliance Test Specification Version 2.0 (HDMI CTS 2.0). HDMI Forum created HDMI CTS 2.0 to specify a set of tests that should be performed to verify features described in HDMI Specification Version 2.0.

Scope

This document provides testing procedures for HDMI CTS 2.0 Test ID HF1-34: “Source Video Timing - YCBCR 4:2:0 Deep Color Test.”

References Document

Normative References

High-Definition Multimedia Interface Specification Version 1.4b, October 11, 2011.
HDMI Compliance Test Specification Version 1.4b, October 11, 2011.
High-Definition Multimedia Interface Specification Version 2.0, August, 2013.
HDMI Compliance Test Specification Version 2.0.
HDMI 2.0 Generic Compliance Test Specification Version (GCTS), Version 2.0b, April 2, 2015.

Informative Reference

No additional informative references.

Test ID HF1-34: Source Video Timing - YCBCR 4:2:0 Deep Color Tests

Objective

Confirm that the Source outputs a correct timing for YCbCr 4:2:0 Deep Color timings.

Table 7-58 Source Video Timing – YCBCR 4:2:0 Deep Color Requirements

Reference	Requirement
[HDMI 2.0: 7.1.1]	<p>“When transmitting Deep Color 4:2:0 encoded Pixels, the Color Depth bits of the General Control Packet shall be set accurately (See [HDMI: 5.3.6] and [HDMI: 6.5.3]).”</p> <p>“Transmission of Deep Color 4:2:0 encoded Pixels is achieved by first mapping two 4:2:0 Pixels onto a single 4:4:4 Pixel. The mapping is described in Table 7-1, Table 7-2, Table 7-3, and Table 7-4 for 24-, 30-, 36-, and 48-bit Pixels respectively.</p> <p>The mapped Pixels are then transported utilizing the packing methods described in [HDMI: 6.5.2], [HDMI: 6.5.3], and [HDMI: Appendix D].”</p> <p>“A Source shall not send a Deep Color 4:2:0 Pixel Encoded signal to a Sink that does not indicate its support in the HF-VSDB.”</p>
[HDMI: 5.3.6]	<See reference for details on General Control Packet>
[HDMI: 6.5.2, 6.5.3, Appendix D]	<See reference for details on Deep Color packing and signaling>
CEA 861-F, Section 4	<See reference for details on Video Timings>

Capability(s)

The Source DUT supports at least one Video Format in YC_BC_R 4:2:0 color sampling mode with 10, 12 or 16 bits per color component.

Test Equipment

Item	Generic Equipment	Vendor Specific Equipment	Quantity
1	DDC Slave Emulator	980 Advanced Test Platform series:	1
2	EDID Emulator	980 HDMI Protocol Analyzer module	1
3	Video Timing Analyzer	HDMI CTS 2.0 Compliance Test Package #3	1

Generic Procedure

- 1 If the CDF fields Source_HDMI_YCBCR_420_DC10 equals “N”, Source_HDMI_YCBCR_420_DC12 equals “N” and Source_HDMI_YCBCR_420_DC16 equals “N”, then SKIP this test.
- 2 If the CDF field Source_HDMI_YCBCR_420 is “N”, then FAIL.

- 3 If CDF field Source_Above_340 is “N”, then FAIL.
- 4 Connect the Source DUT to a 594MHz Video Protocol Analyzer with the DDC Slave Emulator and EDID Emulator.
- 5 Program the EDID Emulator to reveal an EDID containing the following:
 - 5.2 YC_BC_R 4:2:0 Video Data Block with:
 - 5.2.1 YC_BC_R 4:2:0-only SVDs = 96, 97, 101, 102, 106 and 107 (NOTE: If a regular Video Data Block is also present, then it shall not contain SVDs = 96, 97, 101, 102, 106, or 107).
 - 5.3 HF-VSDB with:
 - 5.3.1 Max_TMDS_Character_Rate = 119 (595Mcsc).
 - 5.3.2 One of DC_30bit_420, DC_36bit_420 or DC_48bit_420 equals to 1.
- 6 Operate the Source DUT to output a YCBCR 4:2:0 Pixel encoded Deep Color signal at a Video Format for which it supports 4:2:0 transmission (see CDF field Source_HDMI_YCBCR_420_Video_Formats) with Deep Color (see CDF fields Source_HDMI_YCBCR_420_DC10, Source_HDMI_YCBCR_420_DC12, and Source_HDMI_YCBCR_420_DC16), repeating all of the following tests for at least one of the supported Video Formats with all of the supported color depths.
- 7 Capture and descramble the data.
- 8 For every packet where the Packet Type equals 0x03 (General Control Packet), verify the following:
 - 8.2 If either byte HB1 or HB2 does not equal 0x00, then FAIL.
 - 8.3 Compare SB0...SB6 of subpacket 0 with SB0...SB6 of subpackets 1, 2 and 3. Likewise, compare subpacket 1 with subpacket 2 and 3 and compare subpacket 2 with subpacket 3.
 - 8.4 If any subpacket differs from any other, then FAIL.
 - 8.5 If SB0 of subpacket 0 does not equal 0x00, 0x01, or 0x10, then FAIL.
 - 8.6 If any byte SB3...SB6 of subpacket 0 does not equal 0x00, then FAIL.
 - 8.7 If the transmitted color depth is equal to 10 and the SB1 field Color Depth does not indicate 30-bit (0101), then FAIL.
 - 8.8 If the transmitted color depth is equal to 12 and the SB1 field Color Depth does not indicate 36-bit (0110), then FAIL.

- 8.9 If the transmitted color depth is equal to 16 and the SB1 field Color Depth does not indicate 48-bit (0111), then FAIL.
- 8.10 Track the TMDS Character Rate and Video Timing across several fields. For each General Control Packet received during that period with a non-zero Color Depth:
- 8.10.1 Verify that the PP field is correctly updated to indicate the packing phase of the last Pixel in the most recent Video Data Period.
- 8.10.2 Verify that the TMDS Character Rate is correct (i.e. 30-bit: 1.25 x, 36-bit: 1.5 x or 48-bit: 2 x 4:2:0 Pixel Clock Rate (297Mcsc)). If not, then FAIL.
- 8.10.3 If the Default_Phase bit is set (=1), verify that:
- 8.10.3.1 The first Pixel of each Video Data Period has a Pixel packing phase of 0 (10P0, 12P0, 16P0).
- 8.10.3.2 The first Pixel following each Video Data Period has a Pixel packing phase of 0 (10C0, 12C0, 16C0).
- 8.10.3.3 The PP bits are constant for all General Control Packets and equal to the last packing phase (10P4, 12P2, 16P1).
- 8.10.3.4 The first Pixel following every transition of HSYNC or VSYNC has a Pixel packing phase of 0 (10C0, 12C0, 16C0).
- 8.10.4 If any of these conditions is not true, then FAIL, "Default_Phase is incorrectly set".
- 8.11 Verify that all of the Video Data Periods, after unpacking (per the Pixel packing indicated by the PP field) have the correct length and that all HSYNC and VSYNC positions and lengths are accurate. If any of the values is incorrect, then FAIL. (NOTE: All horizontal timing is reduced by half including the Htotal, Hactive, Hblank, Hfront, Hsync, and Hback parameters).

Vendor Specific Test Procedure

Test Equipment

A variety of equipment is needed for testing HDMI products. Each piece is authorized and included by name in this Compliance Test Specification. This section describes the Quantum Data test equipment.

HDMI 2.0 Protocol Analyzer module

The Quantum Data 980 HDMI 2.0 Protocol Analyzer module can be installed in the 980B or 980R series Advanced Test Platforms. This 980 HDMI 2.0 Protocol Analyzer module serves the generic test functions called out in the HDMI 2.0 Generic CTS. Refer to the table below:

Item	Quantum Data Equipment	
1	980 Advanced Test Platform series:	
	Equipped with:	980 HDMI 2.0 Protocol Analyzer module
		HDMI CTS 2.0 Compliance Test Package #3

980 HDMI 2.0 Protocol Analyzer Module with 980 Series Platform Configurations

The figures below show depictions of the 980 HDMI 2.0 Protocol Analyzer module equipped in various 980 series platforms. **Note:** Card positioning may vary depending on configuration.



Source Video Timing - YCBCR 4:2:0 Deep Color Tests

1. Objective

Confirm that the Source outputs the correct timing for YCBCR 4:2:0 Deep Color timings.

Due to lack of availability of DUT devices supporting YCBCR 4:2:0 Deep Color timings during MOI verification, this MOI is approved with limited scope. Only VIC 97 was tested and verified.

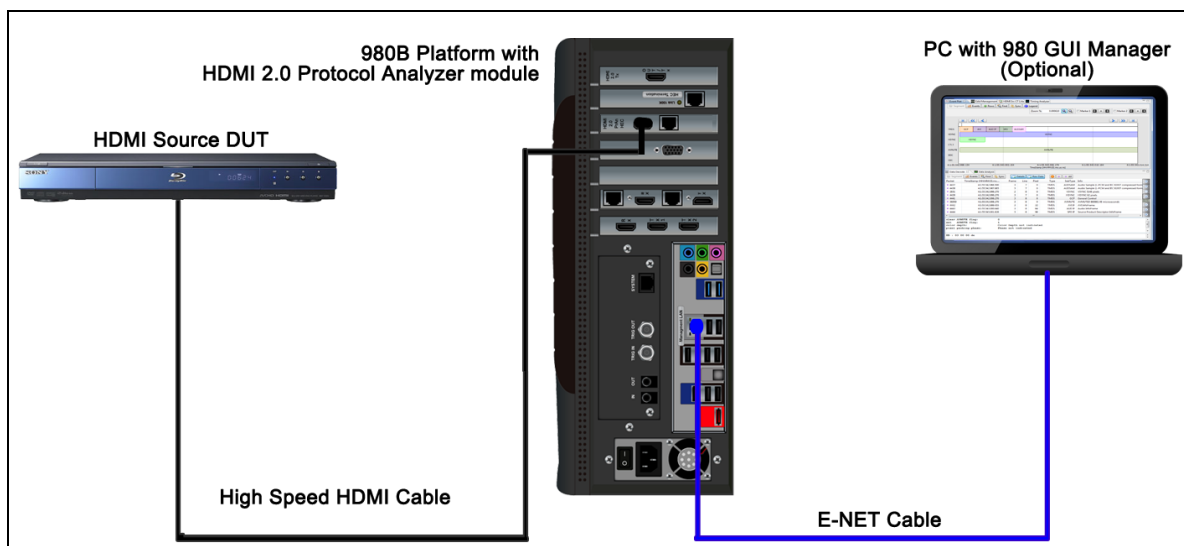
2. Test Overview

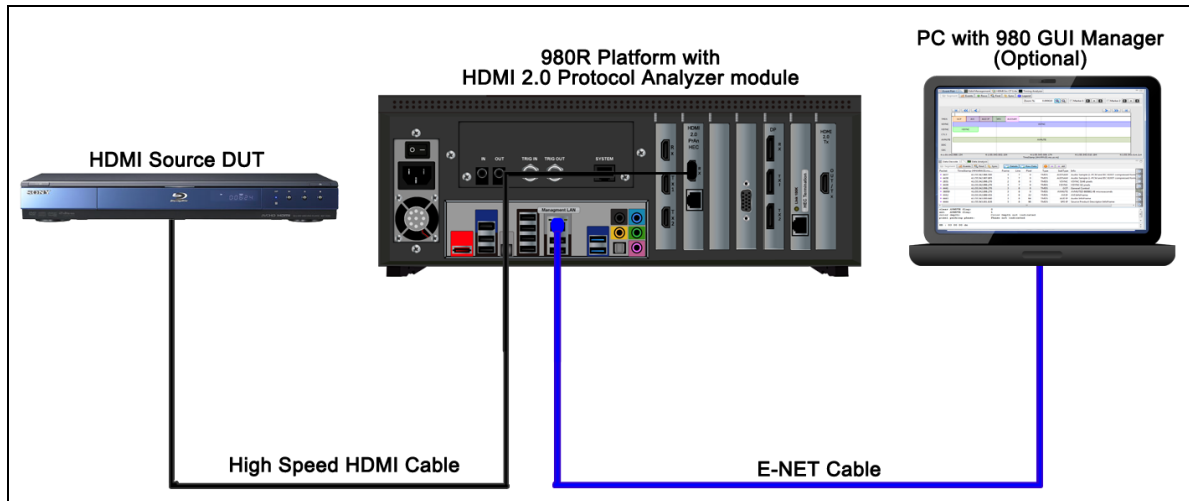
The Pass/Fail criterion is assessed by the application with no human examination required.

3. Procedure

Use the following procedure to conduct this test.

- 1 Connect Source DUT to the Quantum Data 980 HDMI 2.0 Protocol Analyzer at the module's port labeled Rx. Use a High Speed HDMI cable. The figures below show depictions of connections to the 980 HDMI 2.0 Protocol Analyzer module residing in the 980 series chassis.

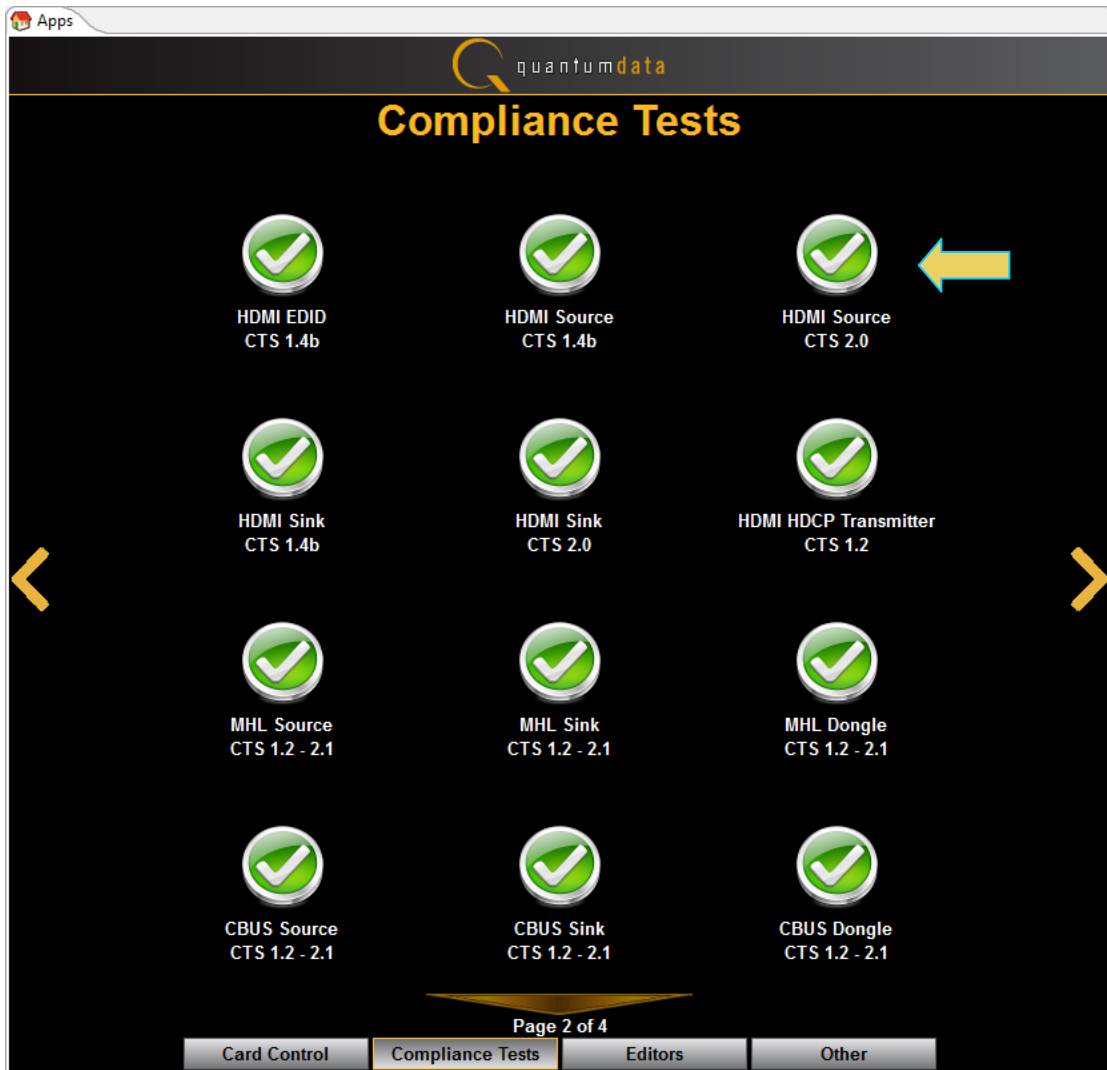




- 2 Operate the Source DUT to output the tested formats.
- 3 Use Quantum Data 980 Embedded Manager GUI (touchscreen) or invoke Quantum Data 980 External Manager GUI (Windows application).

Note: You will not need to connect the PC shown in the figures above if you are running the compliance test through the 980's embedded display. The PC running the 980 HDMI 2.0 Protocol Analyzer module's compliance test application is connected to the 980 through a standard Ethernet cable.

- 4 Complete the following steps:
 - 4.1 Click on the HDMI Source CTS 2.0 icon in the Compliance Tests page of the Apps panel.



- 4.2 Navigate to the CDF tab if not already there. If there is a saved CDF file, then click on Open and select it. Otherwise, enter the DUT's CDF information for each tab and optionally click on Save to save the CDF.

Be sure to indicate support for Source_HDMI_YCBR_420, Source_HDMI_YCBCR_420_DC10/12/16 and Source_HDMI_YCBCR_420_Video_Formats on the Y420 Video tab and Source_Above_340 on the 6G Video tab. The CDF screens are shown below.

HDMI 2.0 Src CT 2.0

CDF Entry Test Selection Test Options / Preview

Open New Save CDF File: <not saved>

General Y420 Video 21:9 (64:27) Video 6G Video non2160p Timings HDR

Source_HDMI_YCBCR_420 Does the DUT support YCBCR4:2:0 Pixel encoding transmission?
☒ Yes ☐ No

Source_HDMI_YCBCR_420_Test_Image Does the DUT support the generation of the prescribed test images for YCBCR4:2:0 Pixel encoding transmission?
☐ Yes ☒ No

Source_HDMI_YCBCR_420_DC10 Does the DUT support YCBCR 4:2:0 Deep Color Pixel encoding with 10-bits per component?
☒ Yes ☐ No

Source_HDMI_YCBCR_420_DC12 Does the DUT support YCbCr 4:2:0 Deep Color Pixel decoding with 12-bits per component?
☒ Yes ☐ No

Source_HDMI_YCBCR_420_DC16 Does the DUT support YCbCr 4:2:0 Deep Color Pixel decoding with 16-bits per component?
☐ Yes ☒ No

Source_HDMI_YCBCR_420_BT2020_YCC Does the DUT support YCC 4:2:0 Pixel encoding in BT.2020 Y'C'BC'R Colorimetry?
☐ Yes ☒ No

Source_HDMI_YCBCR_420_BT2020_cYCC Does the DUT support YCC 4:2:0 Pixel encoding in BT.2020 Y'CC'BCC'RC Colorimetry?
☐ Yes ☒ No

Source_HDMI_YCBCR_420_Video_Formats

(96) 3840x2160p @ 50 Hz 16:9	<input checked="" type="checkbox"/> 24	<input checked="" type="checkbox"/> 30	<input type="checkbox"/> 36	<input type="checkbox"/> 48	(bits per pixel)
(97) 3840x2160p @ 60 Hz 16:9	<input checked="" type="checkbox"/> 24	<input checked="" type="checkbox"/> 30	<input type="checkbox"/> 36	<input type="checkbox"/> 48	(bits per pixel)
(101) 4096x2160p @ 50 Hz 256:135	<input type="checkbox"/> 24	<input type="checkbox"/> 30	<input type="checkbox"/> 36	<input type="checkbox"/> 48	(bits per pixel)
(102) 4096x2160p @ 60 Hz 256:135	<input type="checkbox"/> 24	<input type="checkbox"/> 30	<input type="checkbox"/> 36	<input type="checkbox"/> 48	(bits per pixel)
(106) 3840x2160p @ 50 Hz 64:27	<input type="checkbox"/> 24	<input type="checkbox"/> 30	<input type="checkbox"/> 36	<input type="checkbox"/> 48	(bits per pixel)
(107) 3840x2160p @ 60 Hz 64:27	<input type="checkbox"/> 24	<input type="checkbox"/> 30	<input type="checkbox"/> 36	<input type="checkbox"/> 48	(bits per pixel)


Close

HDMI 2.0 Src CT 2.0

CDF Entry ☒ Test Selection ☐ Test Options / Preview

Open New Save CDF File: <not saved>

General Y420 Video 21:9 (64:27) Video 6G Video non2160p Timings HDR

Source_ITURBT_2020_101	Does the DUT support ITU-R BT.2020 Y'CC'BCC'RC Colorimetry?	<input type="radio"/> Yes <input checked="" type="radio"/> No
Source_ITURBT_2020_110	Does the DUT support ITU-R BT.2020 Y'C'BC'R Colorimetry?	<input type="radio"/> Yes <input checked="" type="radio"/> No
Source_LTE_340Msc_Scrambling	Does the product support scrambling for TMDS Character Rates at or below 340Msc?	<input type="radio"/> Yes <input checked="" type="radio"/> No
 Source_Above_340	Does the product support any Video Format/color mode for TMDS Character Rate above 340Msc up to 600Msc?	<input checked="" type="radio"/> Yes <input type="radio"/> No

Source_2160p_Video_Formats_Above_340

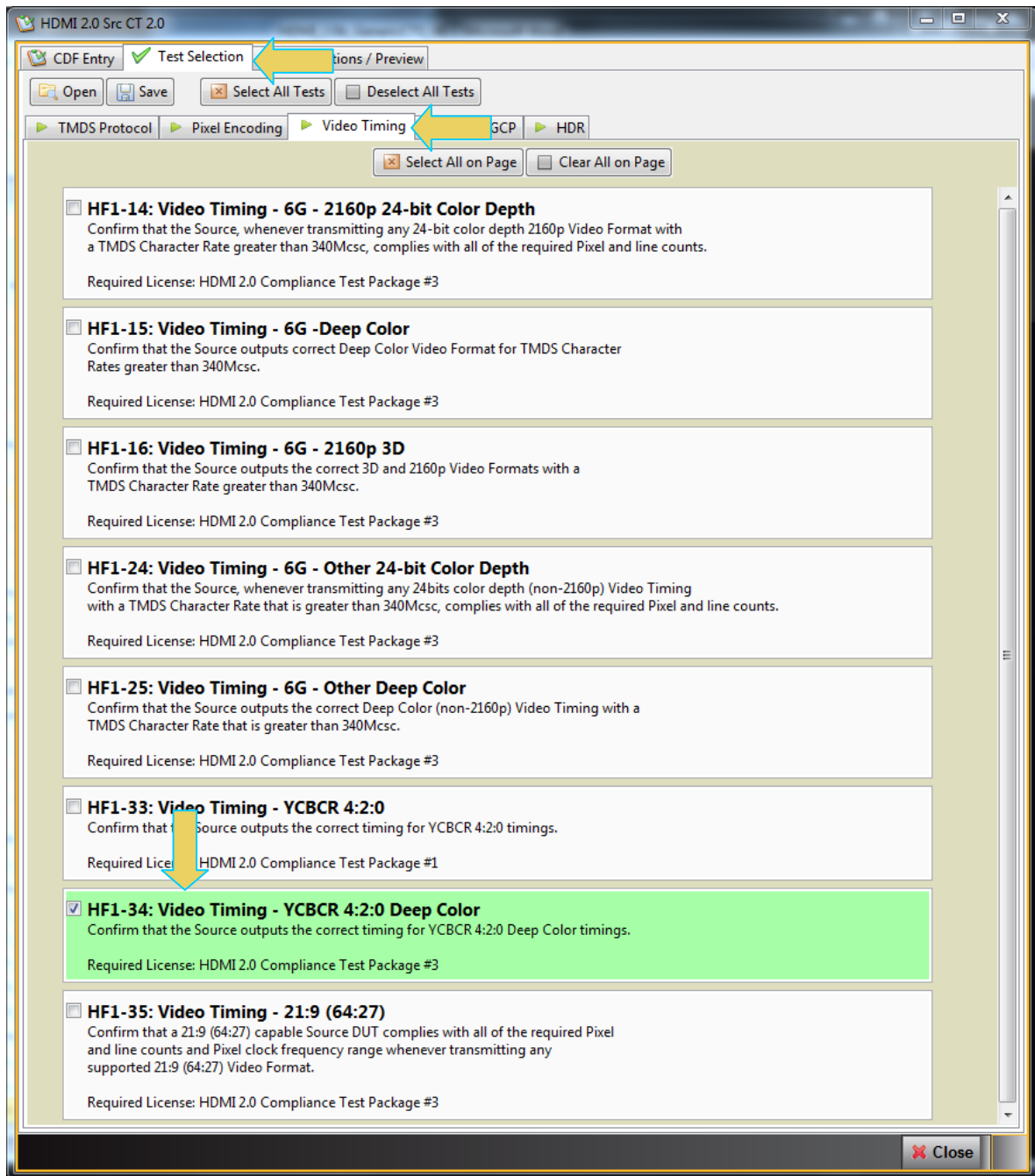
(96) 3840x2160p @ 50 Hz 16:9	<input checked="" type="radio"/> Yes <input type="radio"/> No
(97) 3840x2160p @ 60 Hz 16:9	<input checked="" type="radio"/> Yes <input type="radio"/> No
(101) 4096x2160p @ 50 Hz 256:135	<input type="radio"/> Yes <input checked="" type="radio"/> No
(102) 4096x2160p @ 60 Hz 256:135	<input type="radio"/> Yes <input checked="" type="radio"/> No
(106) 3840x2160p @ 50 Hz 64:27	<input type="radio"/> Yes <input checked="" type="radio"/> No
(107) 3840x2160p @ 60 Hz 64:27	<input type="radio"/> Yes <input checked="" type="radio"/> No

Source_2160p_DC_Video_Formats_Above_340

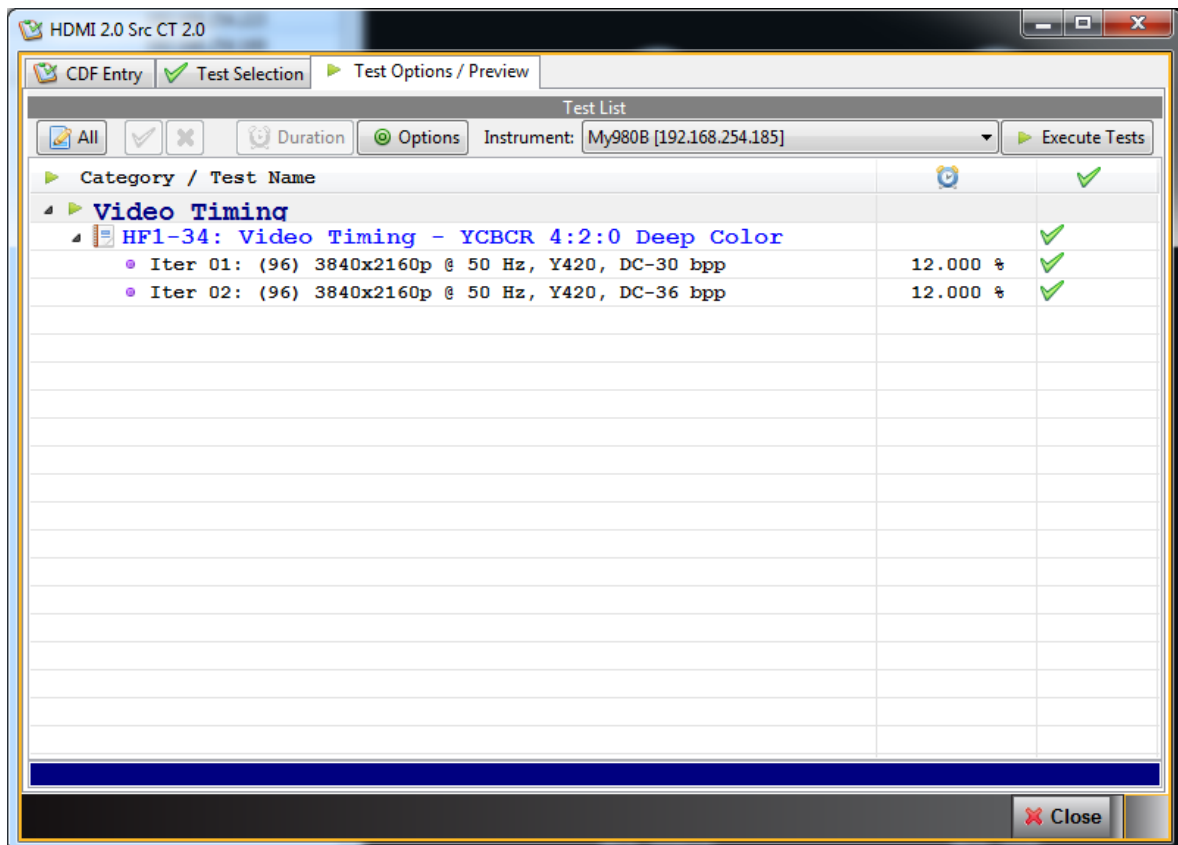
(93) 3840x2160p @ 24 Hz 16:9	<input checked="" type="checkbox"/> 30 <input checked="" type="checkbox"/> 36 <input type="checkbox"/> 48 (bits per pixel)
(94) 3840x2160p @ 25 Hz 16:9	<input checked="" type="checkbox"/> 30 <input checked="" type="checkbox"/> 36 <input type="checkbox"/> 48 (bits per pixel)
(95) 3840x2160p @ 30 Hz 16:9	<input checked="" type="checkbox"/> 30 <input checked="" type="checkbox"/> 36 <input type="checkbox"/> 48 (bits per pixel)
(98) 4096x2160p @ 24 Hz 256:135	<input type="checkbox"/> 30 <input type="checkbox"/> 36 <input type="checkbox"/> 48 (bits per pixel)
(99) 4096x2160p @ 25 Hz 256:135	<input type="checkbox"/> 30 <input type="checkbox"/> 36 <input type="checkbox"/> 48 (bits per pixel)
(100) 4096x2160p @ 30 Hz 256:135	<input type="checkbox"/> 30 <input type="checkbox"/> 36 <input type="checkbox"/> 48 (bits per pixel)
(103) 3840x2160p @ 24 Hz 64:27	<input type="checkbox"/> 30 <input type="checkbox"/> 36 <input type="checkbox"/> 48 (bits per pixel)
(104) 3840x2160p @ 25 Hz 64:27	<input type="checkbox"/> 30 <input type="checkbox"/> 36 <input type="checkbox"/> 48 (bits per pixel)
(105) 3840x2160p @ 30 Hz 64:27	<input type="checkbox"/> 30 <input type="checkbox"/> 36 <input type="checkbox"/> 48 (bits per pixel)

Close

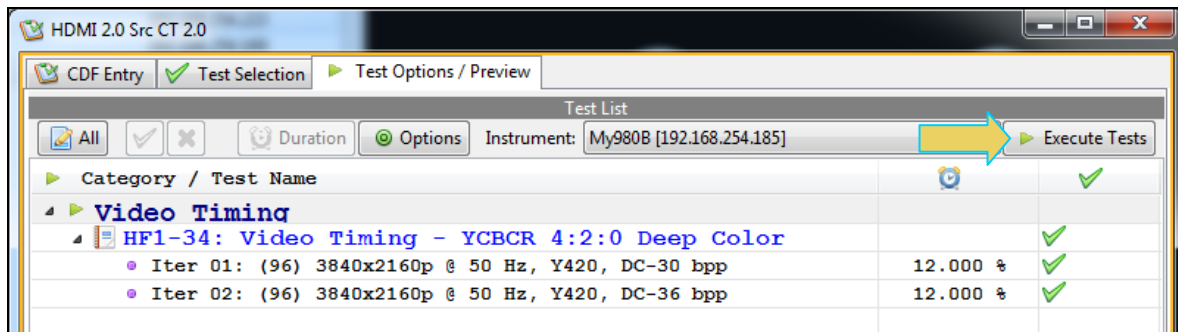
- 4.3 Click on the Test Selection tab and the Video Timing sub tab and select the HF1-34: Source Video Timing YCbCr 4:2:0 Deep Color Test. Refer to the sample screen below.



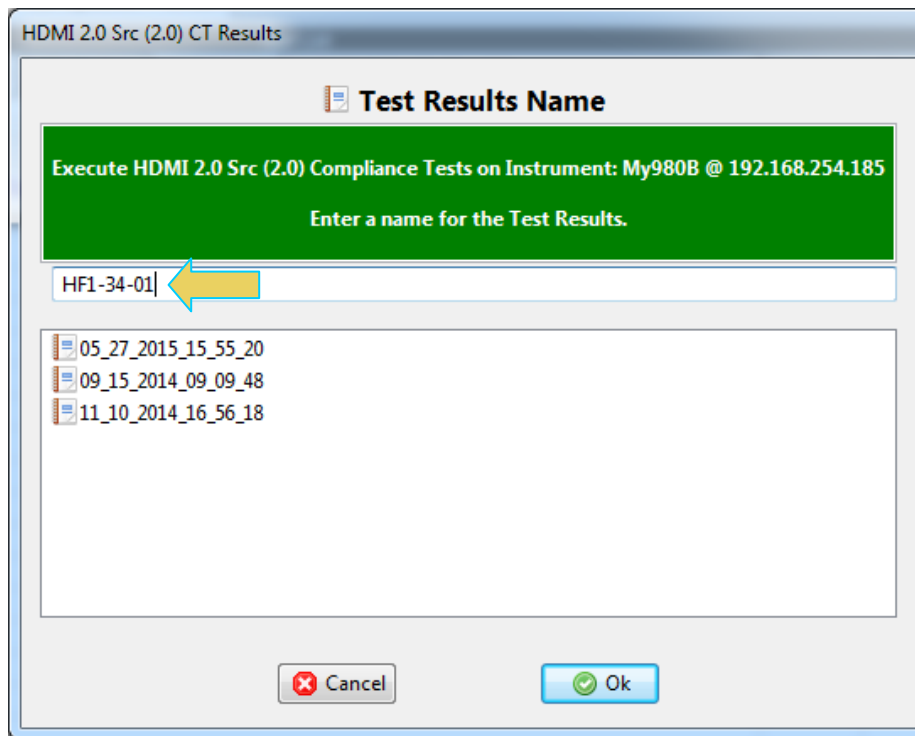
- 4.4 Click on Test Options / Preview tab and review the list of tests. Refer to the sample screen below.



4.5 Click on Execute tests activation button to initiate the test. Refer to the sample screen below.

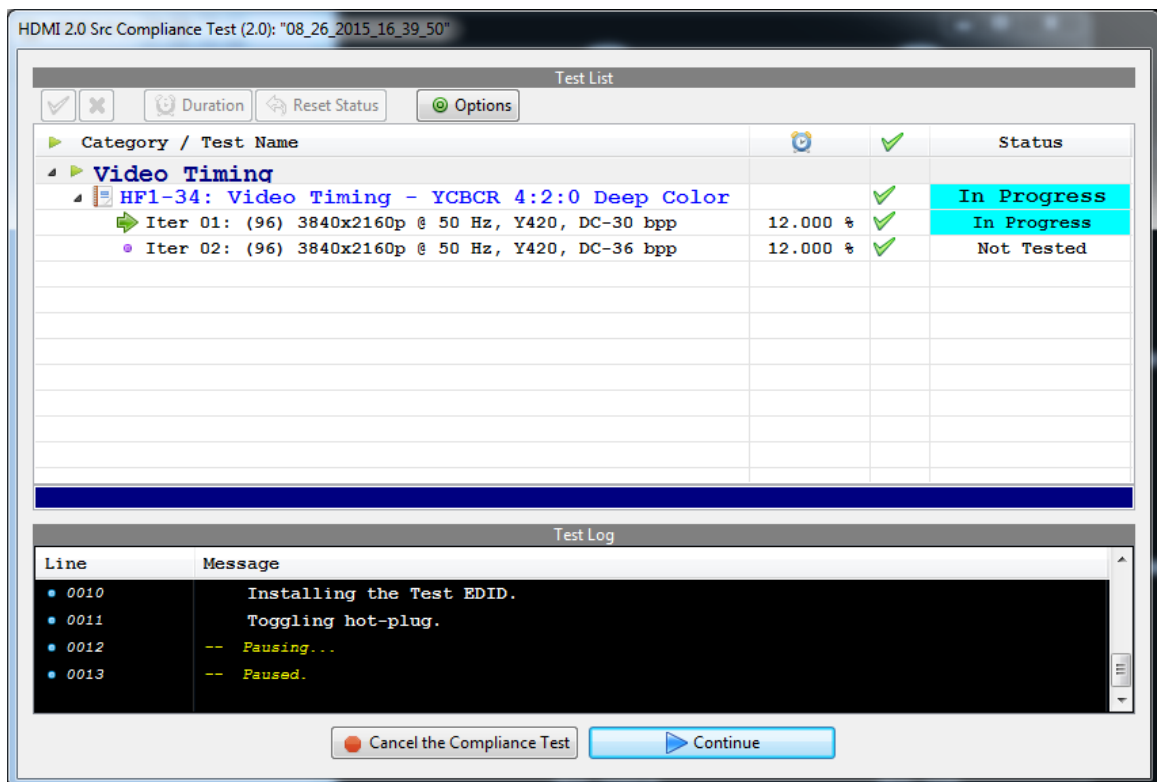


Note: You will be prompted with a dialog box to assign a name to the test results. Refer to the screen example below:

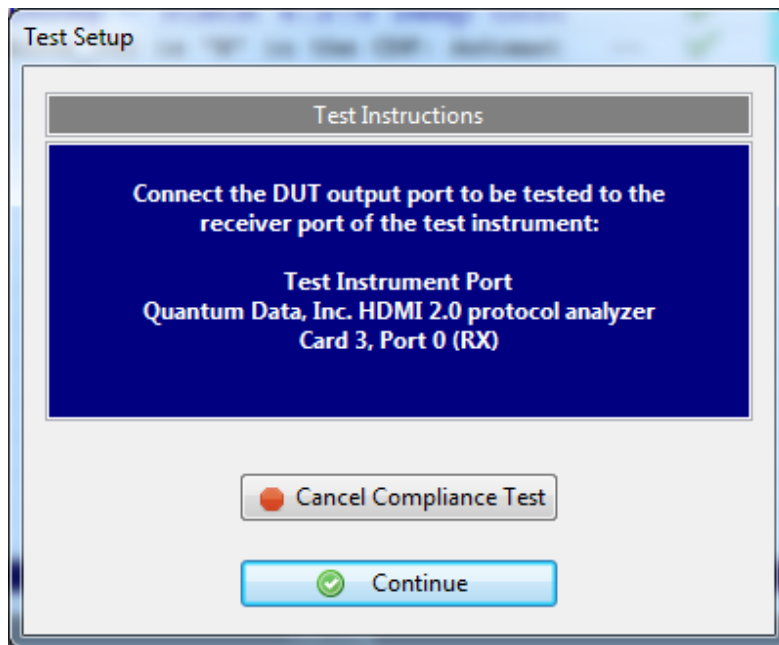


Enter a name, click OK and the test will begin.

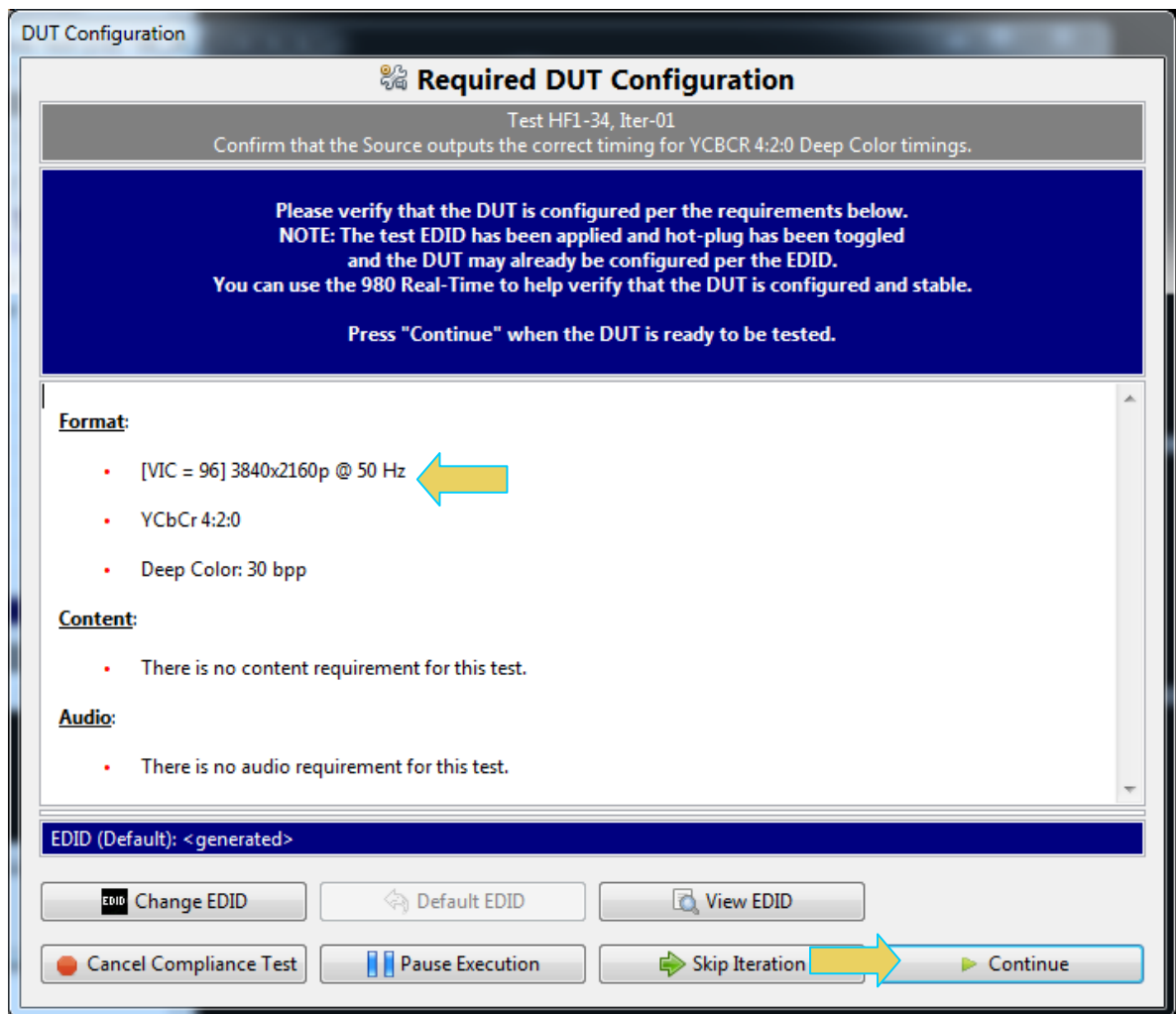
A Test Window will appear (below) indicating the progress of the test.



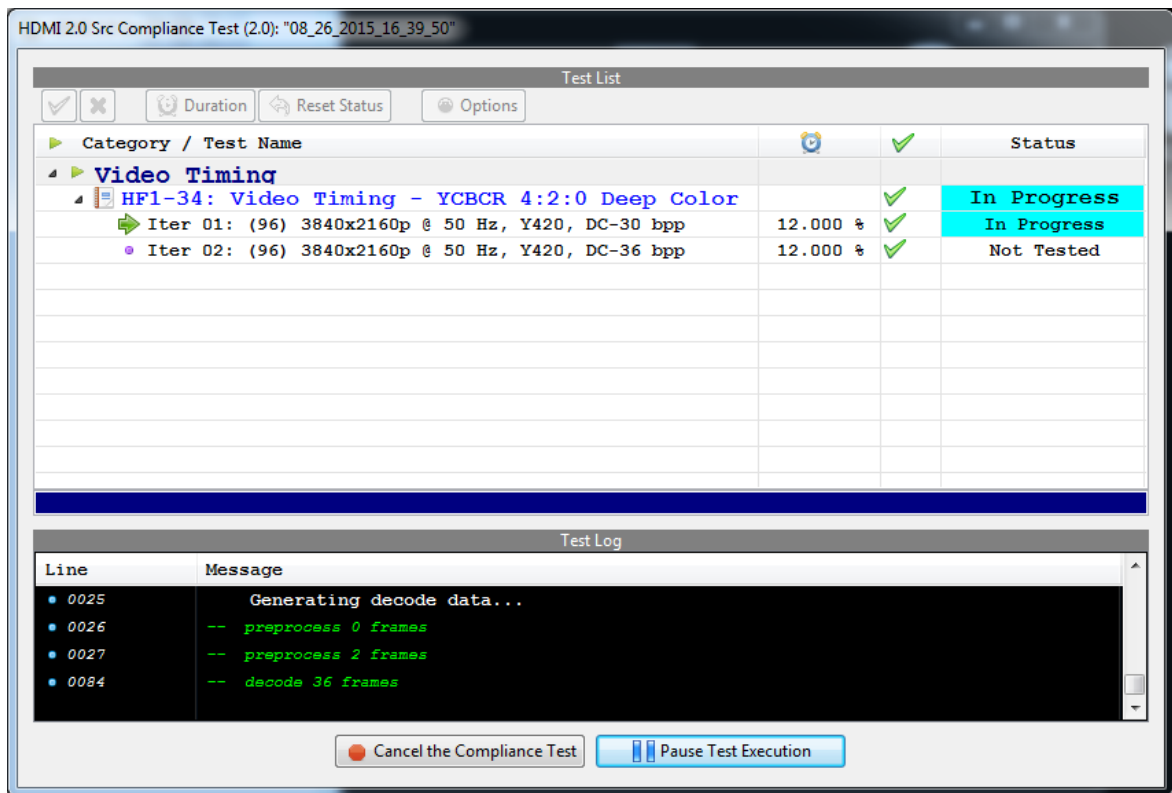
A Test Window will appear (below) with instructions on the proper test setup.



You will be prompted with a dialog box(es) informing you of the requirements of the source DUT. Verify that the source is outputting the required HDMI format and pixel encoding and press Continue to run the test.



The tests will run and you will see a status on the test window.



- 5 If the 980 HDMI Protocol Analyzer's compliance test application reports PASS, then PASS.
If the 980 HDMI Protocol Analyzer's compliance test application reports FAIL, then FAIL.

