

# **High-Definition Multimedia Interface**

**Version 2.0**

**Quantum Data MOI v1.0b**

**Test ID: HF1-35**

July 29, 2015

# Preface

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## Document Revision History

1.0b July 29, 2015 – Updated to reflect approval date and remove limited scope restrictions.

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## Contact Information

The URL for the HDMI Forum web site is: <http://www.hdmiforum.org/>

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# Introduction

This document provides a set of Method of Implementation for test method described in HDMI Compliance Test Specification Version 2.0 (HDMI CTS 2.0). HDMI Forum created HDMI CTS 2.0 to specify a set of tests that should be performed to verify features described in HDMI Specification Version 2.0.

## Scope

This document provides testing procedures for HDMI CTS 2.0 Test ID HF1-35: “Source Video Timing – 21:9 (64:27).” The procedure below deals with single resolution and only one Test ID is considered at a time.

## References

### Normative References

High-Definition Multimedia Interface Specification Version 1.4b, October 11, 2011.  
HDMI Compliance Test Specification Version 1.4b, October 11, 2011.  
High-Definition Multimedia Interface Specification Version 2.0, August, 2013.  
HDMI Compliance Test Specification Version 2.0.

### Informative Reference

No additional informative references.

## Test ID HF1-35: Source Video Timing – 21:9 (64:27)

### Objective

Confirm that a "21:9" (64:27) capable Source DUT complies with all of the required Pixel and line counts and Pixel clock frequency range whenever transmitting any supported "21:9" (64:27) Video Format.

Table 7-60 Source Video Timing – “21:9” (64:27) Requirements

Reference	Requirement
[HDMI 2.0: 7.5]	<See reference for details>

### Capability(s)

The Source DUT supports any “21:9” (64:27) Video Format.

### Test Equipment

Item	Generic Equipment	Vendor Specific Equipment	Quantity
1	Video Timing Analyzer	980 Advanced Test Platform series: 980 HDMI 2.0 Protocol Analyzer module HDMI CTS 2.0 Compliance Test Package #3	1

### Generic Procedure

- 1 If the CDF field SOURCE\_Video\_Formats\_21by9 all are “N”, then SKIP this test.

Setup:

- 2 Connect the Source DUT to a Video Timing Analyzer which contains an EDID with a Video Data Block containing all of the VIC codes (Short Video Descriptor) in the range 65..92 and 103..107.

Measure:

- 3 For each of the VIC codes in the CDF field SOURCE\_Video\_Formats\_21by9, perform the following test (for timing parameters for the VIC's, refer to CEA-861-F table 1,2,3):
  - 3.1 Setup the Source DUT to generate the Video Format associated with this VIC at 24 bit/Pixel.
  - 3.2 Verify that the Source generates an AVI InfoFrame with this VIC at least every 2 frames.
    - 3.2.1 If AVI InfoFrame does not occur at least every 2 frames, then FAIL.
  - 3.3 Check contents of AVI InfoFrame.
    - 3.3.1 If HB1 (AVI InfoFrame version) is not equal to 2, then FAIL.

- 3.3.2 If PB1 bit 7, bits 6 and 5 (Y2, Y1, Y0 fields) does not equal one of 000, 001 or 0101, then FAIL.
- 3.3.3 If PB4 of each AVI InfoFrame does not contain the correct VIC, then FAIL.
- 3.3.4 If bytes PB14 through PB27 are not zero, then FAIL.
- 3.4 Measure the Pixel Clock Rate; if the measured value deviates more than the allowed range described below, then FAIL.
  - For Video Formats with a 25Hz frame rate (or multiples thereof), the measured Pixel Clock Rate shall be within -0.5%/+0.5% of the nominal value.
  - For Video Formats with a 24 or 30Hz frame rate (or multiples thereof), the measured Pixel Clock Rate shall be within -0.6%/+0.5% of the nominal value.
- 3.5 Measure the timing parameters (Hactive, Vactive, Htotal, Hblank, Vtotal, Vblank, Hfront, Hsync, Hback, Hpol, Vfront, Vsync, Vback, Vpol), and check all these values against the nominal values in CEA-861-F tables 1, 2, and 3. If any of the measured values is different from the value listed in these tables for this format, then FAIL.
- 3.6 Visually inspect the video signal generated by the Source DUT.
- 3.7 If the picture is distorted, parts are missing, or the aspect ratio is incorrect, then FAIL.

## Vendor Specific Test Procedure

### Test Equipment

A variety of equipment is needed for testing HDMI products. Each piece is authorized and included by name in this Compliance Test Specification. This section describes the Quantum Data test equipment.

#### HDMI 2.0 Protocol Analyzer module

The Quantum Data 980 HDMI 2.0 Protocol Analyzer module can be installed in the 980B or 980R series Advanced Test Platforms. This 980 HDMI 2.0 Protocol Analyzer module serves the generic test functions called out in the HDMI 2.0 Generic CTS. Refer to the table below:

Item	Quantum Data Equipment	
1	980 Advanced Test Platform series:	
	Equipped with:	980 HDMI 2.0 Protocol Analyzer module
		HDMI CTS 2.0 Compliance Test Package #3

#### 980 HDMI 2.0 Protocol Analyzer Module with 980 Series Platform Configurations

The figures below show depictions of the 980 HDMI 2.0 Protocol Analyzer module equipped in various 980 series platforms. **Note:** Card positioning may vary depending on configuration.



Source Video Timing – 21:9 (64:27)

## Test ID HF1-35: Source Video Timing – 21:9 (64:27)

### 1. Objective

Confirm that a "21:9" (64:27) capable Source DUT complies with all of the required Pixel and line counts and Pixel clock frequency range whenever transmitting any supported "21:9" (64:27) Video Format.

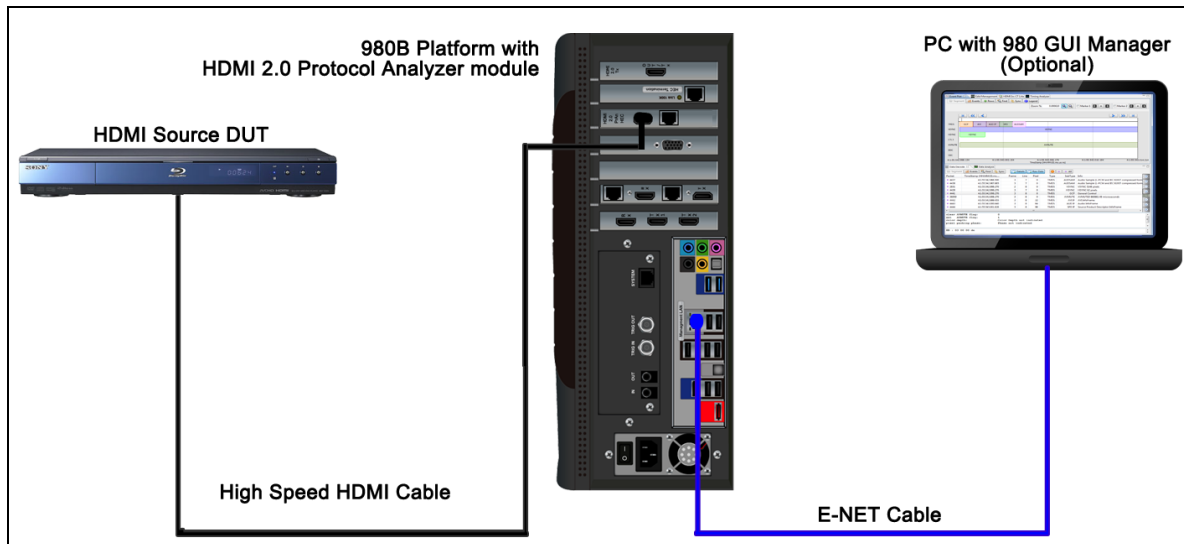
### 2. Test Overview

The Pass/Fail criterion is assessed by the application with no human examination required.

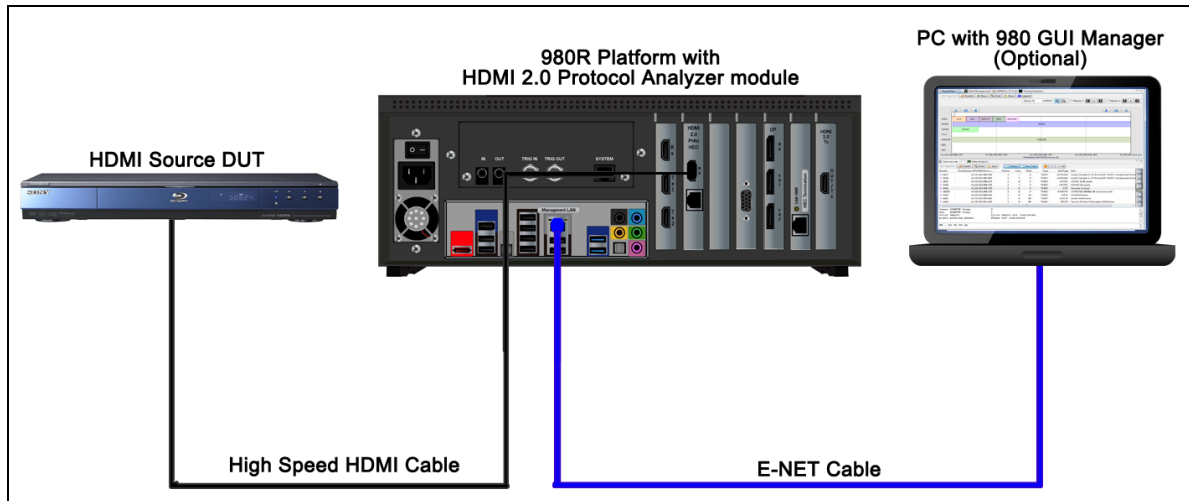
### 3. Procedure

Use the following procedure to conduct this test.

- 1 Connect Source DUT to the Quantum Data 980 HDMI 2.0 Protocol Analyzer at the module's port labeled Rx. Use a High Speed HDMI cable. The figures below show depictions of connections to the 980 HDMI 2.0 Protocol Analyzer module residing in the 980 series chassis.



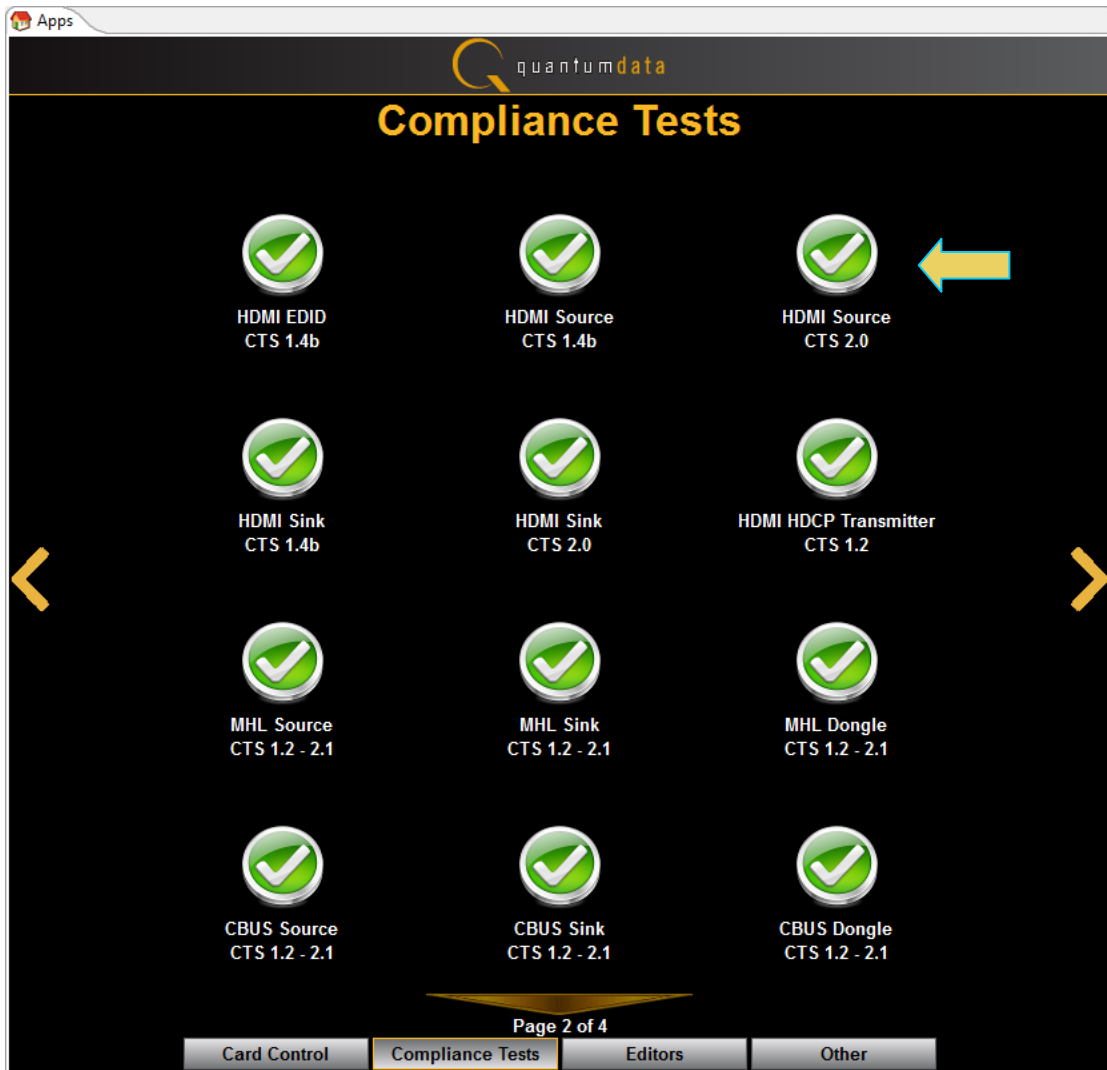




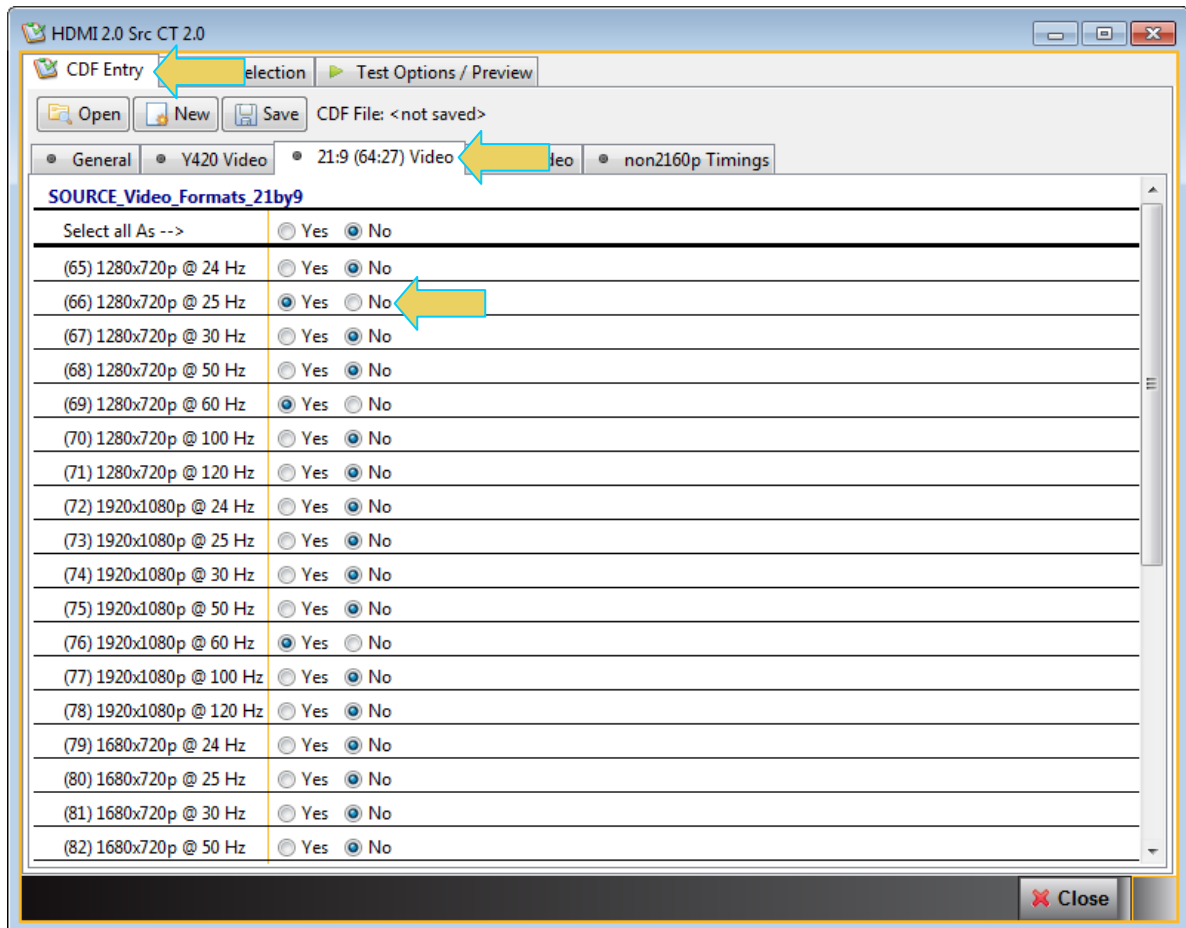
- 2 Operate the Source DUT to output the tested formats.
- 3 Use Quantum Data 980 Embedded Manager GUI (touchscreen) or invoke Quantum Data 980 External Manager GUI (Windows application).

**Note:** You will not need to connect the PC shown in the figures above if you are running the compliance test through the 980's embedded display. The PC running the 980 HDMI 2.0 Protocol Analyzer module's compliance test application is connected to the 980 through a standard Ethernet cable.

- 4 Complete the following steps:
  - 4.1 Click on the HDMI Source CTS 2.0 icon in the Compliance Tests page of the Apps panel.



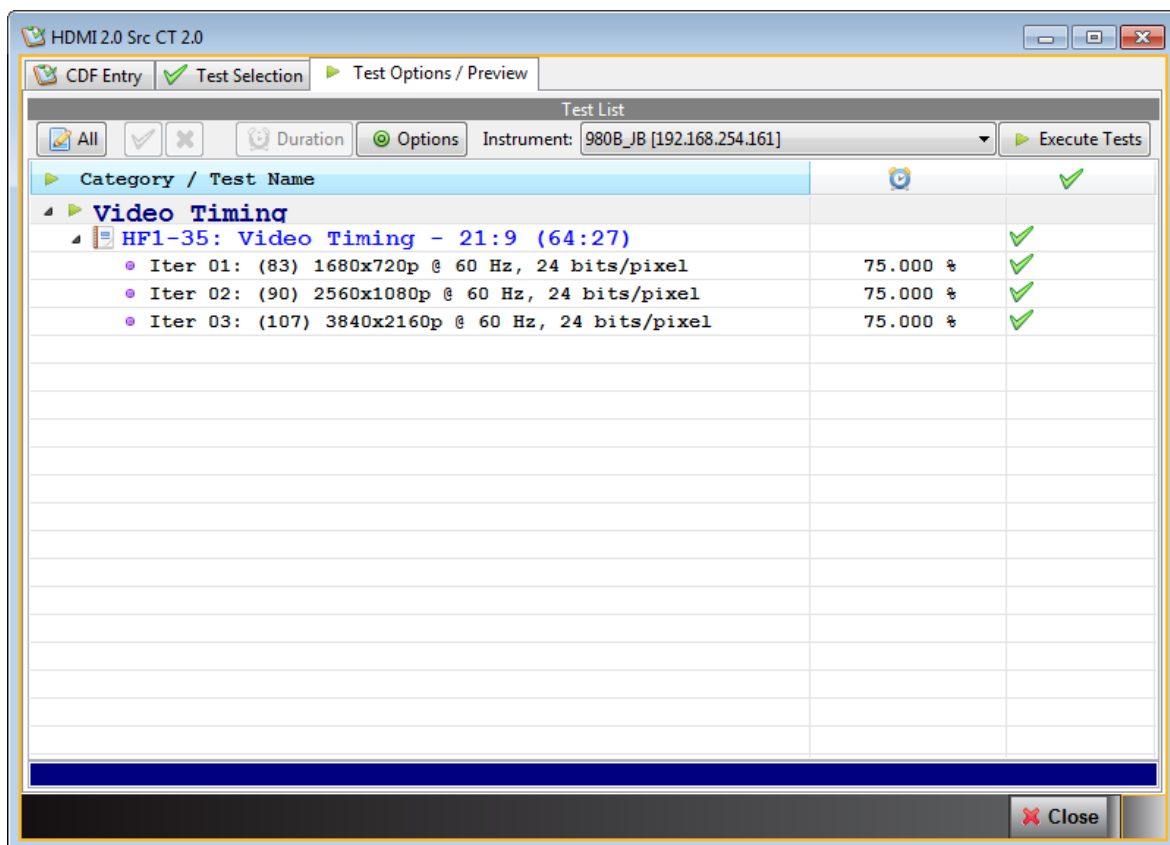
- 4.2 Navigate to the CDF tab if not already there. If there is a saved CDF file, then click on Open and select it. Otherwise, enter the DUT's CDF information for each tab and optionally click on Save to save the CDF. Be sure to check the supported formats on the 21:9 (64:27) Video tab for the SOURCE\_Video\_Formats\_21by9 parameter.



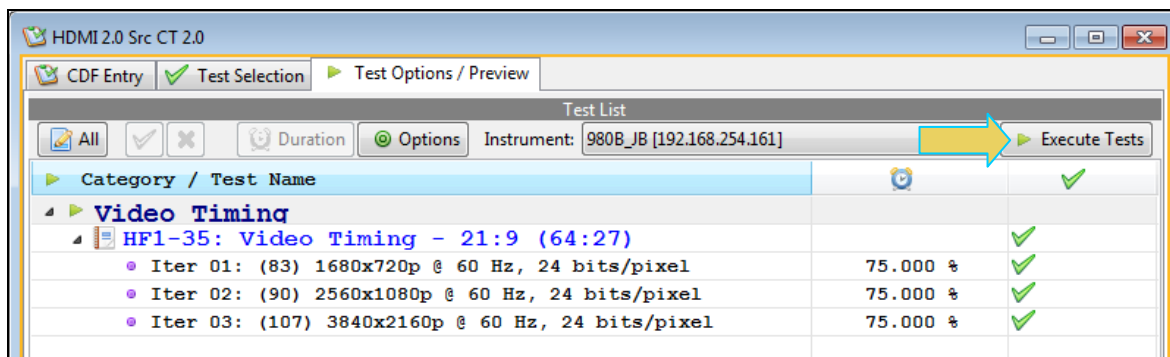
- 4.3 Click on the Test Selection tab and the Video Timing sub tab and select the HF1-35: Source Video Timing – 21:9 (64:27) Test. Refer to the sample screen below.



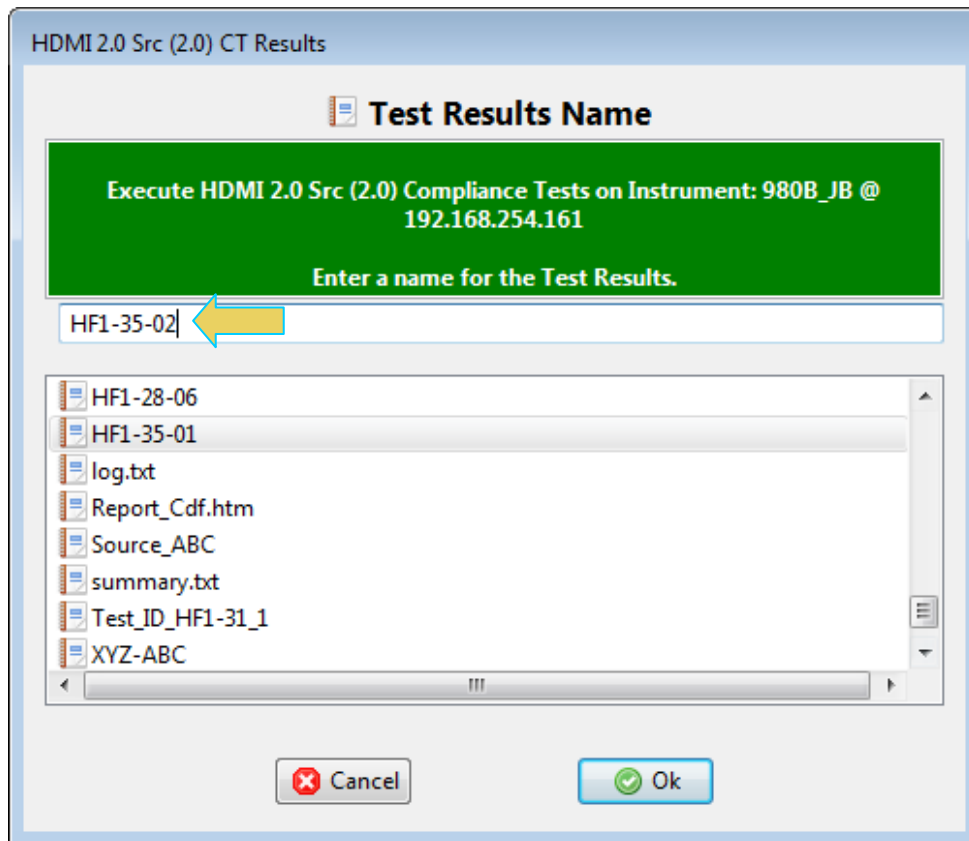
- 4.4 Click on Test Options / Preview tab and review the list of tests. Refer to the sample screen below.



4.5 Click on Execute tests activation button to initiate the test. Refer to the sample screen below.



**Note:** You will be prompted with a dialog box to assign a name to the test results. Refer to the screen example below:



Enter a name, click OK and the test will begin.

A Test Window will appear (below) indicating the progress of the test.

HDMI 2.0 Src Compliance Test (2.0): "HF1-35-02"

Test List

✓ ✕ ⌚ Duration ↺ Reset Status ⚙ Options

Category / Test Name	⌚	✓	Status
▶ Video Timing			
▶ HF1-35: Video Timing - 21:9 (64:27)		✓	In Progress
▶ Iter 01: (83) 1680x720p @ 60 Hz, 24 bits/pixel	75.000 %	✓	In Progress
▶ Iter 02: (90) 2560x1080p @ 60 Hz, 24 bits/pixel	75.000 %	✓	Not Tested
▶ Iter 03: (107) 3840x2160p @ 60 Hz, 24 bits/pixel	75.000 %	✓	Not Tested

Test Log

Line	Message
0009	Installing the Test EDID.
0010	Toggling hot-plug.
0011	Measuring video parameters for capture
0012	Performing the Capture
0013	Starting...

A Test Window will appear (below) with instructions on the proper test setup.

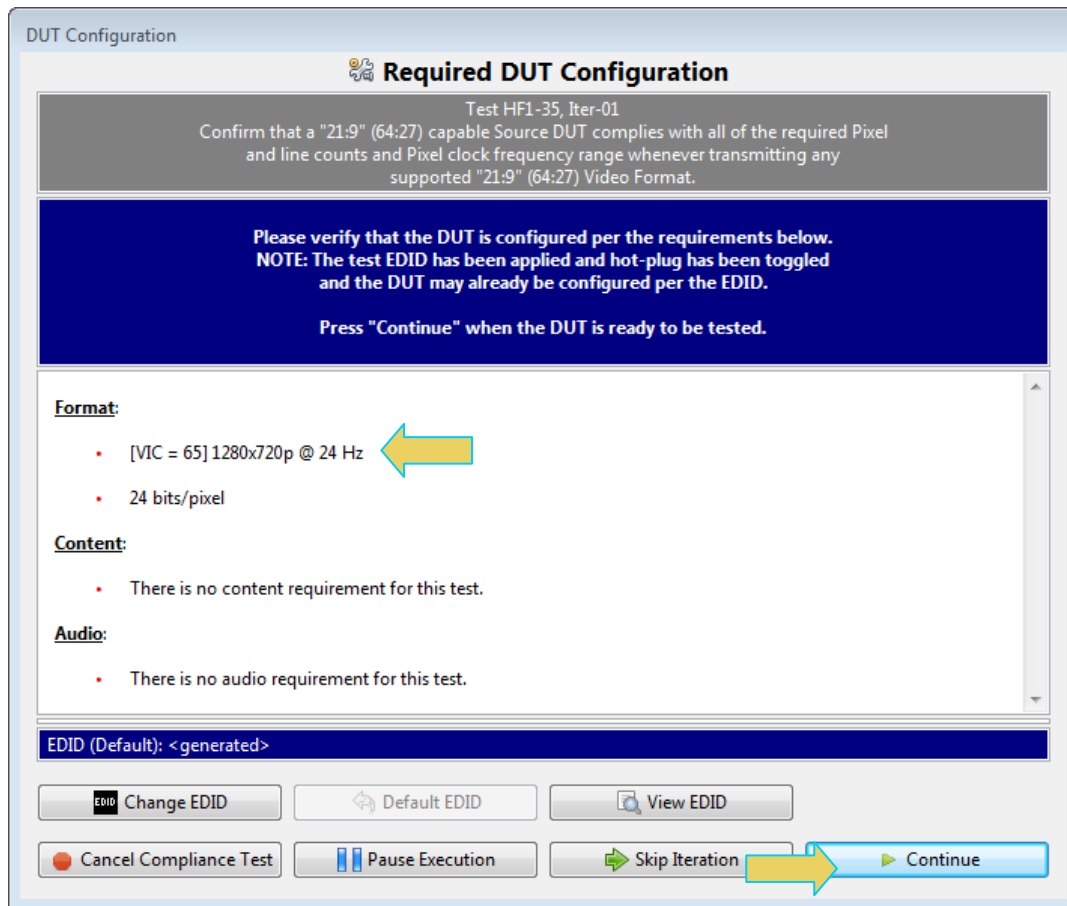
Test Setup

Test Instructions

Connect the DUT output port to be tested to the receiver port of the test instrument:

Test Instrument Port  
Quantum Data, Inc. HDMI 2.0 protocol analyzer  
Card 6, Port 0 (RX)

You will be prompted with a dialog box(es) informing you of the requirements of the source DUT. Verify that the source is outputting the required HDMI format and pixel encoding and press Continue to run the test.



- 5 If the 980 HDMI Protocol Analyzer's compliance test application reports PASS, then PASS.  
If the 980 HDMI Protocol Analyzer's compliance test application reports FAIL, then FAIL.



Compliance Test Results Viewer

HDMI 2.0 Src (2.0) Compliance Test Results

Results Name: HF1-35-02
Date Tested: August 6, 2014 11:07 AM
Overall Status: **CTS 2.0 - Fail**

Manufacturer:
Model Name:
Port Tested: Output 1

HTML Report

Test Results

Test Name / Details		Status
Iter 01: (83) 1680x720p @ 60 Hz, 24 bits/pixel	75.000 %	Pass
01: Verify AVI InfoFrame occurs at least once per two Video Lines		Pass
02: Verify AVI InfoFrame version is equal to 2		Pass
03: Verify PB1 bit 7, bit 6 and 5 (Y2, Y1, Y0 fields) equals 0		Pass
04: Verify PB4 equals the correct VIC		Pass
05: Verify bytes PB14 through PB27 equal to 0		Pass
06: Verify Pixel Clock Rate within the nominal value		Pass
07: Verify the timing parameters against the nominal value		Pass
Iter 02: (90) 2560x1080p @ 60 Hz, 24 bits/pixel	75.000 %	Pass
01: Verify AVI InfoFrame occurs at least once per two Video Lines		Pass
02: Verify AVI InfoFrame version is equal to 2		Pass
03: Verify PB1 bit 7, bit 6 and 5 (Y2, Y1, Y0 fields) equals 0		Pass
04: Verify PB4 equals the correct VIC		Pass
05: Verify bytes PB14 through PB27 equal to 0		Pass
06: Verify Pixel Clock Rate within the nominal value		Pass
07: Verify the timing parameters against the nominal value		Pass
Iter 03: (107) 3840x2160p @ 60 Hz, 24 bits/pixel	75.000 %	Fail

Open Capture
HF1-35: Video Timing - 21:9 (64:27)

Instrument: 980B\_JB [192.168.254.161]
Continue Test Execution

Close